X Band 7.5 W MMIC Power Amplifier for Radar Application

Kyung Ai Lee*, Jong-hoon Chun, and Songcheol Hong***

***Abstract*—An X-band MMIC power amplifier for radar application is developed using 0.25-μm gate length GaAs pHEMT technology. A bus-bar power combiner at output stage is used to minimize the combiner size and to simplify bias network. The fabricated power amplifier shows 38.75 dBm (7.5 Watt) Psat at 10 GHz. The chip size is 3.5 mm × 3.9 mm.**

***Index Terms*—X band, high power amplifier, radar application, MMIC**

I. INTRODUCTION

Currently, there is an increasing demand for X band radar transmitter-receiver (T/R) modules for military and public and space application. In the T/R module, the high power amplifier module is the most current-consuming and the biggest component of the T/R module. Hence, the high power amplifier in the module should preferably be developed as an MMIC for minimization and reproducibility of the module [1,2].

To achieve high output power, power transistors have to be combined. Therefore, power combining-method is very important for high output power and small chip size. For minimizing size and simplifying bias connection, the bus-bar power combiner at the output stage is used. Most of reported researches use the binary-tree combiner topology due to symmetry of bias. However, it has bigger DC current loss and larger size because of long and wide bias paths. This paper presents the design and development of the 7.5-watt X band MMIC power amplifier with bus-bar combiner.

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II. CIRCUIT DESIGN

The power amplifier is implemented with a Triquint's 3MI 0.25 μm GaAs pseudomorphic HEMT technology. A 0.25 μm × 1800 μm transistor is used as a unit transistor. A modified Marteka model was supported as a transistor model. Load-pull source pull simulation is performed using HP ADS to obtain the optimum load and source impedances. At the optimum impedance, the power sweep simulation results of the basic cell are shown in Fig.1. This transistor shows saturated power of 30 dBm and Gain of 12 dB, and 58% PAE under the bias condition of VDS=9 V and IDS=130 mA at the 10 GHz. To get output power above 38 dBm, eight transistors need to be combined at the output stage. Also, to achieve the gain above 20 dBm, two-amplication stage is needed.

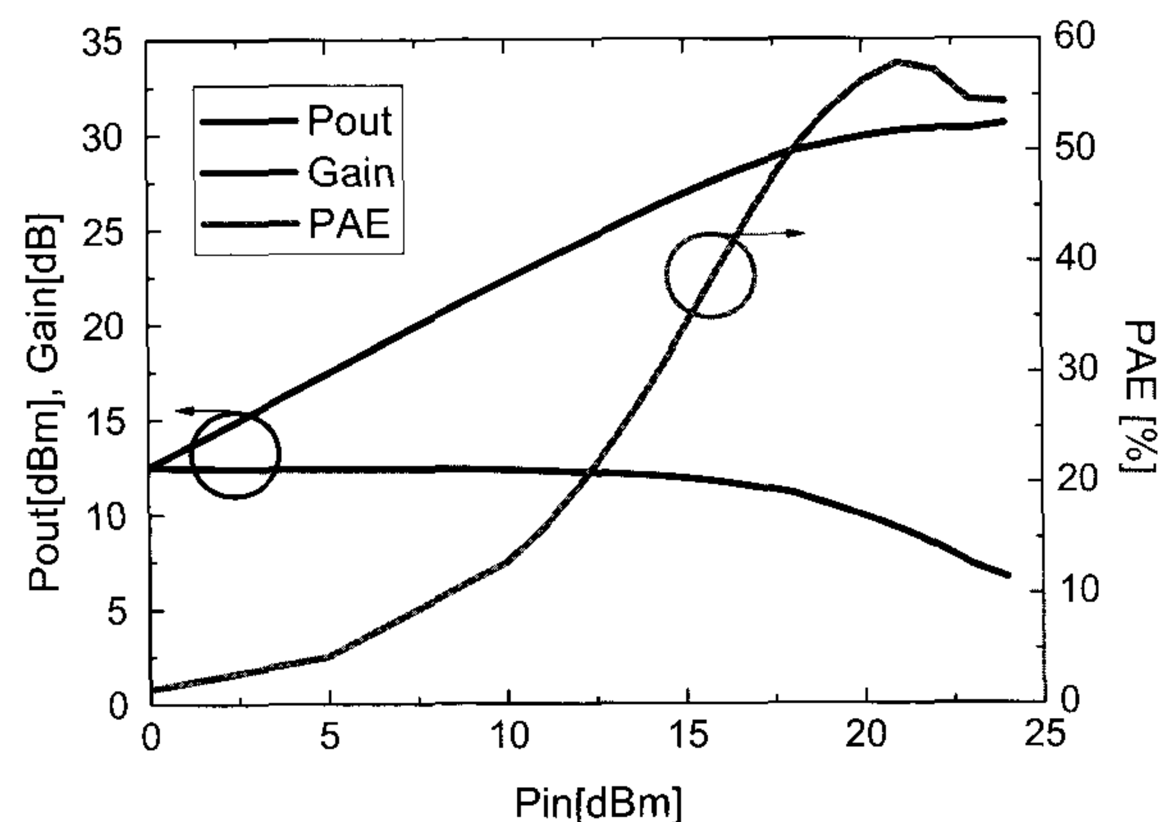

Fig. 1. The power sweep simulation results of the basic cell.

The topology of the power amplifier is shown in Fig. 2. The power combiner for high power amplifier must provide the output matching network for optimum load impedance to the output of the transistor. And it combine the output power of all transistors to the output of the amplifier with as low as possible losses, and it provide the bias supply to the transistors, and it provide DC decoupling to the output [3].

In bus-bar combiner, all the outputs of the last stage devices are connected together by a wide "bus-bar" which feeds DC current to all the devices as shown in fig. [4,5]. The power from the transistors in combined in the wide track, and is tapped-off symmetrically on the output side of bus-bar and fed to a single output using parallel matching network combiner. The advantage of bus-bar combiner is the ease of providing the high DC current to all the output devices form either side of the chip, and this direct bus-bar connection between devices usually eliminates all odd-mode instability [4]. The bus-bar combiner has asymmetry at output of each transistor because of difference of bias path. But, the drain bias line is longer than 1/16λ, the lowering of performance due to those asymmetries in the power amplifier will be negligible [5]. As longer length of the drain bias line increased to 1/4λ, the asymmetries of phase and amplitude are decreased. However, the longer length of the drain bias line needs large chip size. Therefore, the trade-off between performance and chip size is needed.

The resistor between the combined transistors is included to suppress odd-mode oscillation. Also, in order to prevent low frequency oscillation in bias-circuit, RC resonance circuits were included at the gate and the drain-bias line.

III. Measurement Results

Fig. 3 shows a chip photograph of the designed high power amplifier with bus-bar combiner. The chip size is 3.5 mm by 3.9 mm. The performance of the chip was measured with a test fixture that considers the heat dissipations and eliminates the bias-circuit oscillation. The power amplifier is tested with GSG probes. The input power is given by means of a signal generator (Anritsu MG3694A), the output power is detected by means of a spectrum analyzer (HP 8564E), and the gate pulse is given by a function generator. The period of the gate pulse is 10 kHz and the duty rate is 10%.

Fig. 4 shows the measured S-parameters of the power amplifier. The small-signal gain is above 20 dB from 9 to 10 GHz. Input/output return loss is less than -3 dB and -8 dB in band.

The output power characteristics of the power amplifier are shown as Fig. 5 to Fig. 7. These are measured at drain bias of 10 V. The output power characteristics of the power amplifier with input frequency of 9 GHz is shown as Fig. 5. From the figure, the gain of the amplifier is more than 20 dB, the saturated output power is 38.33 dBm (6.8 W). The output power characteristics of the power amplifier with input frequency of 10 GHz is shown as Fig. 6. From the figure, the gain of the amplifier is more than 20 dB, the saturated output power is 38.7 dBm (7.48 W).

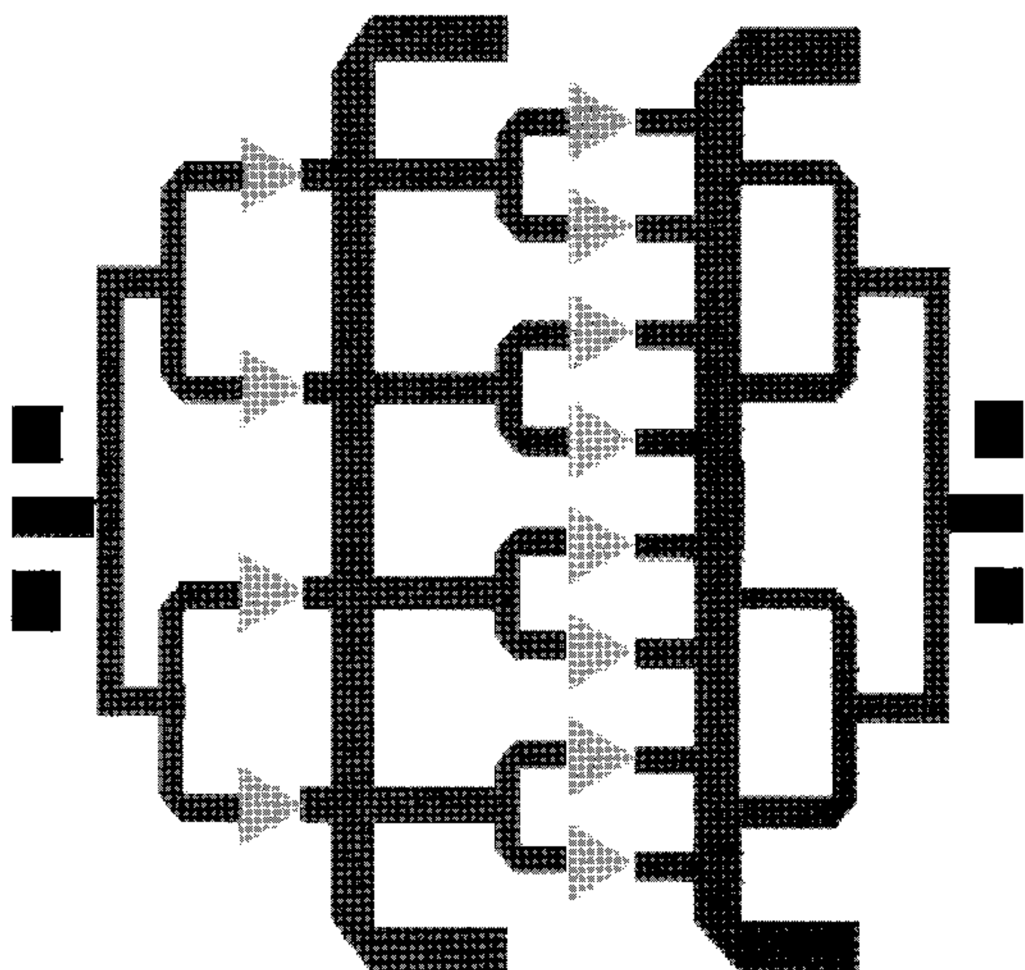

Fig. 2. The topology of the power amplifier with bus-bar combiner.

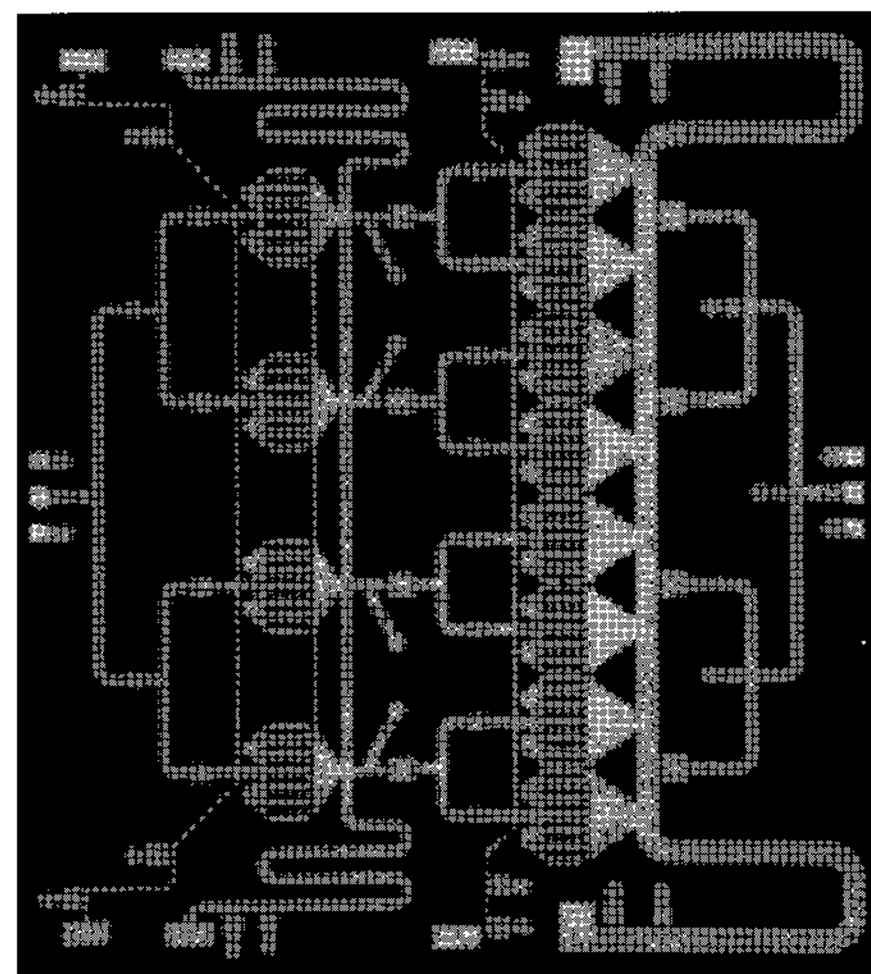

Fig. 3. A chip photograph of the designed high power amplifier.

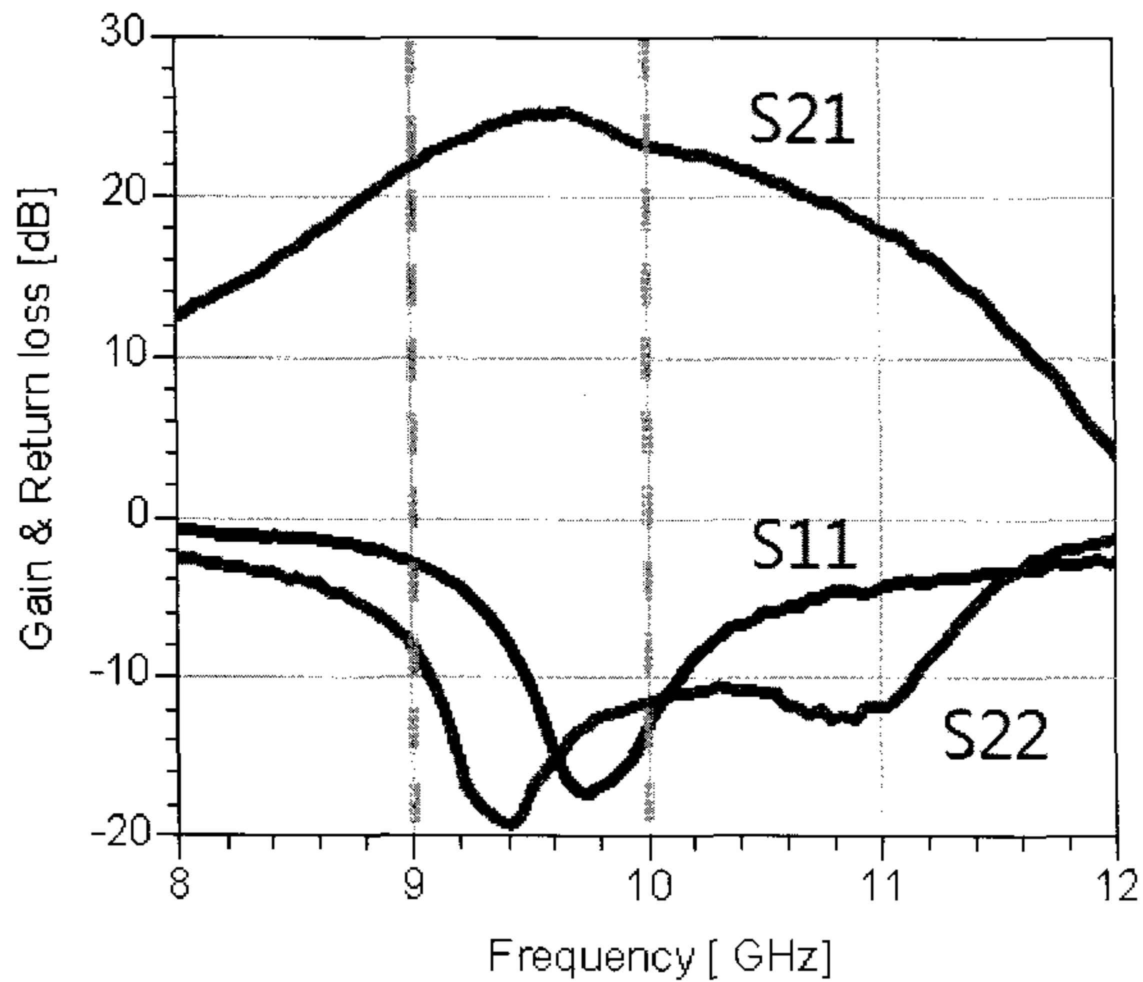

Fig. 4. Measured S-parameters of the power amplifier.

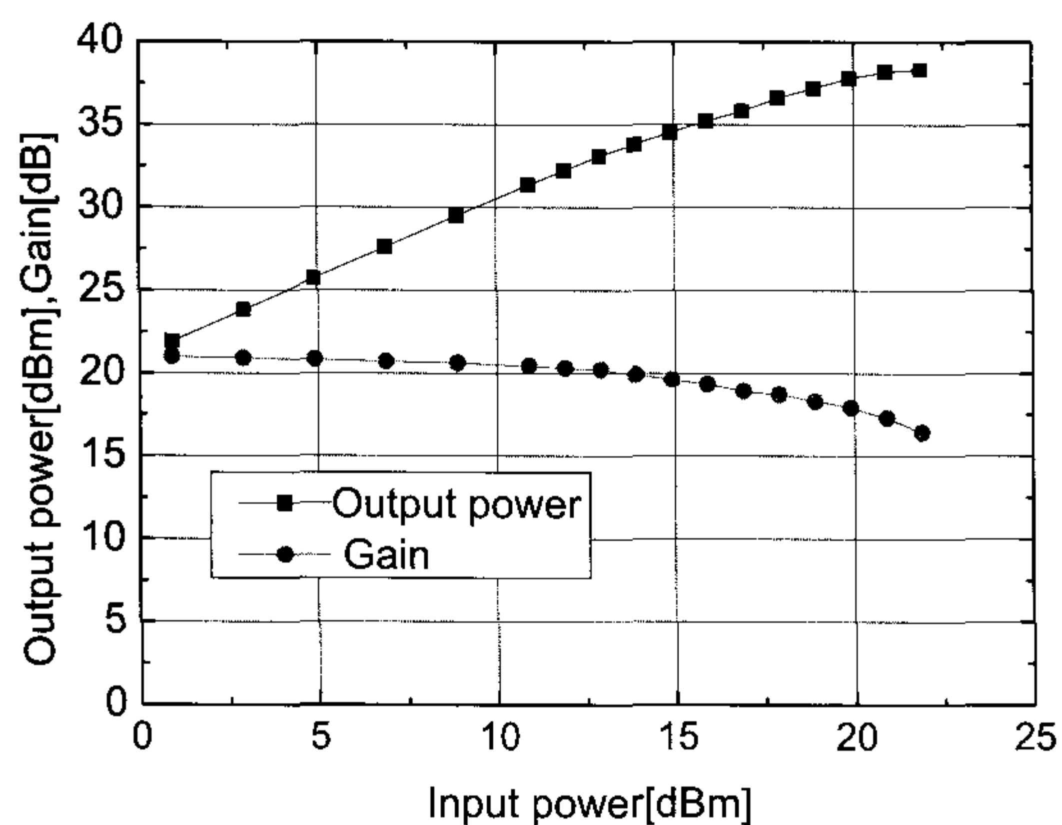

Fig. 5. Measurement results of the output power characteristic of the designed power amplifier (9 GHz).

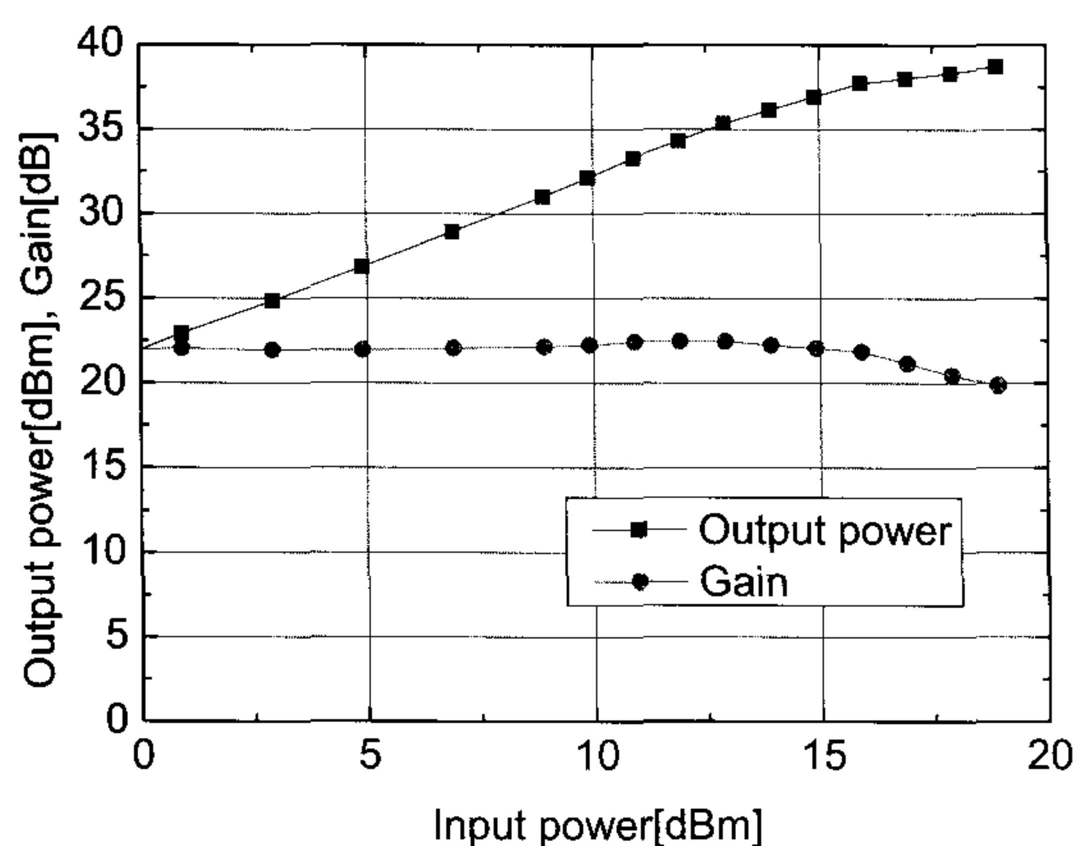

Fig. 6. Measurement results of the output power characteristic of the designed power amplifier (10 GHz).

The variation of output power is shown as Fig. 7 about five power amplifier chips. These are measured at drain bias of 10 V. The saturated powers of all power amplifiers have more s than 37.6 dBm (5.7 W) and the frequency

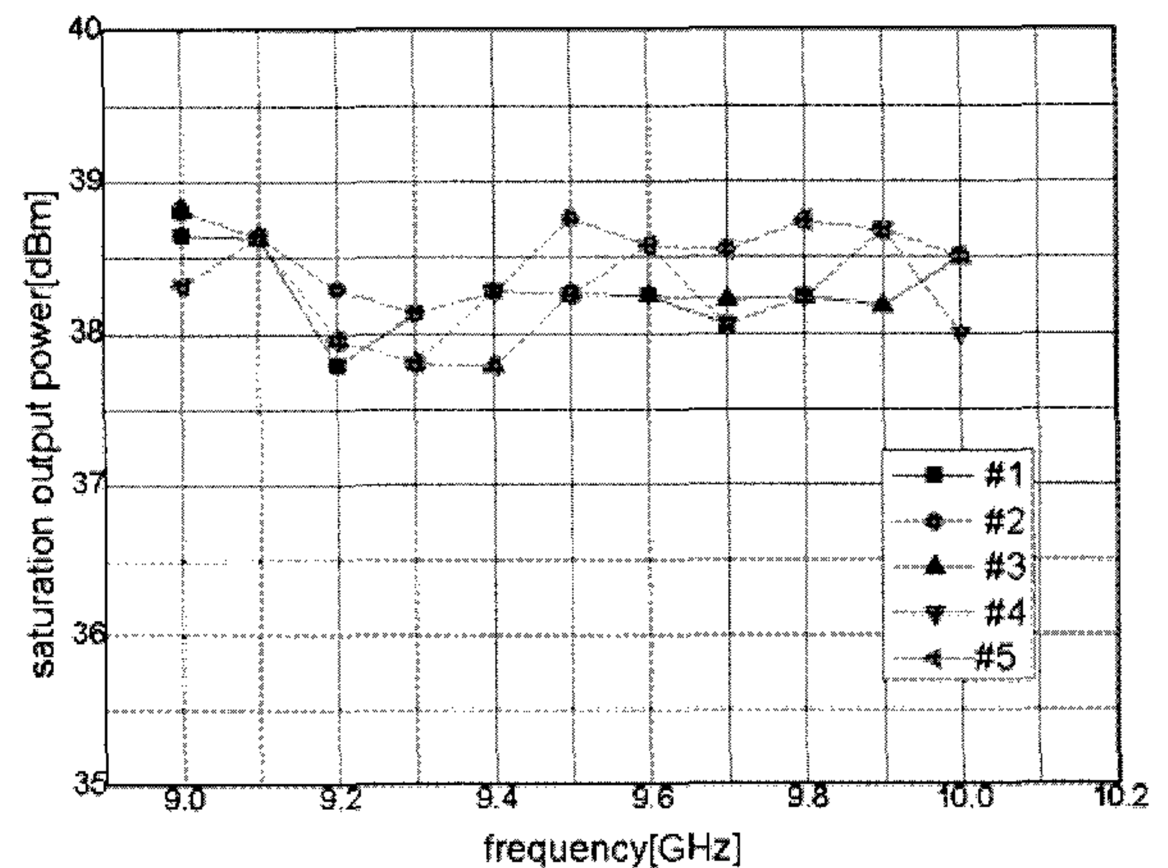

Fig. 7. The sample variation of frequency characteristics of output power.

Table 1. Summary of the measurement results of the power amplifier.

	Measurement results
Bandwidth	9~10 GHz (1 dB)
Power gain	21 dB
Output power (Psat)	5.7 W (37.6 dBm) 7.48 W (38.7 dBm)
Input return loss	< -3
Output return loss	< -8
Supply voltage	10 V

and sample variation of the amplifier is less than 0.5 dB. These measurement results are summarized in Table 1.

IV. CONCLUSIONS

A high power amplifier is designed with bus-bar power combiner. An X-band MMIC power amplifier for radar application is developed using 0.25-μm gate length GaAs pHEMT technology. A bus-bar power combiner at output stage is used to minimize the combiner size and to simplify bias network. This chip has a PSAT of 38.7 dBm (7.48 W) and a gain of 22 dB at 10 GHz. The chip size is 3.5 mm by 3.9 mm.

ACKNOWLEDGMENTS

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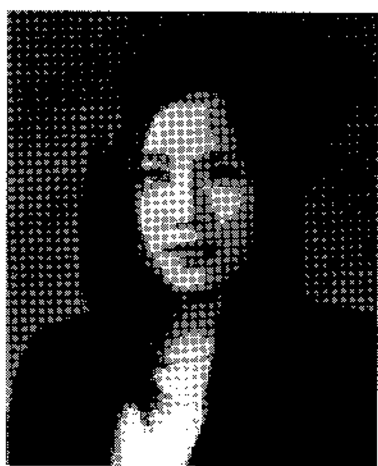

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