Design of a 2.4-GHz Fully Differential Zero-IF CMOS Receiver Employing a Novel Hybrid Balun for Wireless Sensor Network

Shinil Chang*, Jubong Park*, Kwang-Ho Won, and Hyunchol Shin***

Abstract—**A novel compact model for a five-port transformer balun is proposed for the efficient circuit design of hybrid balun. Compared to the conventional model, the proposed model provides much faster computation time and more reasonable values for the extracted parameters. The hybrid balun, realized in 0.18 μm CMOS, achieves 2.8 dB higher gain and 1.9 dB lower noise figure than its passive counterpart only at a current consumption of 0.67 mA from 1.2 V supply. By employing the hybrid balun, a differential zero-IF receiver is designed in 0.18 μm CMOS for IEEE 802.15.4 ZigBee applications. It is composed of a differential cascode LNA, passive mixers, and active RC filters. Comparative investigations on the three receiver designs, each employing the hybrid balun, a simple transformer balun, and an ideal balun, clearly demonstrate the advantages of the hybrid balun in fully differential CMOS RF receivers. The simulated results of the receiver with the hybrid balun show 33 dB of conversion gain, 4.2 dB of noise figure with 20 kHz of 1/f noise corner frequency, and -17.5 dBm of IIP3 at a current consumption of 5 mA from 1.8 V supply.**

Index Terms—**Receiver, balun, transformer, model**

Manuscript received May 22, 2008; revised June 3, 2008.
* High-Speed Integrated Circuits and Systems Laboratory, Kwangwoon University, Seoul, Korea
** Ubiquitous Computing Research Center, Korea Electronics Technology Institute, Seongnam, Korea
E-mail : hshin@kw.ac.kr

I. INTRODUCTION

A novel hybrid balun circuit that can be applied to a fully differential CMOS receiver was proposed for a power-efficient and high-performance single-to-differential conversion [1]. In this work, we describe design results of a fully differential direct conversion receiver employing the novel hybrid balun. Although it is originally designed for 2.4-GHz ZigBee applications, the fully differential receiver design in this work will be also applicable to other wireless communication and broadcasting applications such as tuners [2]. First, a novel five-port compact model of a transformer-based balun is proposed. The proposed model is more compact than the conventional model and thus allows fast and flexible time-domain circuit simulations. A zero-IF receiver is comprised of a low noise amplifier, passive mixers, and baseband amplifiers. Comparative investigations on three receiver designs, each employing the hybrid balun, a simple transformer balun, and an ideal balun, clearly demonstrate the advantages of the hybrid balun.

II. HYBIRD BALUN DESIGN AND RESULTS

The hybrid balun is composed of a passive transformer and loss-compensating auxiliary amplifiers. Since the passive transformer balun typically shows better signal symmetry and linearity than an active balun circuit, we utilize the passive balun as a main signal path. The unwanted insertion loss of the passive balun is then compensated by the auxiliary amplifiers. Fig. 1 shows the simplified circuit schematic of the hybrid balun. It also illustrates the RF signal flow to depict how the

signals are compensated. A common-drain and common-source amplifiers compensate the in-phase and inverted-phase signals, respectively. Signal phases from the auxiliary amplifiers are aligned with less than 15 degree of mismatch to the signals transferred through the transformer. Bias currents of the two compensating amplifiers are reused to save the total current consumption in the hybrid balun.

For the design of the hybrid balun circuit, the core transformer must be properly designed first. Five-port S-parameters of a transformer can be obtained by using an electromagnetic simulation tool such as an FEM-based HFSS. However, such mere s-parameters can not be directly used in the time-domain circuit simulations. Thus, an equivalent circuit model of the transformer is needed in order to carry out various time-domain circuit simulations.

In this work, we propose a novel and compact lumped-element equivalent circuit model of a transformer. Fig. 2 shows the proposed model of the five-port transformer. For comparison, a conventional model is shown also in the inset. The conventional model involves six non-ideal k-factors (k_{12}, k_{13}, k_{14}, k_{23}, k_{24}, k_{34}) between primary and secondary windings [3,4]. We have found that the complexity of the conventional model, which is mainly due to the six k-factors, causes the calculation speed to slow down and the extracted parameter values to be in an unreasonable range. The proposed model eliminates the six k-factors by replacing the coupled-transformer with an ideally coupled transformer with a proper magnetizing inductance (TF1, TF2, TF3, L_1, L_4), as can be seen in Fig. 2. TF1 and TF2 are needed for describing the main magnetic coupling path in the transformer. Meanwhile, TF3 that represents the magnetic coupling between the two halves of the secondary windings is found to be crucial in enhancing the modeling accuracy of the differential characteristics of the output signal. Also, R_M is included to improve the accuracy of Q-factor.

Fig. 3 compares the modeling accuracy of the conventional and proposed models. As can be seen, the proposed model provides comparable level of accuracy compared to the conventional model, but with much simpler equivalent circuit. Due to such simplicity, the proposed model converges about ten times faster and significantly shortens circuit simulation time than the conventional model.

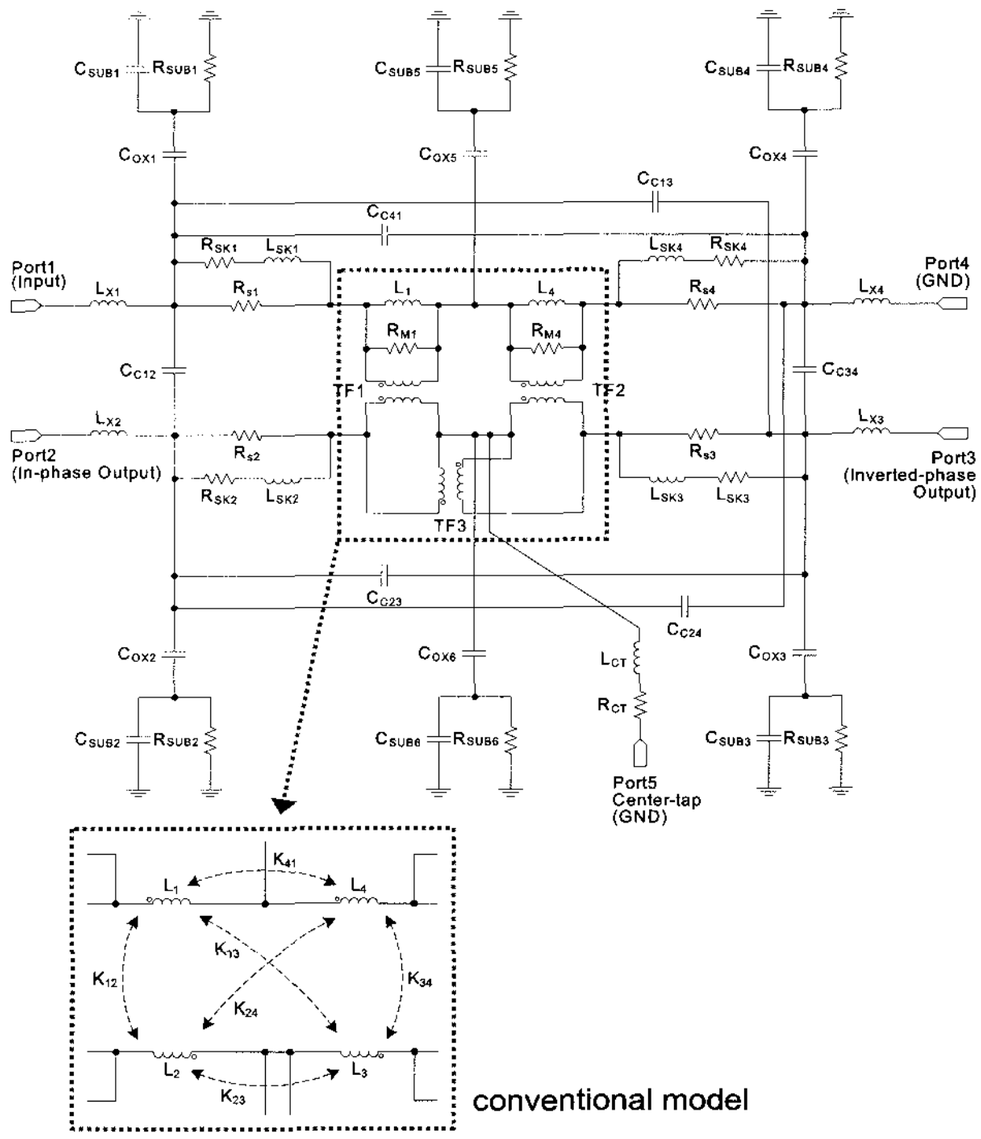


Fig. 2. Proposed compact model of five-port transformer-based balun. Inset shows the conventional model.

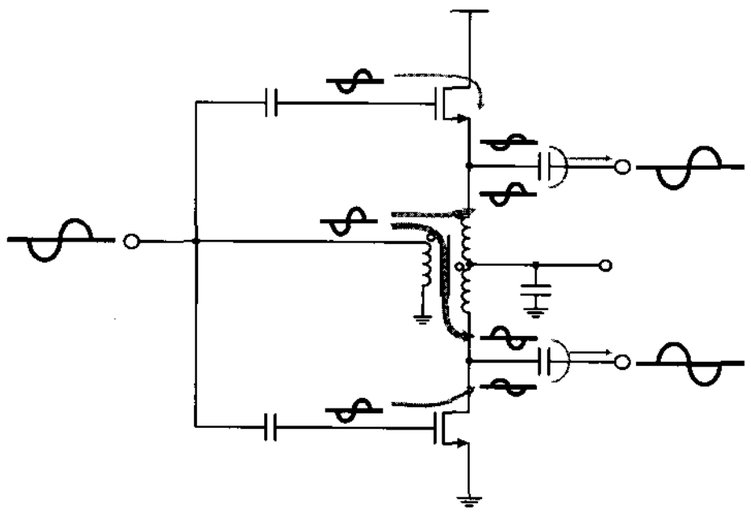


Fig. 1. Simplified Circuit schematic and RF signal flow of hybrid balun.

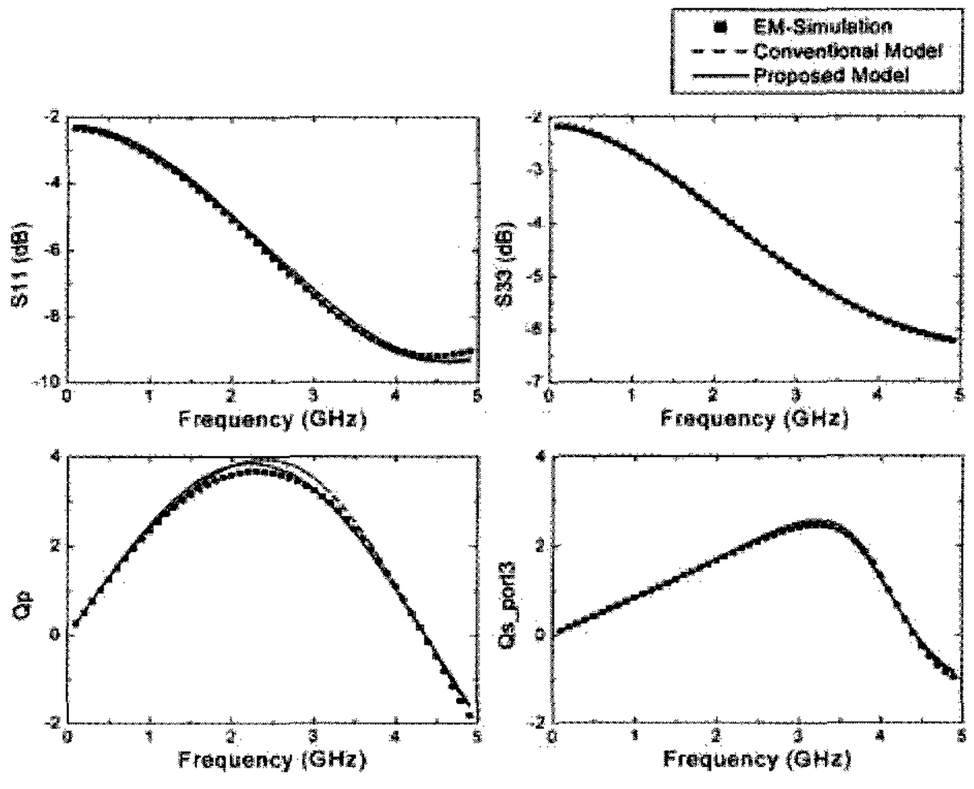


Fig. 3. Comparison of modeling accuracy.

The proposed model also generates reasonable parameter values. Table 1 compares the extracted parameter values for the proposed and conventional models. The extracted value of the primary inductance in the conventional model (L_1+L_4) is 1.55 nH, which is totally different from the real inductance value of 2.76 nH. By contrast, the primary inductance (L_1+L_4) of the proposed model is extracted to be 2.51 nH, which is very close to the real inductance value. Moreover, the extracted value of a parasitic inductance L_{sk2} is 38.52 nH in the conventional model, which is physically unreasonable. By contrast, it is found to be 412 pH in the proposed model, which is much more reasonable.

The proposed compact model is employed to the hybrid balun circuit design. Fig. 4 compares the measured and simulated gains of the hybrid and passive balun. At 2.4 GHz, the gains of the passive balun and hybrid balun are -3.6 dB and -0.8 dB, respectively. As can be seen, the simulated results show excellent agreement with the measured results. It proves the validity of the proposed transformer model. Detailed description of the 2.4-GHz hybrid balun design can be also found in [1].

Table 1. Comparison of the model parameter values for the conventional and the proposed models.

	L_{sk1}	L_1	L_2	L_3	R_{sk1}	R_{sk2}	R_{sk3}	R_{sk4}	R_{sk5}	R_{sk6}	R_{sk7}	R_{sk8}
Conventional Model	0.9 nH	0.65 nH	0.52 nH	0.61 nH	0.03 Ω	7.72 Ω	5.9 Ω	6.2 Ω	17.3 Ω	253.6 Ω	55.8 Ω	44.7 Ω
Proposed Model	1.256 nH	1.255 nH	na	na	16.8 Ω	3.94 Ω	11.4 Ω	8.8 Ω	4.6 Ω	11.27 Ω	19.21 Ω	9.4 Ω
	C_{sk1}	L_{sk2}	L_{sk3}	L_{sk4}	K_{12}	K_{23}	K_{24}	K_{41}	K_{13}	K_{24}	R_{sk9}	R_{sk10}
Conventional Model	460 pH	38.52 nH	11.0 nH	6.63 nH	0.99	0.99	1.0	0.41	0.86	0.99	na	na
Proposed Model	16 pH	412 pH	3 pH	12 pH	na	na	na	na	na	na	432 Ω	380 Ω

III. Zero-IF Receiver with the Hybrid Balun

A fully differential zero-IF receiver is designed for wireless sensor network applications. In order to realize the fully differential structure, the hybrid balun is adopted in front of a differential LNA. A passive mixer is used to reduce the 1/f noise and lower the current consumption. Fig. 5 shows the circuit schematic of the designed receiver.

The low noise amplifier takes a fully-differential cascode topology. The series inductor L_S at the source node is used to achieve simultaneous noise and input matching. Adding the L_S, however, requires extremely large gate width for minimum noise factor and input matching simultaneously, which easily leads to high current consumption. Therefore, we add an additional capacitor C_{EX} between the gate and source nodes to resolve this design conflict. Gain and frequency control capability is implemented by using a variable resistance

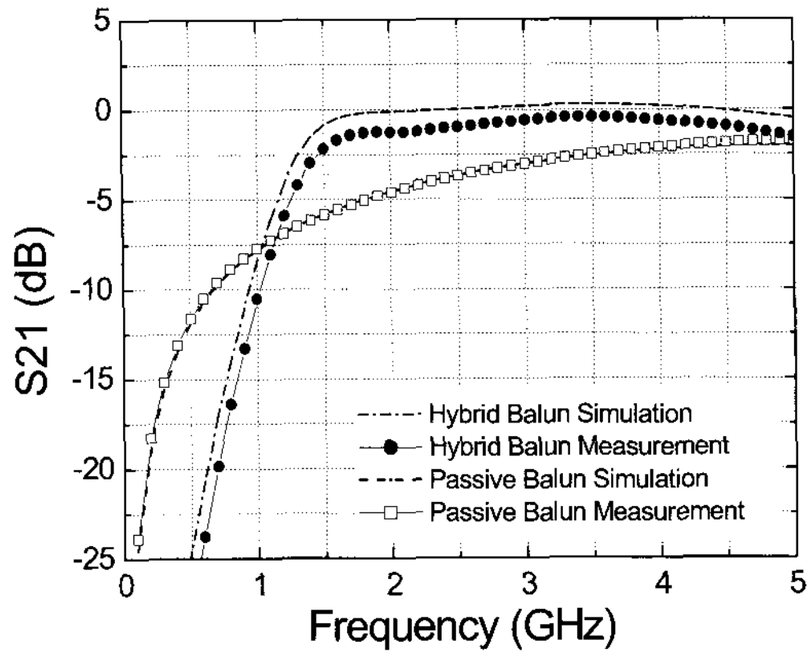


Fig. 4. Measured gain of the hybrid and passive balun.

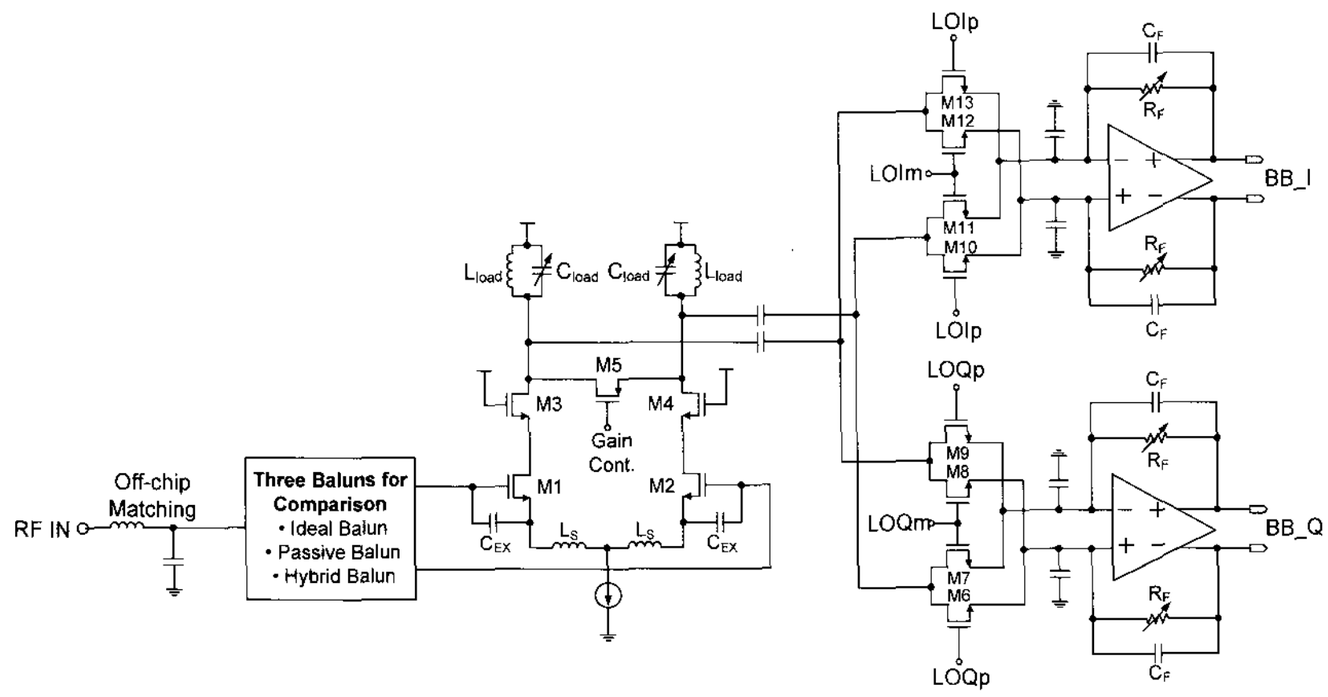


Fig. 5. Simplified circuit schematic of the fully differential direct conversion receiver.

(M5) and a tuned load (L_{load}, C_{load}), respectively. Fig. 6(a) illustrates the equivalent circuit of the LNA-to-mixer interface part. The LNA is modeled by $g_m v_i$, C_{out}, and a variable resistance R_{out}. And the tuned resonant circuit is represented by L_{load} and C_{load}. Input impedance of the passive mixer is represented by C_{in} and R_{in}. Fig. 6(a) is then further simplified to Fig. 6(b). As depicted in Fig. 6(c), the gain is tuned by controlling the equivalent resistance via R_{out}, and the center-frequency is tuned by adjusting the capacitance via C_{load}.

The passive switching mixer is employed to reduce the 1/f noise, lower the current consumption, and enhance the linearity. But, a rather big conversion loss involved with the passive mixer is disadvantageous compared to an active counterpart. The mixer is followed by an op-amp active RC filter. Fig. 7 shows the circuit schematic of the op-amp. It uses a two stage design for obtaining high gain and low noise. The input stage uses PFET for low 1/f noise characteristic.

Optimal design of the mixer with respect to the following op-amp filter stage is crucial for the total receiver performance. Fig. 8 depicts the equivalent circuit of that part. The input impedance of op-amp $Z_{in}(s)$ is given by

$$Z_{in}(s) \approx \frac{2}{A(f)+1} \cdot \frac{R_F}{1+sC_F R_F} \tag{1}$$

where $A(f)$ is the open loop gain of the op-amp. The on-resistance of the passive mixer given by

$$R_{on} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L}\left[V_{GS} - V_{TH}\right]} \tag{2}$$

Usually $Z_{in}(s)$ is very low in the frequency range of our interest since $A(f)$ is very high. Thus the input impedance of the mixer, Z_{load} can be expressed by

$$Z_{load}(s) = R_{on} + Z_{in}(s) \tag{3}$$

If R_{on} is relatively high, the transfer gain to the op-amp input port becomes small and results in low gain and high noise figure. By contrast, if R_{on} is relatively small with a large gate width of the switching FET, a larger amount of noise is sampled during the switching process due to large parasitic capacitances, and as a result, significantly increases the noise figure. Too large width also leads to higher swing at the op-amp input port, which leads to a linearity degradation [5, 6]. The linearity requirement of receivers for wireless sensor network is not as stringent as other cellular communication standards. Thus we optimize the mixer width by putting more focus on the noise figure and power consumption rather than the linearity. Fig. 9 shows the gain, noise figure, and IIP3 performances with respect to the gate width of the switching

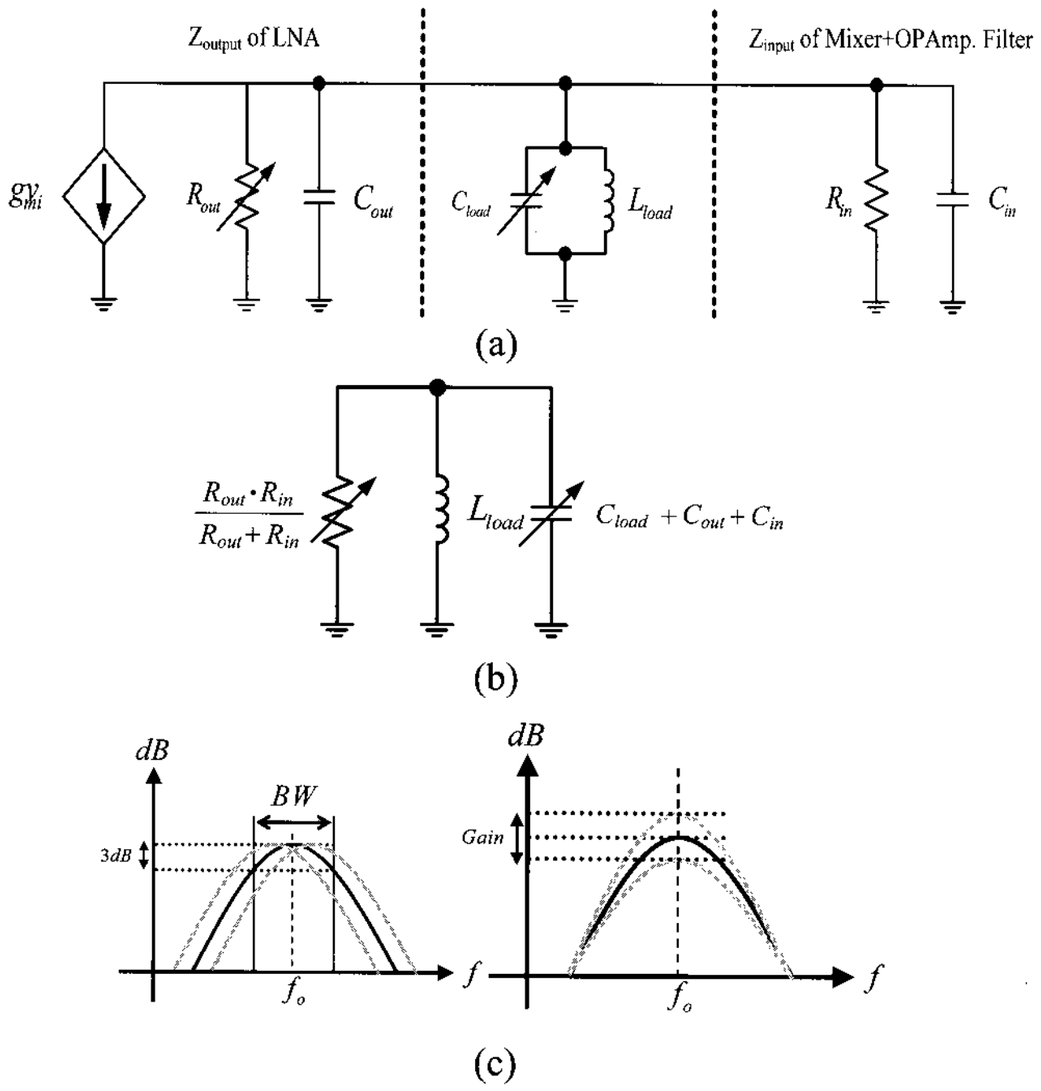


Fig. 6. (a) Equivalent circuit of the LNA-mixer interface. (b) Simplified equivalent circuit of (a). (c) Gain and frequency tuning characteristics.

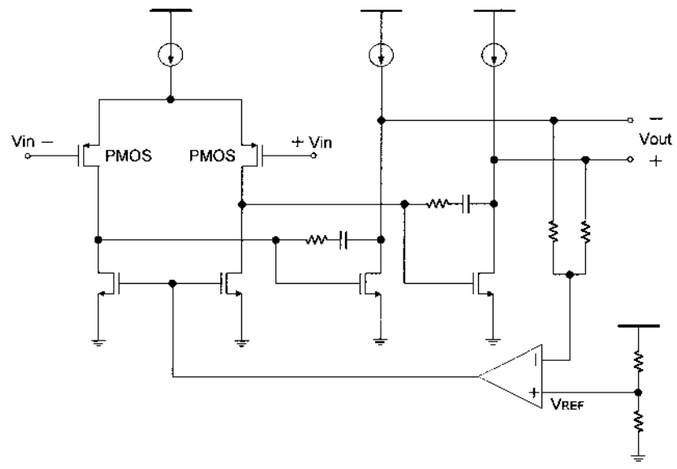


Fig. 7. Circuit schematic of the two-stage operational amplifier.

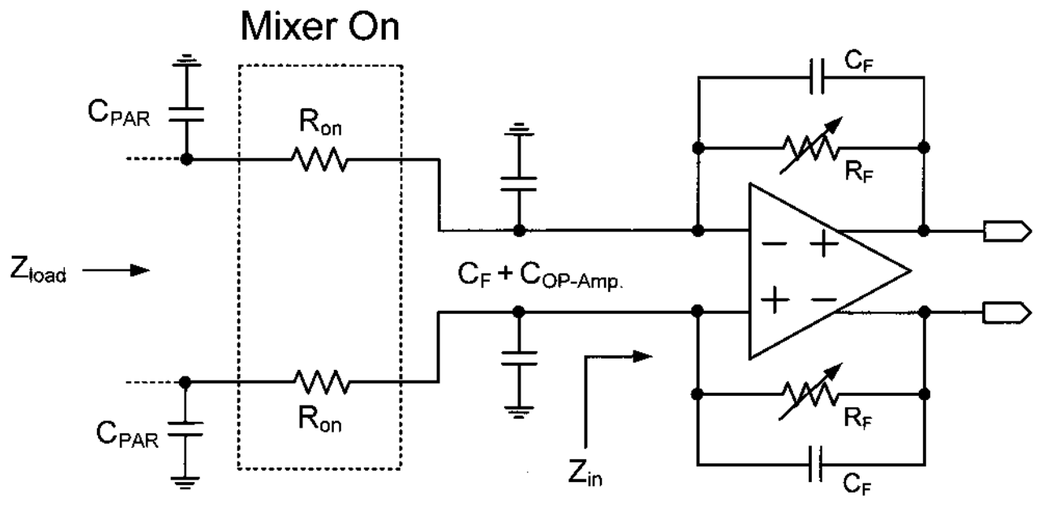


Fig. 8. Equivalent circuit of the interface between the mixer and baseband amplifier.

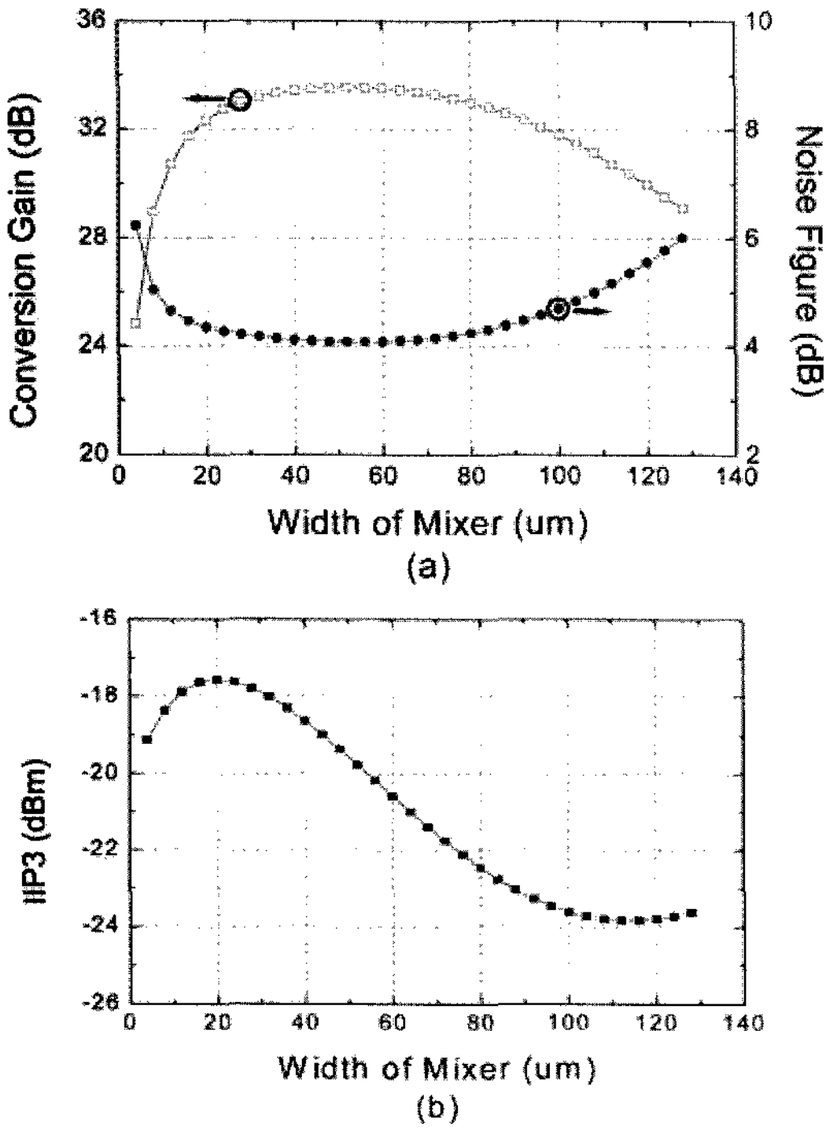
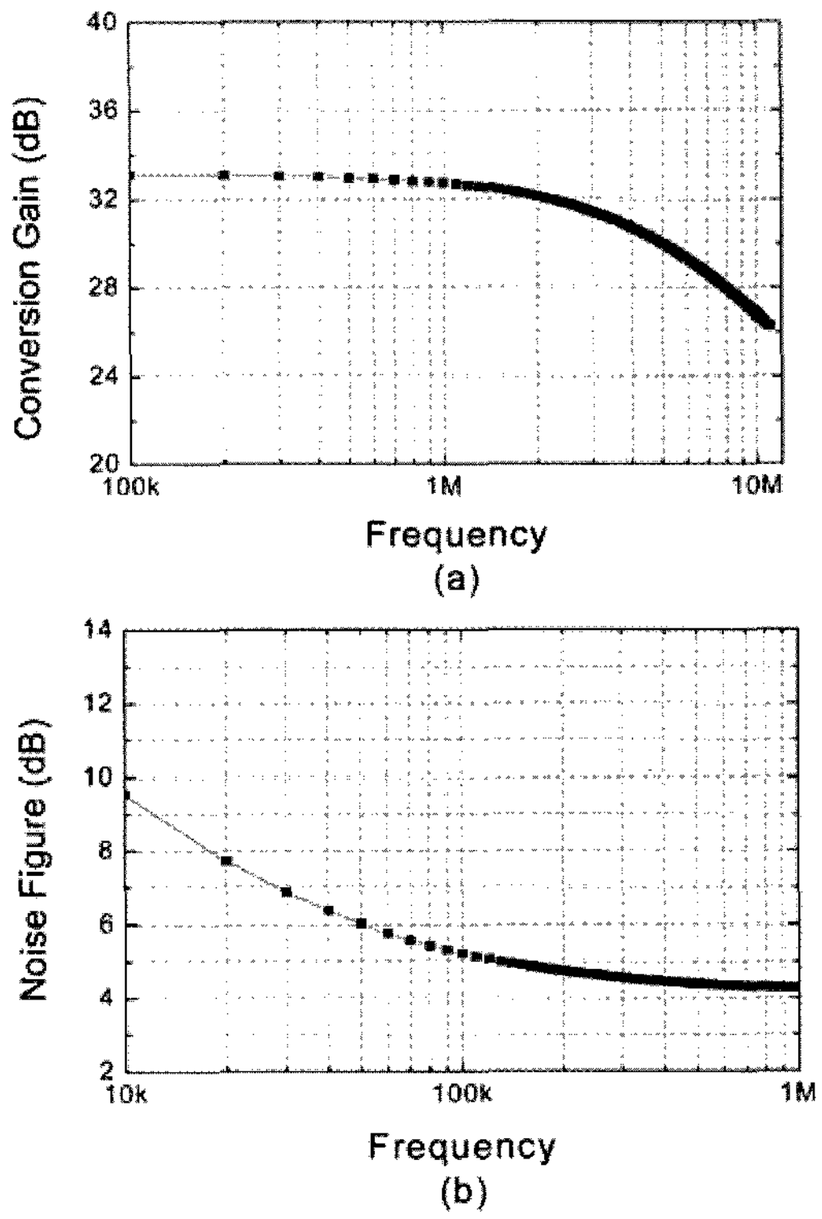


Fig. 9. (a) Gain and noise figure and (b) IIP3 of the receiver with respect to the gate width of the passive mixer.

FET, in which LNA's current consumption is fixed at 3 mA and the load of the baseband amplifier is set to 800 Ω. The optimum width is found to be in the range of 20 μm to 30 μm, and 24 μm is chosen in our design.

Fig. 10 shows simulated results of the conversion gain, noise figure, and IIP3 of the receiver when it employs an ideal transformer balun in front of the LNA. We obtain the +33 dB of gain, the 3-dB cutoff frequency of 4.8 MHz (Fig. 10(a)), 4.2 dB of noise figure with 1/f noise corner frequency of 20 kHz (Fig. 10(b)), and IIP3 of -17.5 dBm (Fig. 10(c)). The current consumption is 5 mA from a 1.8 V supply.

By using this initial receiver that employs the ideal balun, we extend the design to incorporate the passive balun and the hybrid balun. Fig. 11 compares the performances of the receivers employing the ideal, passive, and hybrid baluns. As can be seen, the performances of the hybrid-balun receiver are almost comparable with the ideal-balun-based receiver, whereas the receiver with the passive balun shows much inferior performances. Table 2 summarizes performances of the three receivers each employing the ideal, passive, and hybrid balun, respectively. The hybrid-balun-based receiver achieves higher gain by 2.7 dB and lower noise figure by 1.8 dB compared to the passive-balun-based receiver. All



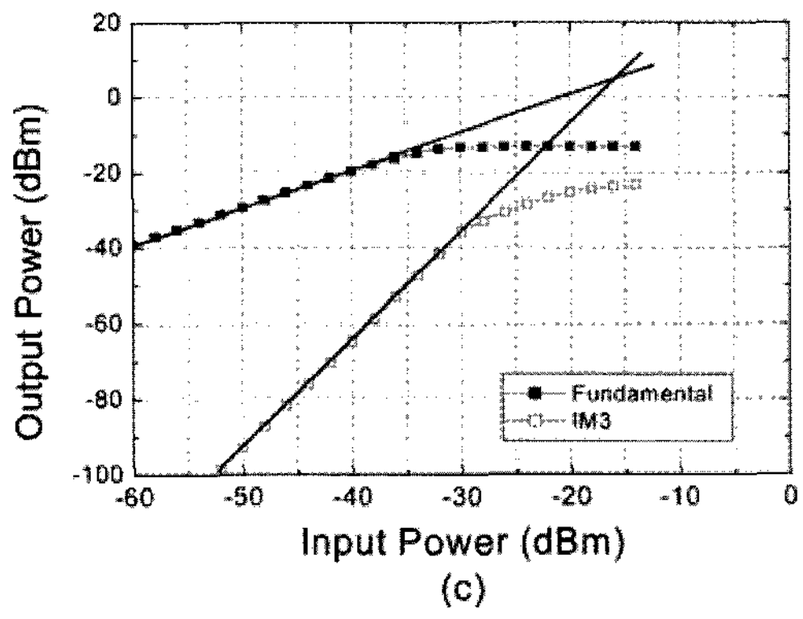


Fig. 10. Simulation results of Zero-IF receiver (a) gain (b) noise figure and (c) IIP3.

the improvements are obtained only at the cost of additional power consumption of 0.8 mW due to the hybrid balun. The designed receiver is laid out in 0.18 μm CMOS technology, whose layout is shown in Fig. 12. The area is 1.05 x 1.2 mm^2.

IV. CONCLUSIONS

The proposed circuit model of the five-port transformer balun is much more compact than but as accurate as the conventional one so that it provides much faster convergence time and more reasonable parameter values. We designed three receivers employing a passive balun, a hybrid balun and an ideal lossless balun. Gain and noise figure

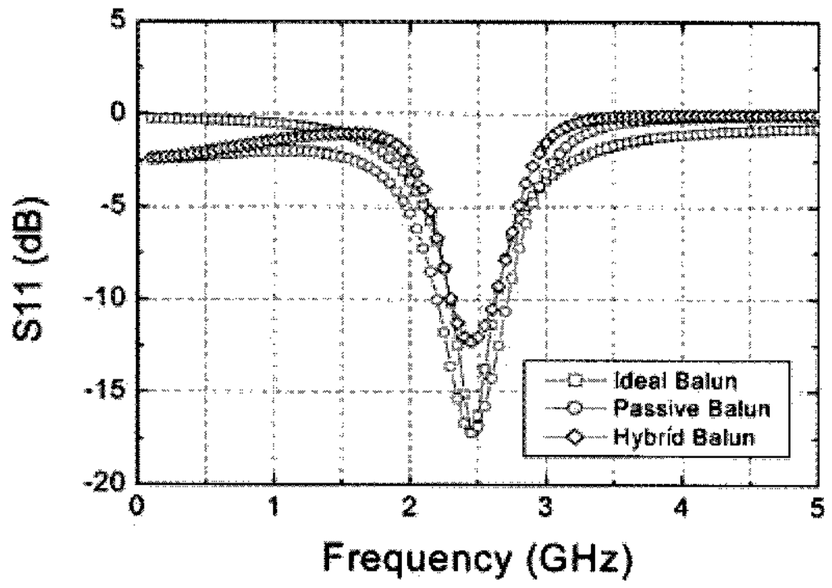


Fig. 11. Performance comparisons of three receivers with the hybrid balun, the passive balun, and the ideal balun. (a) Input matching. (b) Gain and noise figure. (c) IIP3.

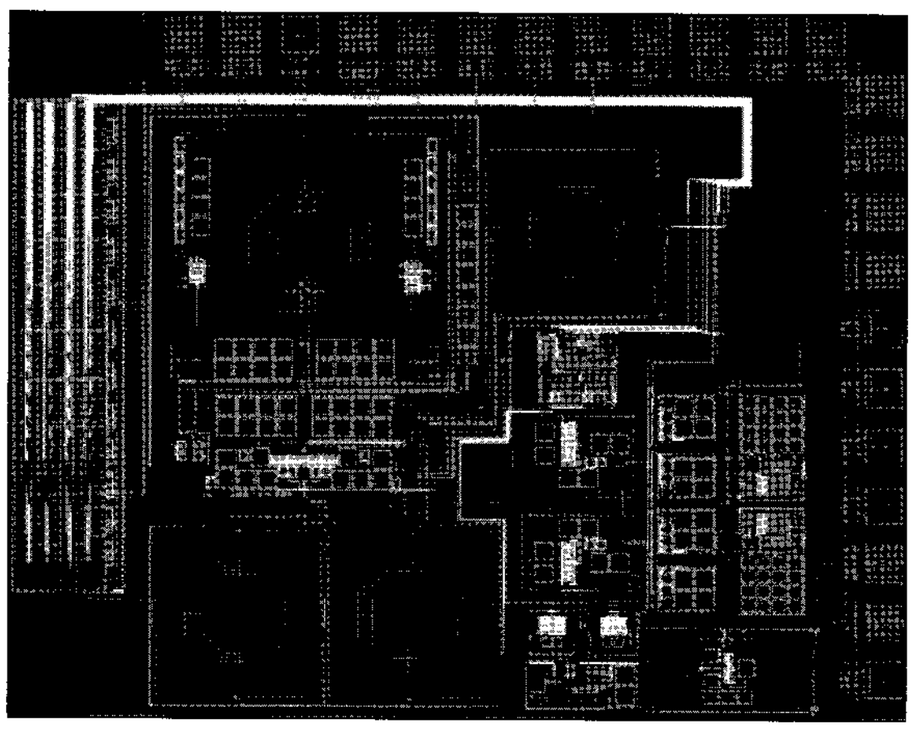


Fig. 12. Chip layout.

Table 2. Performance summary of three receivers with the ideal, passive and hybrid baluns.

	Ideal Balun Rx	**Passive Balun Rx**	**Hybrid Balun Rx**
Frequency of operation [GHz]	2.45	2.45	2.45
Conversion gain [dB]	33.3	30.5	33.2
Noise figure [dB]	4.27	6.8	5.0
1/f noise corner freq. [kHz]	Below 20	Below 20	Below 20
IIP3 [dBm]	-17.5	-15.1	-17.7
Power consumption [mW]	9	9	9.8

of the receiver with the hybrid balun is improved by 2.7 dB and 1.8 dB, respectively, compared to the receiver with the passive balun. The results prove that the proposed transformer balun and the novel hybrid balun circuit are instrumental in fully differential receiver designs.

ACKNOWLEDGMENTS

This work has been supported by in part by University ITRC Program (IITA-2008-C1090-0801-0038) and the Research Grant of Kwangwoon University in 2008.

REFERENCES

[1] H. Shin and J. Park, "A 2.4-GHz 0.82-mW Hybrid Balun for Low-Power Fully-Differential Direct Conversion Receiver in 0.18 um CMOS," *IEEE RFIC Symposium*, pp.617-620, Jun. 2007.

[2] J. Shin, J. Kim, S. Kim, and H. Shin, "A Delta-Sigma Fractional-N Frequency Synthesizer for Quad-Band Multi-Standard Mobile Broadcasting Tuners in 0.18 μm CMOS," *Journal of Semiconductor Technology and Science*, vol. 7, no. 4, pp.267-273, 2007.

[3] A. M. Niknejad and G. Meyer, "Analysis, Design, and Optimization of Spiral Inductors and Transformers for Si RF IC," *IEEE Journal of Solid-State Circuits*, vol.33, no.10, pp.1470-1481, Oct. 1998.

[4] J. R. Long, "Monolithic Transformers for Silicon RF IC Design," *IEEE Journal of Solid-State Circuits*, vol.35, no.9, pp.1368-1382, Sep. 2000.

[5] M. Valla, C. Montagna, R. Castello, R. Tonietto, and I. Bietti, "A 72 mW CMOS 802.11a Direct Conversion Receiver Front-End With 3.5-dB NF and 200-kHz 1/f Noise Corner," *IEEE Journal of Solid-State Circuit*, vol.40, no.4, pp.970-977, Apr.2005.

[6] T. Nguyen, N. Oh, V. Le, and S. Lee, "A Low-Power CMOS Direct Conversion Receiver With 3-dB NF and 30-kHz Flicker-Noise Corner for 951-MHz Band IEEE 802.15.4 Zigbee Standard," *IEEE MTT*, pp. 735-741, Feb. 2006.

Shinil Chang received B.S. degree in the department of radio science and engineering of Kwangwoon University, Seoul, Korea, in 2006. He is currently working toward M. S. degree at the same university. His research interests are CMOS RF receiver design and transformer modeling.

Jubong Park received B.S. degree in electronic engineering and avionics from Korea Aerospace University in 2001 and M.S. degree in the department of radio science and engineering of Kwangwoon University, Seoul, Korea in 2007. He had worked at Microline, Korea from April 2001 to March 2005 and at EZ Digital, Korea from March to July 2005. He is currently with Phychips, Daejon, Korea as Senior Research Engineer. His research interests are CMOS RF/Analog receiver and VCO design.

Kwang-Ho Won received B.S. degree form Dankook University in 1989, and M.S. degree in electronic and electrical engineering from Chungang University in 2003, and is currently working toward Ph. D. degree in Electronic and Communication engineering at Kwangwoon University, Seoul, Korea. From 1991 to 1997, he was with Hyundai Electronics as a Assistant Senior RF/Analog Design Engineer, where he was involved in the Tuner, Channel Decoder development for Satellite (DVB-S) and Terrestrial HDTV (8-VSB) Receiver. In April 1997, he joined the Ubiquitous Computing Research Center at Korea Electronics Technology Institute, Korea, where he was involved in the development of Wireless Communication System (Bluetooth/WLAN), Digital Satellite (DVB-S) and Digital Terrestrial (8-VSB) Receiver. His current research is focused on the RF/Analog Integrated Circuits, Baseband Modem/MAC Processor and WPAN (Wireless Personal Area Network) Systems at his Ubiquitous Computing and Network Research Team (UCN).

Hyunchol Shin received B.S., M.S. and Ph.D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejon, Korea, in 1991, 1993 and 1998, respectively. In 1997, he worked at Daimler Benz Research Center, Ulm, Germany as a doctoral research student. From 1998 to 2000, he was with Samsung Electronics as a Senior RF/Analog IC Design Engineer, where he was involved in the RF/IF chipset development for CDMA/AMPS mobile handsets. From 2000 to 2002, he was with the Electrical Engineering Department of the University of California, Los Angeles as a Postdoctoral Research Associate, where he had worked on RF transceiver design using CMOS and SiGe BiCMOS. He also served as a Lecturer at UCLA teaching Analog Electronic Circuits for undergraduate students. In May 2002, he joined Qualcomm RF/Analog IC design group as a Senior Engineer, where he had been involved in the development of multi-band multi-mode GSM/WCDMA transceivers. Since September 2003, he has been with the department of Radio Science and Engineering, Kwangwoon University, Seoul, Korea, where he is currently an Associate Professor. His research interests are RF/Analog/ Microwave Integrated Circuits and Systems. Dr. Shin has served on the technical program committee of IEEE Asian Solid-State Circuit Conference since 2007 and Korean Conference on Semiconductor since 2005.