

Reliability Evaluation of RF Power Amplifier for Wireless Transmitter

Jin Ho Choi, Member, KIMICS

Abstract—A class-E RF(Radio Frequency) power amplifier for wireless application is designed using standard CMOS technology. To drive the class-E power amplifier, a class-F RF power amplifier is used and the reliability characteristics are studied with a class-E load network. The reliability characteristic is improved when a finite-DC feed inductor is used instead of an RF choke with the load. After one year of operating, when the load is an RF choke the output current and voltage of the power amplifier decrease about 17% compared to initial values. But when the load is a finite DC-feed inductor the output current and voltage decrease 9.7%. The S-parameter such as input reflection coefficient(S11) and the forward transmission scattering parameter(S21) is simulated with the stress time. In a finite DC-feed inductor the characteristics of S-parameter are changed slightly compared to an RF-choke inductor. From the simulation results, the class-E power amplifier with a finite DC-feed inductor shows superior reliability characteristics compared to power amplifier using an RF choke.

Index Terms—RF power amplifier, class-E, class-F, reliability, stress time.

I. INTRODUCTION

The main requirements for RF power amplifier used in wireless communication are low power consumption, high power efficiency and high output power. In recent, much study has focused on one-chip RF circuit design [1, 2]. Mainly GaAs (Gallium Arsenide) has been used to implement RF circuits because of high operating speed. But it is difficult to implement one-chip RF circuit using GaAs technology. CMOS technology has been a suitable candidate to implement RF circuit with the improving CMOS process technology [3, 4, 5, 6]. And deep submicron CMOS technology offers lower cost and higher integration capability than GaAs technology. However, the HC (Hot Carrier) stress and FN (Fowler-Nordheim) stress are a critical problem in deep submicron CMOS circuit. The performance of CMOS circuit can be degraded points of the transconductance

characteristics, threshold voltage and mobility shift.

In this paper, a class-E RF power amplifier is designed using 0.25 μm standard CMOS technology. The reliability characteristics of a class-E power amplifier report with a load network.

II. CLASS-E POWER AMPLIFIER DESIGN

Fig. 1 shows the schematic of class-E power amplifier. In the class-E power amplifier, the important issue is the input waveform by the driver stage to turn the MOS M2 on and off. Ideally, a square waveform should be applied to the M2 to reduce transition times. The best solution to generate a square wave is by using a class F power amplifier with driving circuit [7]. The class-F power amplifier is realized by the transistor M1 and LC tanks (L_{O1} , C_{O1} and L_{O3} , C_{O3}) which resonates at the first and third harmonics of the carrier frequency. The finger number of transistor M1 is 300 and the width and length are 0.25 μm and 0.25 μm , respectively. The class-E power amplifier consists of MOS M2 and LC tank(L_E , C_E). The finger number of transistor M2 is 400 and the width and length are 0.25 μm and 0.25 μm , respectively.

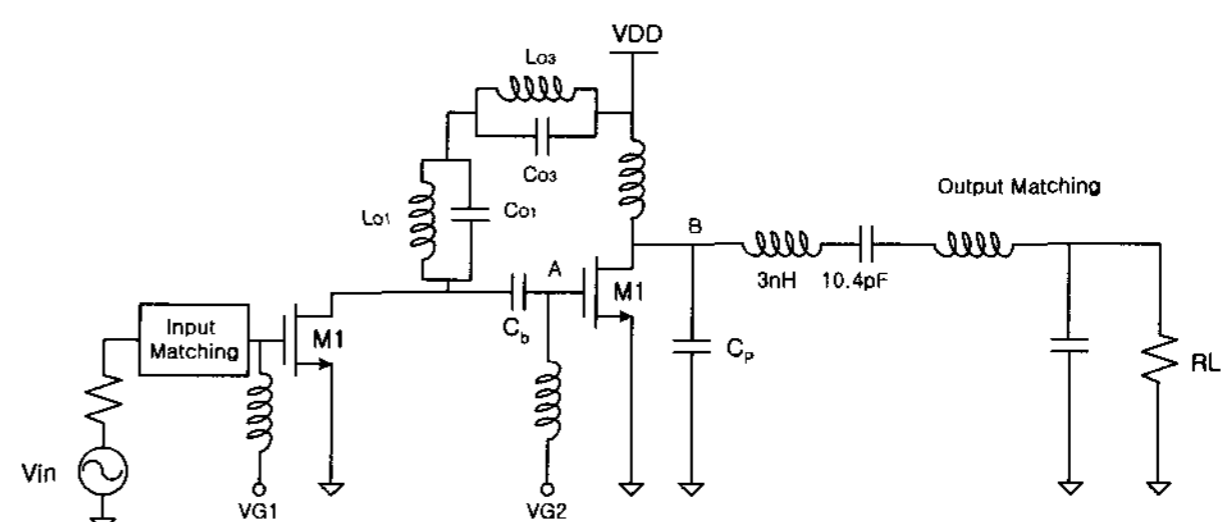


Fig.1 Schematic of class-E power amplifier

In the class-E power amplifier MOS M2 operates as a switch and this operation leads to high voltage stress because the drain voltage of the class-E power amplifier is approximately 3.6 times the supply voltage. In the class-E power amplifier the drain voltage of MOS M2 can be reduced with the load network. The drain voltage is 2.5 times the supply voltage when a finite DC-feed inductor is used instead of a RF choke inductor [8].

Fig. 2 shows the simulated gate voltage(node A) and drain voltage(node B) waveforms when the supply voltage is 1.8volts. When the RF choke, 1mH, is used as the load inductor the drain voltage of MOS M2 is about 6.5volt. However when a finite DC-feed inductor, 1nH, is used the drain voltage of MOS M2 is about 4.5volt.

Manuscript received February 15, 2008; revised May 10, 2008. Jin Ho Choi is with the Dept. of Computer Engineering, Pusan University of Foreign Studies (Tel: +82-51-640-3194, Email: jhchoi@pufs.ac.kr) Ji Hong Kim is with the Dept. of Visual Information Engineering, Donggeui University, (Tel: +82-51-890-2267, Email: arim@deu.ac.kr)

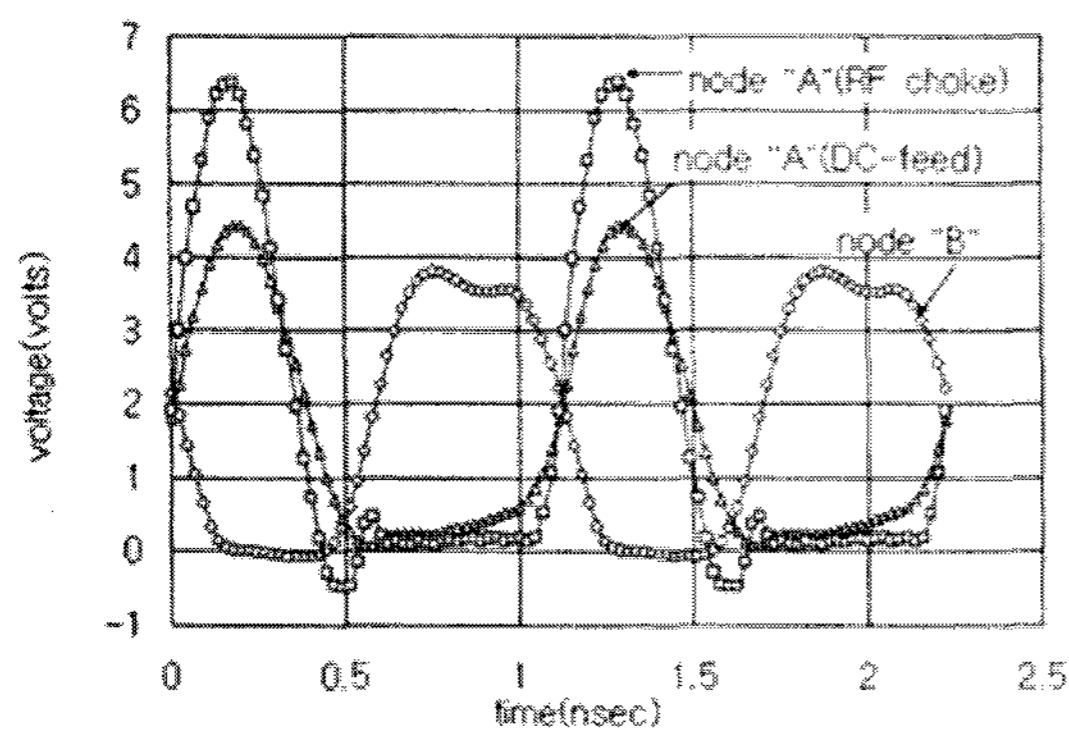


Fig. 2 Gate and drain voltages in RF power amplifier

III. CIRCUIT SIMULATION WITH STRESS TIME

The electrical characteristic of MOS M2 is degraded due to a high drain voltage with operation time. Recently, a degradation subcircuit model is described after HC stress and FN stress as a function of substrate current and operation time [9, 10]. The subcircuit model describing device characteristics changes due to HC stress and FN stress.

The stress condition is that V_{GS} is 1.8V and $I_{sub}/(W/L)$ is 1nA and 0.35nA, respectively. When the drain voltage, V_{DS} , is 6.5V $I_{sub}/(W/L)$ is 1nA and when V_{DS} is 4.5V $I_{sub}/(W/L)$ is 0.35nA [11]. Fig. 3 shows the drain current change of MOS M2 with the stress time. The used model is Wei-Cheng Lin's degradation subcircuit model to analysis MOS characteristics with the stress time. As shown in Fig. 3 when the substrate current, $I_{sub}/(W/L)$, is 1nA the drain current reduces about 49% after one year. But when the substrate current, $I_{sub}/(W/L)$, is 0.35nA the change of drain current is about 17%.

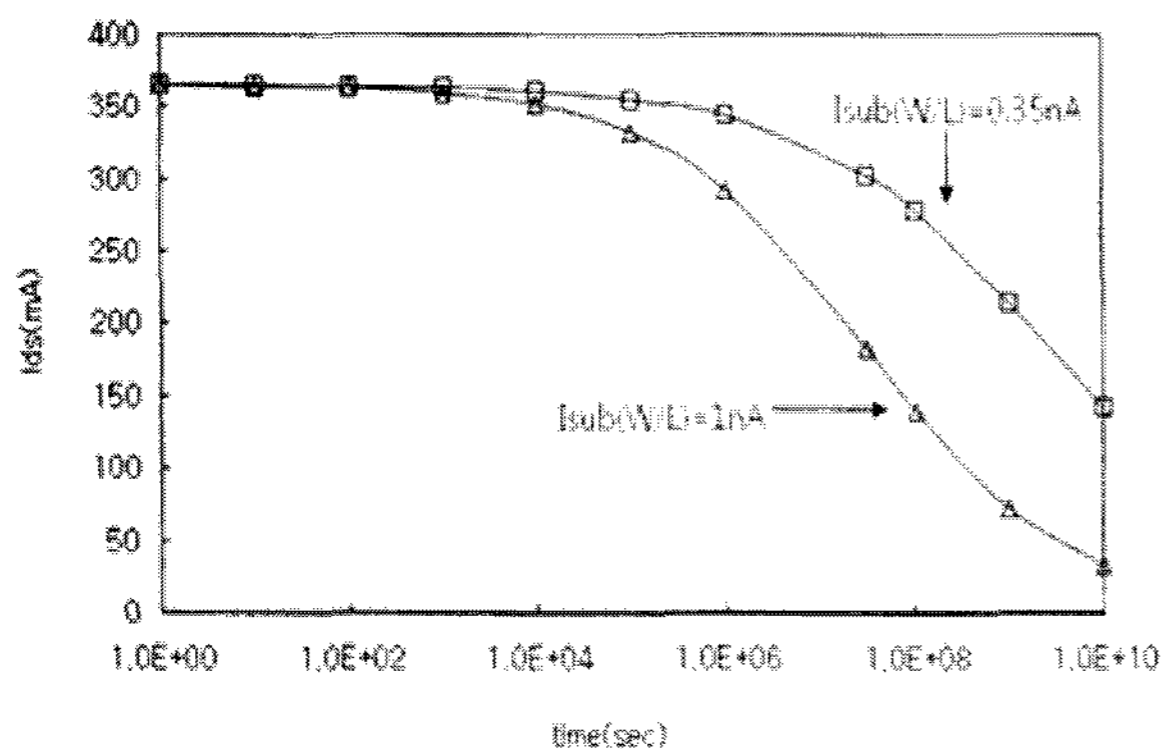
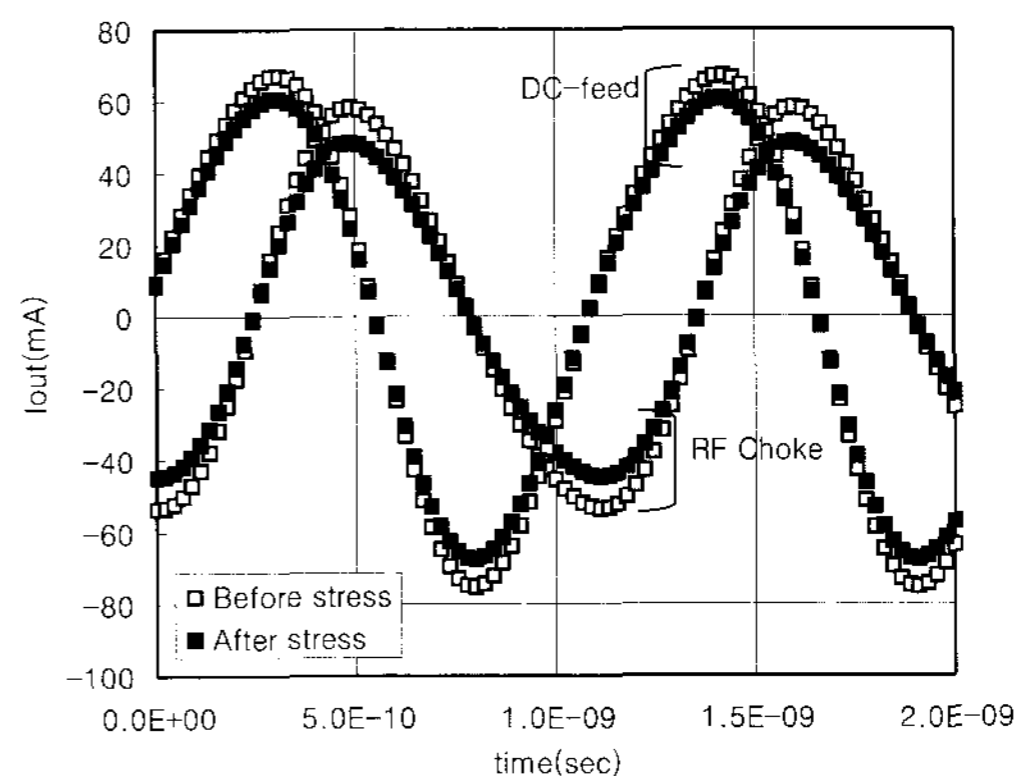
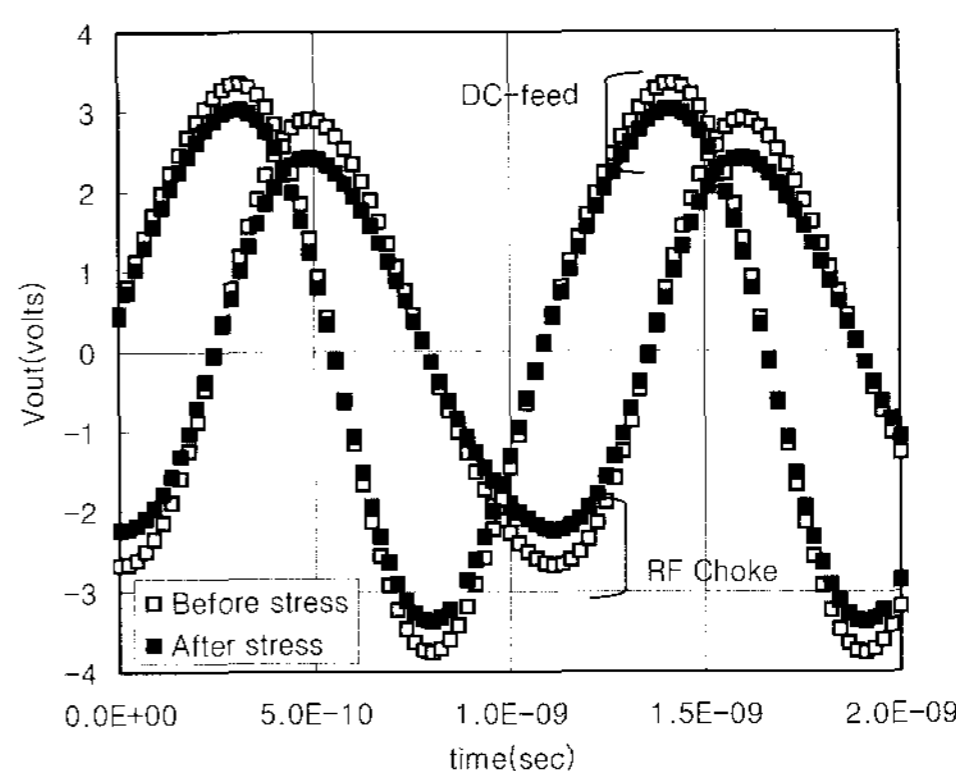


Fig. 3 Drain current change with stress time

Fig. 4 (a) and (b) show the output current (I_{out}) and the output voltage (V_{out}) waveforms before and after stress. In case of an RF choke I_{out} and V_{out} decrease about 17% compared to initial I_{out} and V_{out} . But I_{out} and V_{out} decrease only 9.7% when the load is a finite DC-feed inductor.



(a)



(b)

Fig. 4 Output current and voltage waveforms after stress time (a) Output current (b) output voltage

Fig. 5 and Fig. 6 show the effect of the stress on the input reflection coefficient (S_{11}) and the forward transmission scattering parameter (S_{21}). From Fig.5 and Fig.6 the S_{11} is changed significantly, while the S_{21} only decreases slightly. In an RF-choke S_{11} parameter is changed more significant than a finite DC-feed inductor due to high drain voltage [12]. There is no movement of the minimum S_{11} .

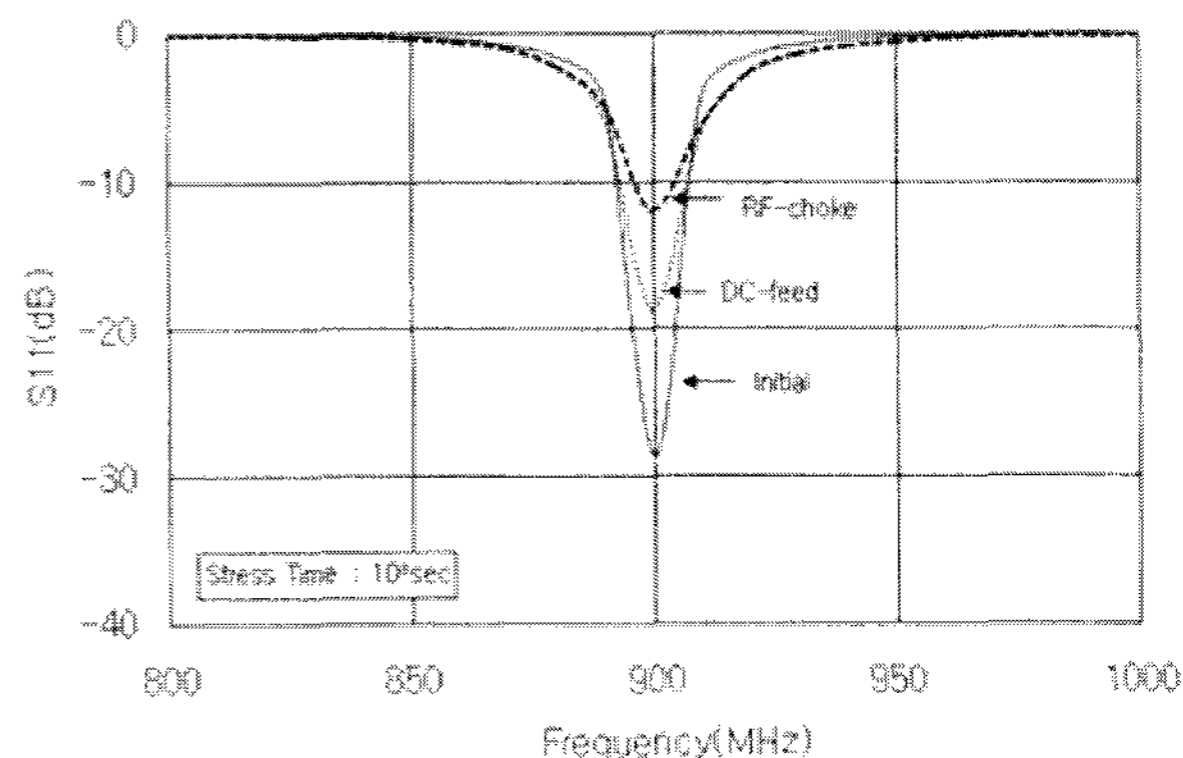


Fig. 5 S_{11} versus frequency before and after stress

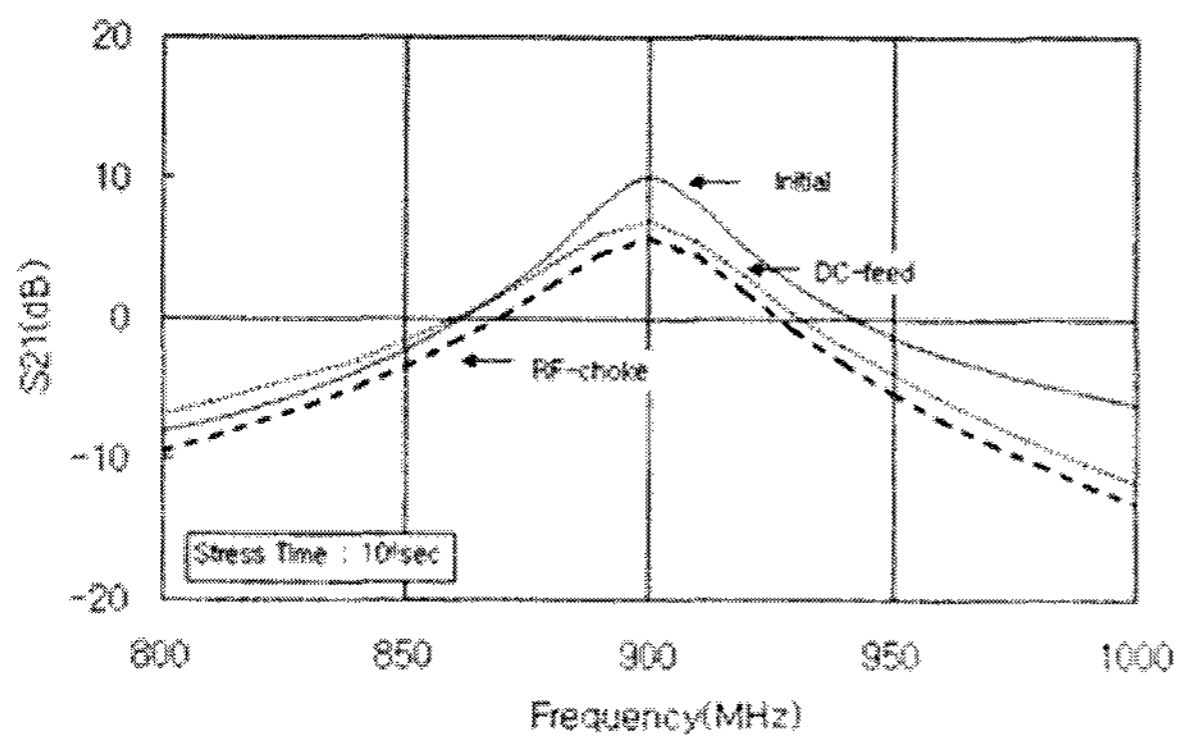


Fig. 6 S21 versus frequency before and after stress

Fig. 7 and Fig. 8 show the change of PAE and the output power with stress time. After one year, the PAE decreases about 12% in the power amplifier with an RF choke. However, the PAE decreases 6.5% in case of a finite DC-feed. The output power decreases about 28.6% in the power amplifier with an RF choke and the output power decreases 18.7% in case of a finite DC-feed.

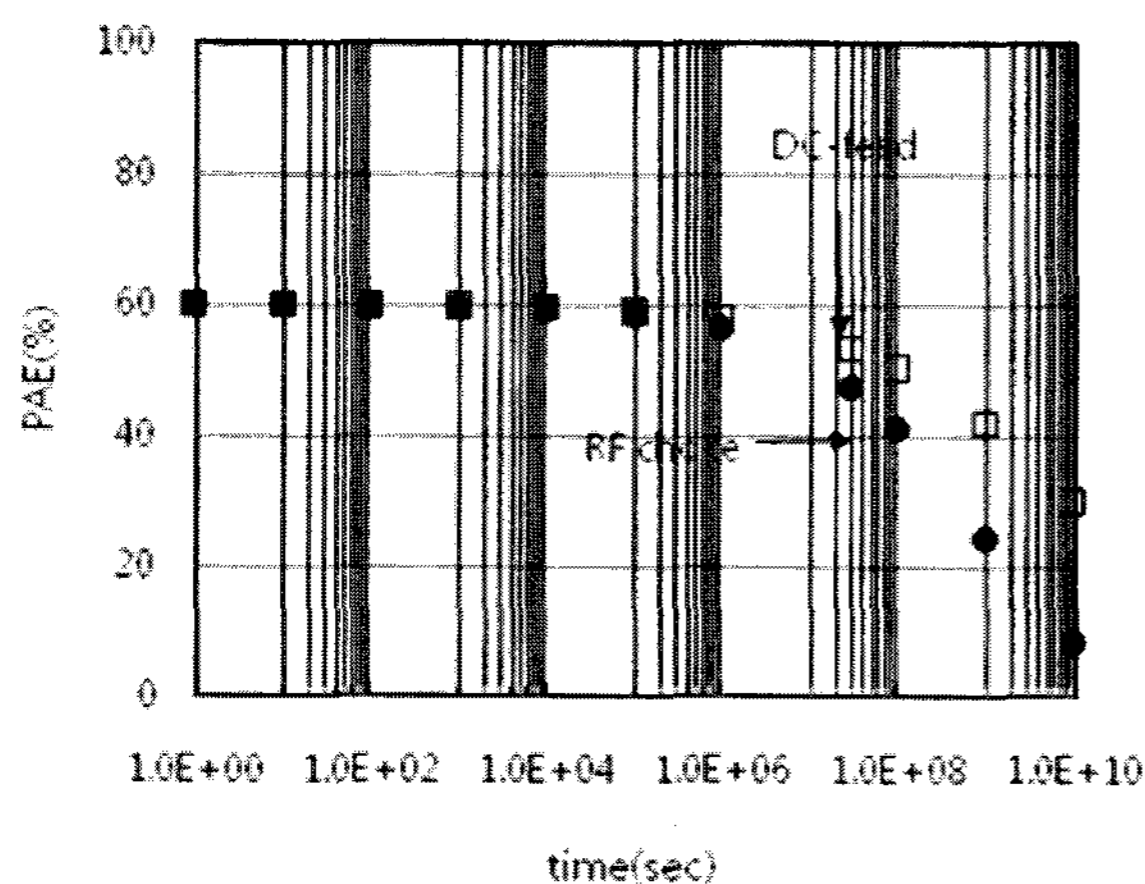


Fig. 7 PAE change with stress time

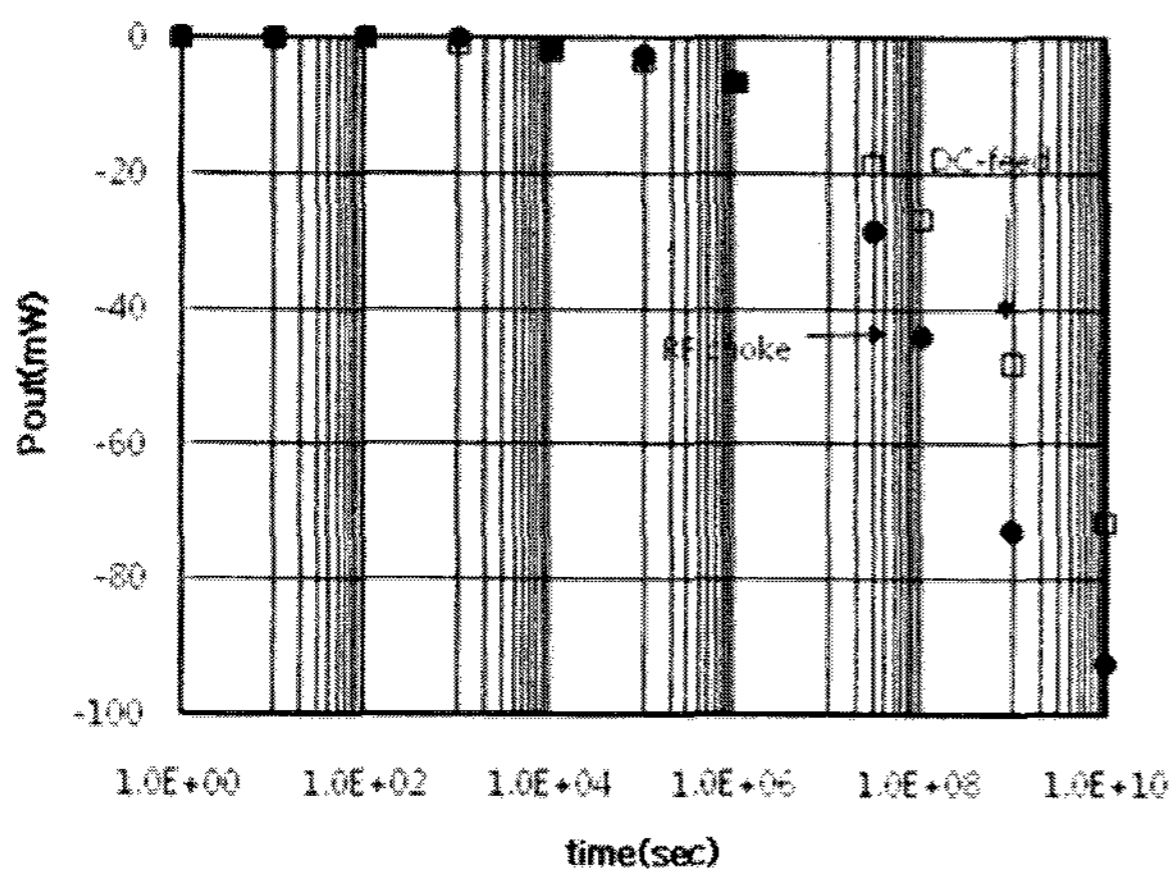


Fig. 8 Output Power change with stress time

The simulated results show the class-E power amplifier with a finite DC-feed inductor exhibits superior reliability characteristics.

IV. CONCLUSIONS

A reliability characteristic of a class-E power amplifier was studied with the load network. A class-E RF power amplifier with 1.8volts power supply is designed using 0.25 μ m standard CMOS technology at 900MHz. After HC stressing, the performance degradation of power amplifier using an RF choke was more serious than a finite DC-feed amplifier. Also the class-E amplifier with finite DC-feed inductance provides high efficiency and high output power compared to RF choke amplifier. The simulated results show that the class-E power amplifier with a finite DC-feed inductor has superior reliability characteristics.

REFERENCES

- [1] A. A. Abidi, RF CMOS comes of age," IEEE VLSI Circuits Dig., no. 6, pp. 113-116, Jun 2003.
- [2] E. Morifuji, H. S. Momose, T. Ohguro, T. Yoshitomi, H. Kimijima, F. Matsuoka, M. Kinugawa, Y. Katsumata and H. Iwai, "Future perspective and scaling down Roadmap for RF CMOS," Symposium on VLSI Circuits Digest of Technical Papers, pp. 165-166, 1999.
- [3] P. J. Sullivan, B. A. Xavier and W. H. Ku, "Low Voltage Performance of a Microwave CMOS Gilbert Cell Mixer," IEEE J. Solid-State Circuits, vol. 32, pp. 1151-1155, 1997
- [4] R. A. Rafla and M. N. Gamal, "Design of a 1.5V CMOS Integrated 3GHz LNA," in proceeding ISCAS, pp. 440-443, 1999.
- [5] Steve Hung-Lung Tu and Fu Jen, "Class E RF Tuned Power Amplifiers in CMOS Technologies : Theory and Circuit Design Considerations," IEDEE Radio Communications, pp. S6-S11, September 2004.
- [6] King-Chun Tsai and Paul R. Gray, "A 1.9GHz, 1W CMOS Class-E Power Amplifier for Wireless Communications," IEEE Journal of Solid-State Circuits, vol. 34, no. 7, pp. 962-970, July 1999.
- [7] Chris Trask, "Class-F Amplifier Loading Networks : A Unified Design Approach," IEEE MTT-S Digest, pp. 351-354, 1999.
- [8] C. Yoo and Q. Huang, "A Common-Gate Switched 0.9W Class-E Power Amplifier with 41% PAE in 0.25 μ m CMOS," IEEE. Journal of Solid-State Circuits, vol. 36, pp. 823-830, May 2001.
- [9] E. Xiao, J. S. Yuan and H. Yang, "CMOS RF and DC reliability subject to hot carrier stress and oxide soft breakdown," IEEE Trans. Device Mater. Rel., vol. 4, no. 3, pp. 92-98, Mar. 2004.
- [10] W. C. Lin, T. C. Wu, Y. H. Tsai, L. J. Du and Y. C. King, "Reliability evaluation of class-E and class-A Power Amplifiers with nanoscaled CMOS Technology," IEEE Trans. on Electron Devices, vol. 52, no. 7, July 2005.
- [11] J. E. Chung, M. C. Jeng, J. E. Moon, P. K. Ko and C. Hu, "Low-voltage Hot-electron currents and degradation in deep submicronmeter MOSFETs,"

IEEE Trans. on Electron Devices, vol. 37, no. 7, pp. 1651-1657, July 1990.

- [12] Qiang Li, Jinlong Zhang, Wei Li, Jiann S. Yuan, Yuan Chen and Anthony S. Oates, "RF Circuit Performance Degradation Due to Soft Breakdown and Hot-Carrier Effect in Deep-Submicrometer CMOS Technology," IEEE Trans. on Microwave and Techniques, vol. 49, no. 9, pp. 1546-1551, September 2001.



Jin Ho Choi

received the B.S. degree in electronics from Busan University in 1985, and the M.S. degree in electronics from KAIST in 1987. He received the Ph. D. degree in electronics from KAIST in 1992. From 1992 to 1996, he was a researcher at Hynix Semiconductor Inc.. Since 1996, he has been a professor in Dept. of Computer Engineering, Pusan University of Foreign Studies. His research interest includes VLSI design.