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# 코드 기반 기법을 이용한 디지털 회로의 스캔 테스트 데이터와 전력단축

# ( Reduction of Test Data and Power in Scan Testing for Digital Circuits using the Code-based Technique )

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요 약

디지털 논리회로의 테스트 데이터와 전력소비를 단축시킬 수 있는 효율적인 테스트 방법을 제안한다. 제안 하는 테스트 방법은 테스트장비내의 테스트 데이터 저장 공간을 줄이는 하이브리드 run-length 인코딩 방법에 기초하고, 수정된 Bus-invert 코딩 방법과 스캔 셀 설계를 제안하여, 스캔 동작시의 개선된 전력 단축효과를 가져온다. ISCAS'89 벤치마크 회로의 실험결과 고장 검출율의 저하 없이 평균 전력은 96.7%, 피크전력은 84%의 단축을 보이며 테스트 데이터는 기존 방법보다 78.2%의 압축을 갖는다.

Abstract

We propose efficient scan testing method capable of reducing the test data and power dissipation for digital logic circuits. The proposed testing method is based on a hybrid run-length encoding which reduces test data storage on the tester. We also introduce modified Bus-invert coding method and scan cell design in scan cell reordering, thus providing increased power saving in scan in operation. Experimental results for ISCAS'89 benchmark circuits show that average power of 96.7% and peak power of 84% are reduced on the average without fault coverage degrading. We have obtained a high reduction of 78.2% on the test data compared the existing compression methods.

**Keywords :** low power, scan testing, Bus- invert coding, Run-length code, compression

## I. Introduction

Recently, it becomes more important to reduce power dissipation for portable electronic products like the cell phone, PDA, and laptop, etc. Integrated chip (IC) is one of critical components in modern electronic devices. Most of electronic devices' require more IC for improving their performance and more functionality can be integrated into a single IC than ever as the technology is being developed. Furthermore, heterogeneous components are now inserted into a single IC, which is generally called System-On-a-Chip (SOC). The complex design methodology like a SOC and high-density circuits make the testing of these devices harder. More testing time and power consumption are increasing. Therefore, the excessive consumption more than its power limit severely damages the devices including it during testing mode. In VLSI testing area, various low power testing methods have been proposed in literature.[1~7]

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Another big issue in testing is reduction of test data and test time. It is important to reduce the test data volume requirement in the tester which connects to the SOC and tests the SOC. SOCs are used widely in modern VLSI design flows, however, ATE (Automated Test Equipment) has limited ability to test SOCs since it has low data bandwidth to communicate with the device-under-test (DUT) as well as limited memory. Testing an SOC in the ATE environment depends on how much test data needs to be transferred to the SOC and how fast test data in the tester can be supplied to the core.

Scan based design prevails as it enhances both controllability and observability with a limited number of input and output pins. However, in large circuits (or SOC) that necessitate long scan-based architecture, scan based design is confronted with the problem of highly increased testing time and memory requirement. When more IP(Intelligent Property) should be tested, test time turns out to be a big burden since more test data are needed. So, the complex design methodology like a SOC and high-density circuits make the testing of these devices harder.

Test data compression techniques aim at reducing the number of bits needed to be stored and shifted per test vector in ATE, thus achieving a reduction in test data size and time.

A well-known approach is to use traditional run-length encoding and statistical Huffman encoding methods. The test data compression techniques based on run-length encoding include Golomb coding[8] and FDR coding[9] while test data compression using statistical coding includes Huffman coding[10]. Recently, Golomb and FDR coding methods produce good results for compression of test data. For test cubes with the frequency of runs of length less than 24, Golomb coding is more effective than FDR coding for test data compression assuming uniform distribution of frequencies.

The FDR code method gives better compression than the Golomb coding method if data has runs of 24 or more 0's (or 1's) or runs of 1(or 0's) or less 0's (or 1's). However, this is only if the frequencies of runs of 0's (or 1's) are equally distributed. However, in real test data, we find that the frequency of shorter runs of 0's (or 1's) is higher than those of very long ones. Therefore, in addition to a heuristic scheme for mapping 0's and 1's to don't care values in test cubes, we select the codewords carefully in order to bring about considerable reduction in the test data volume on the tester.

This paper investigates the selection of a proper set of codewords suitable to obtain better compression of test cubes. In order to do so, we apply a mapping scheme suitable for 0's runs and 1's runs in test cubes in such a way as to have the minimum transition number between adjacent scan cells using the modified Bus-invert coding. This leads to a significant reduction in test data volume and scan power dissipation for various benchmark circuits.

## II. Proposed Low Power Scan Testing Scheme

In CMOS circuits, power dissipation occurs when the internal node in the circuits undergoes the switching activity, 1 to 0 or 0 to 1. The model to calculate the power consumption in CMOS circuits based on the switching activity is as follows.

$$P_d = 0.5 V_{dd}^2 f_{clk} C_{load} A_{sw} \quad (1)$$

where $V_{dd}$is the power supply voltage, $f_{clk}$ is the clock frequency, $C_{load}$ is the capacitance of load, and $A_{sw}$is the switching activity. The calculation based on this expression is one of the good approximations of the power dissipation of circuits. However, the measurement based on the switching activity in the circuit under test is known to be a time-consuming process. Hence, in this work, the weighted transition metric($WTM_i$ $:\Sigma 1<j<m$ $(m-j)(b_{i,j} \oplus b_{i,j+1})$ for $i^{th}$ input test vector, m: the number of scan cell in a scan chain, $b_{i,1}$: the first bit scanned into the scan chain) in [4] is used to compute the power

consumption due the shifting operation of scan vector. This model is approximately accurate to estimate the switching activity in the internal nodes of the circuits during scanning-in since scan vector is reasonably weighted depending on its bit's position in it and the length of scan path. The average scan in power *SPavg* and *SPpeak* scan in power are estimated as follows: $SPavg = \Sigma 1<i<n\ WTM_i / n$, $SPpeak = MAX\ 1<i<n\ \{WTM_i\}$, where $n$ is the number of test patterns.

Bus-invert encoding techniques[11] are used to reduce the power consumption by changing the original data to a form which has less transition activity. A well-known bus invert coding approach is to compute hamming distance between the present bus value and the next data value. If its value is larger than n/2, the next data value is inverted (where n means bit size of the bus). Therefore, average and peak power dissipation for I/O can be decreased due to reduced the number of transitions of data on the bus. In general, data bus activity is characteristic of random uniformly distributed sequence of values and time-dependent Markovian code. However, in the case of considering deterministic test data, it becomes time-independent and non-uniformly distributed sequence of values. In other words, it is possible to reorder the test data by the column an row. Furthermore, it is easy to reduce the No. of transition of data between adjacent scan cells since there are many number of unspecified value in deterministic test data, that is, only about 23% is specified (0 or 1) in uncompacted test patterns for all benchmark circuits through our experiments. As the above result, we can efficiently reduce power dissipation if Bus-invert coding technique is used to reorder the deterministic test data.

## 1. COMPUTE HAMMING DISTANCE USING MODIFIED BUS-INVERT CODING

We define the Hamming distance between binary datawords c1 and c2, denoted by d(c1, c2) to be the minimum number of bits that must be inverted to go from one word to the other.(where dataword is the column of the deterministic test data obtained, that is, corresponding columns are scan cell of circuit under test). We can apply the modified Bus-invert coding algorithm to deterministic test data to reduce the transition between neighboring scan cells and search the next column of test data such that its transition(Hamming distance) can be minimum, instead of searching the next column with Hamming distance larger than n/2.(where n means the No. of test pattern) The don't care value(x) of test data is assigned as the same value of the compared data. An example illustrating how our proposed low power scan testing is given below. We assume that 34 test data is obtained by ATPG tool. In Fig.1, $S_i$ means the $i^{th}$ scan cell, $T_i$ means the $i^{th}$ test pattern, H and *inv_v* mean Hamming distance and inverting vector, respectively. W means the number of scan in transition by $(WTM^{j}_{in} = (b_{i-1} \oplus b_i) \times (n-i)$, for $j^{th}$ input test vector, $i=1:n-1$, $n$: the number of scan cell in a scan chain, $b$: scan cell) In Fig. 1 (b), the value of inverting vector corresponding to each scan cell becomes 0100($S_1S_4S_2S_3$). The original value of $S_4$ is 111, but retains 000 while shifting and then is applied after inverting. Scan/invert signal in Fig.2 is controlled by the inverting vector's value. The number of scan in transition of reordered test data is reduced from 6 to 3(don'care value mapped to $T_2 \rightarrow 1$ and $T_3 \rightarrow 0$).

In Fig.2 pseudo code for reordering the scan cells

|  | $S_1$ | $S_2$ | $S_3$ | $S_4$ | W |
|---|---|---|---|---|---|
| $T_1$ | 0 | 0 | 1 | 1 | 2 |
| $T_2$ | 0 | 1 | X | 1 | 3 |
| $T_3$ | 0 | X | 0 | 1 | 1 |
| H | 1 1 1 | | | | |
| *inv_v* | 0 | 0 | 0 | 0 | |

(a) original

|  | $S_1$ | $S_4$ | $S_2$ | $S_3$ | W |
|---|---|---|---|---|---|
| $T_1$ | 0 | 0 | 0 | 1 | 1 |
| $T_2$ | 0 | 0 | 1 | 1 | 2 |
| $T_3$ | 0 | 0 | 0 | 0 | 0 |
| H | 0 1 1 | | | | |
| *inv_v* | 0 | 1 | 0 | 0 | |

(b) reordered

그림 1. 스캔 셀 정렬의 예
Fig. 1. An example of scan cell reordering.

```
Test data[N][m](N: No. of test cube, m: No.of scan cell)
Generating complementary vector for test data // → c_data[N][m]
// that is, 0 replaced with 1 and vice versa, x(don't care values are unchanged)
Initialization invert vector(inv_v[m])
for(i=0; i<=m-1; i++)
{       for(j=i+1;j<threshold; j++)
    {       for(k=0;k<N;k++)
                    Compute H_D( );
// Hamming Distance between test data[k][i] and test data[k][j]
for(k=0;k<N;k++)
                Compute H_D( );
//Hamming Distance between test data[k][i] and c_data[k][j]
}
Generate reordered test data( ) and
invert vector( );
// test data is organized the column with lower Hamming Distance value
// inv_v[m] = 1 if c_data[][] is selected.
Mapping routine( );
// x value is assigned specified value 1 or 0
}
```

그림 2. 스캔 셀 재정렬 의사 코드
Fig. 2. Pseudo code for scan cell reordering.

and generating the invert vector is represented.

### 2. PROPOSED SCAN CELL FOR LOW POWER TESTING

The scan cell for low power scan testing is proposed. The proposed scan cell is as follows.

For the test stimulus to be inverted, a multiplexer with scan/invert control is inserted on the invert path

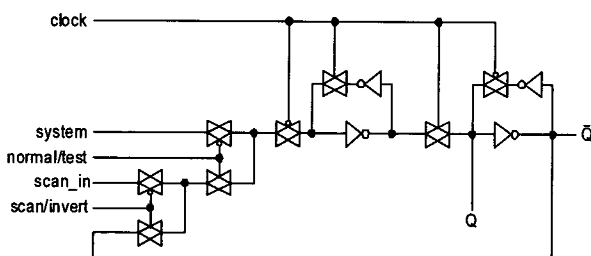


그림 3. 제안된 스캔 셀
Fig. 3. Proposed scan cell.

of the scan cell, whereas the other cells receive the normal stimulus intact during the input applying cycle.

In scan test mode, normal/test and scan/invert control is sensitized, test input vectors derived previous algorithm are applied into the scan cells by the scan_in signal sequentially, and then scan/invert control signals of corresponding scan cells are sensitized. Because of sensitized control signal, test data is inverted and applied into the circuit under test. The responses of applied test vectors are captured and shifted out with next test pattern, simultaneously. In normal operation, the data on system is applied and captured into the scan cell, no performance deterioration whatsoever is suffered during the functional operation. For each circuit, we can choose the number of scan cell reordering based on the proximity to be used in determining the scan cells that can be placed in adjacent positions. These layout area and timing-related matters can be incorporated into the cell reordering problem. We will use the concept of "maximum distance threshold" and show the simulation results of this problem in chapter IV.

## III. Applying The Hybrid Code

The proposed codeword generation scheme is shown in Table 1. The compression method is based on run-length coding. The proposed hybrid coding is a variable-to-variable length runs of 0's(or 1's) to codewords of variable length, and each codeword is composed of a group prefix and a tail bit. In the proposed coding method, runs of 0's(or 1's) are divided into groups $G_1$, $G_2$, ⋯, $G_n$, where $n$ is determined by length index of the longest length run($2n+1 - 4 \le Rmax \le 2n+2 - 5$). Also, the size of the $i^{th}$ group is equal to 2i+1. The proposed codeword size increases by two bits as increasing the group, that is, $G_i$ to $G_{i+1}$. For example, the run-length 2($G_1$) and 10($G_2$) are encoded as 010 and 10110 respectively. As shown in the Table 1, codewords in the first group $G_1$ is same as Golomb codewords,

표 1. 제안된 하이브리드 코딩 예
Table 1. An example of proposed Hybrid coding.

| Group | Run-length | Group prefix | Tail | Codeword |
|---|---|---|---|---|
| $G_1$ | 0 | 0 | 00 | 000 |
| | 1 | | 01 | 001 |
| | 2 | | 10 | 010 |
| | 3 | | 11 | 011 |
| $G_2$ | 4 | 10 | 000 | 10000 |
| | 5 | | 001 | 10001 |
| | 6 | | 010 | 10010 |
| | 7 | | 011 | 10011 |
| | 8 | | 100 | 10100 |
| | 9 | | 101 | 10101 |
| | 10 | | 110 | 10110 |
| | 11 | | 111 | 10111 |
| $G_3$ | 12 | 110 | 0000 | 1100000 |
| | 13 | | 0001 | 1100001 |
| | ... | | ... | ... |
| | 27 | | 1111 | 1101111 |
| ... | ... | ... | ... | ... |

표 2. Golomb, FDR, 제안된 코드워드(블록크기 4)
Table 2. Golomb, FDR, and proposed codeword(block size=4).

| Run-length | Golomb codeword | FDR codeword | Proposed codeword | Size of proposed codeword |
|---|---|---|---|---|
| 0 | 000 | 00 | 000 | 3 bits |
| 1 | 001 | 01 | 001 | 3 bits |
| 2 | 010 | 1000 | 010 | 3 bits |
| 3 | 011 | 1001 | 011 | 3 bits |
| 4 | 1000 | 1010 | 10000 | 5 bits |
| 5 | 1001 | 1011 | 10001 | 5 bits |
| 6 | 1010 | 110000 | 10010 | 5 bits |
| 7 | 1011 | 110001 | 10011 | 5 bits |
| 8 | 11000 | 110010 | 10100 | 5 bits |
| 9 | 11001 | 110011 | 10101 | 5 bits |
| ... | ... | ... | ... | ... |

while codewords in the other groups are similar to FDR codewords except the tail bit size.

As shown in the Table 2, the proposed code word size is different from the other existing codes. The proposed hybrid codeword resembles Golomb codeword for runs of smaller lengths. For the run-lengths of 4 or greater, the proposed codeword is similar to FDR codeword but differs with respect to its size. Also, the tail of the proposed codeword differs by 1 bit from FDR codeword. For example, for a run-length of 9, the size of the codeword for FDR coding is 6 bits versus 5 bits for the proposed codeword. The codeword size increases as an odd number from 3. Also, unlike the FDR codeword, the bit size of the prefix is different from that of the tail for the proposed codeword. The tail is 1 bit longer than the prefix. This allocation shows remarkable results on benchmark circuits through 0's run and 1's runs respectively.

As compared to the FDR codeword, the proposed codeword size is smaller than FDR codeword size except the first and the second run-length in each group (ex. run-length 0 and 1 in $G_1$, run-length 4 and 5 in $G_2$, etc.) Therefore, this allocation incorporates the advantage of the Golomb codewords for shorter lengths of runs (0 to 23) and FDR codewords for longer length runs (24 to ~). For runs of 20, the proposed codeword size is actually smaller (7 bits) as compared with 8 bits for Golomb or FDR.

## Ⅳ. Experimental Results

First, we simulated the ISCAS'89 benchmark circuits and used the MINTEST[12] test cube in order to evaluate the efficiency of proposed power saving test scheme. Table 3 shows the number of test vector, flip-flop, and original test data size for ISCAS'89 benchmark circuits. Table 4 and 5 show that proposed method for power saving is more efficient comparing it with the other power saving methods. In tables, our proposed method is much better than the existing test methods for both the average power and peak power. In addition, proposed

표 3. ISCAS'89 회로와 결정론적인 테스트 데이터
Table 3. ISCAS'89 circuits and deterministic test data.

| circuits | #test | No. of scan cell | test data(bits) |
|---|---|---|---|
| s5378 | 111 | 214 | 23754 |
| s9234 | 159 | 247 | 39273 |
| s13207 | 236 | 700 | 165200 |
| s15850 | 126 | 611 | 76986 |
| s38417 | 99 | 1664 | 164736 |
| s38450 | 136 | 1464 | 199104 |

표 4. 평균 전력 절감 비(%)
Table 4. Reduction ratio(%) for average power saving.

| circuits | [5] | [2] | Proposed |
|---|---|---|---|
| s5378 | 78.0 | 82.9 | 93.4 |
| s9234 | 76.3 | 82.8 | 94.0 |
| s13207 | 93.7 | 95.8 | 94.8 |
| s15850 | 85.3 | 90.2 | 98.4 |
| s38417 | 81.4 | 85.7 | 98.0 |

표 5. 피크 전력 절감 비(%)
Table 5. Reduction ratio(%) for peak power saving.

| circuits | [5] | [2] | Proposed |
|---|---|---|---|
| s5378 | 29.0 | 58.6 | 73.9 |
| s9234 | 31.1 | 57.7 | 75.9 |
| s13207 | 28.0 | 73.8 | 93.4 |
| s15850 | 36.7 | 66.9 | 91.7 |
| s38417 | 40.8 | 73.5 | 93.1 |
| s38584 | 16.3 | 67.3 | 80.6 |

표 6. 레이아웃을 고려한 평균/피크 전력 단축 비(%)
Table 6. Average/peak power reduction ratio(%) considering the layout area.

| circuits | Maximum distance threshold | | | | | |
|---|---|---|---|---|---|---|
| | 0 | 0.1 | 0.25 | 0.33 | 0.5 | 1.0 |
| s5378 | 68.3/ 15.7 | 88.1/ 54.1 | 90.7/ 54.2 | 92.0/ 53.3 | 93.2/ 68.8 | 93.4/ 73.9 |
| s9234 | 78.2/ 21.6 | 87.2/ 46.2 | 91.4/ 58.8 | 92.3/ 54.4 | 94.0/ 67.2 | 94.0/ 75.9 |
| s13207 | 51.8/ 29.6 | 85.0/ 72.1 | 92.0/ 86.0 | 93.9/ 91.7 | 94.7/ 92.5 | 94.8/ 93.4 |
| s15850 | 91.5/ 47.0 | 96.0/ 70.3 | 97.4/ 81.5 | 97.7/ 84.0 | 98.3/ 89.4 | 98.4/ 91.7 |
| s38417 | 84.3/ 36.3 | 93.8/ 73.8 | 96.5/ 85.8 | 97.3/ 88.4 | 97.8/ 92.4 | 98.0/ 93.1 |
| s38584 | 85.4/ 15.8 | 93.0/ 50.5 | 95.2/ 66.9 | 95.9/ 70.0 | 96.4/ 73.8 | 96.8/ 80.6 |
| Avg. | 76.6/ 27.7 | 90.5/ 61.2 | 93.9/ 72.2 | 94.9/ 73.6 | 95.7/ 80.7 | 95.9/ 84.8 |

test methods can be used for any other run-length test compression methods to reduce the test data compression as well as power consumption in scan testing.

In Table 6, simulation results based the maximum distance threshold concept mentioned above(chapter II.2) are showed. In case of no reordering, maximum distance threshold represents 0(2nd column of Table 6). Only inverting operation to the corresponding columns of test data is performed in shifting the data. When maximum distance threshold value is 1.0, scan cell reordering is performed free without constraints of layout. That is, each scan cell can be exchanged at any location based on proposed reordering algorithm. As an example, if we have a scan chain length with 100 and its maximum distance length with 0.1, the scan cells can be replaced within backward or forward 10 scan cells from current location. Therefore, this factor has a characteristic of trade-off threshold value that can be used by designer to specify the relative importance of area overhead and power minimization. As shown in the Table 6, the significant reduction is achieved within 0.1 value for all the circuits. Especially, when maximum threshold value is 0, just adding the invert coding scheme except reordering makes a great reduction for large circuit s15850, s38417, and s38584.

Table 7 shows the compression ratio for each code. The amount of compression obtained was computed as follows: *Compression Ratio(%) = (Test Data - Compressed Test Data)/(Test Data)*. As shown in Table 7, the proposed codeword achieved high levels of compression for every circuit compared with the existing methods. In the 5th column, 0's(1's) means that unspecified values(x) in the test cube are assigned to only 0(1) value and binary means that unspecified values can be assigned to 0 or 1 value after the third step(scan cell reordering) of section II.1. In binary mapping, more increased compression ratio is obtained by compressing both 0's run and 1's

표 7. 각 코드워드간의 압축 비(%)
Table 7. Compression ratio(%) between each codeword.

| circuits | Golomb [9] | FDR [10] | VIHC -16 [13] | Proposed | | |
|---|---|---|---|---|---|---|
| | | | | 0's | 1's | Binary |
| s5378 | 37.1 | 48.0 | 46.9 | 45.6 | 51.3 | 63.5 |
| s9234 | 45.3 | 43.6 | 46.1 | 52.5 | 45.0 | 67.0 |
| s13207 | 79.7 | 81.3 | 80.4 | 86.5 | 84.6 | 92.0 |
| s15850 | 62.8 | 66.2 | 64.1 | 71.6 | 64.9 | 83.3 |
| s38417 | 28.4 | 43.3 | 47.8 | 39.8 | 51.0 | 84.8 |
| s38584 | 57.2 | 60.9 | 59.6 | 65.5 | 63.4 | 78.4 |

run in a test pattern simultaneously. For example, if *dxxxxd*(*d* is 0 or 1) is a test cube, we allocate the value d to all x's. However, in case of *dxxxxd′* (*d′* means the complement of *d*), we have to investigate the length of runs on both sides of xxxx and allocate the value with longer length to the x.

As the result of simulation, compression by 0's mapping for 0's run achieved more compression than 1's mapping for 1's run for most of benchmark circuits. In addition, in the case of applying the scheme of binary mapping to the test cube, more compression ratio has been achieved for all the circuits. The main hardware for the proposed code word will be composed of a part for recognizing the prefix part starting from base 4 and a counter.

## V. Conclusion

In this paper new low power scan test method based on modified Bus-invert coding has been presented and remarkable power savings are obtained for all benchmark circuits. Especially, as adopt of modified Bus-invert coding scheme in column reordering of test data and an efficient scan cell design, we have obtained 96.7% and 84%saving on the average with respect to the average power and peak power, respectively. In addition, the proposed test data compression scheme had an advantage in reducing the amount of test data that needed to be stored on the tester and in reducing the testing time for transferring test data to the SOC under test through the new hybrid codeword. Also, the proposed techniques has potential applications in reducing the cost of testing for multiple scan chain architecture.

## References

[1] L. Whetsel, "Adapting scan architecture for low power operation," in *Proceedings of the International Test Conference*, pp. 863-872, Atlantic, Oct., 2000.

[2] P. Rosinger, P. T. Gonciari, B. M. Al-Hashimi, and N. Nicolici, "Simultaneous reduction in volume of test data and power dissipation for systems-on-a-chip," *IEE Electronic letters*, 37, pp. 1434-1436, 2001.

[3] Xiaodong Chen and Michael S. Hsiao, "Energy-efficient logic BIST based on state correlation analysis," in *Proceedings of VLSI Test Symposium*, pp. 267-272, Napa Valley, May, 2003.

[4] R. Sankaralingam, R. R. Oruganti and N. A. Touba, "Static compaction techniques to control scan vector power dissipation," in *Proceedings of VLSI Test Symposium*, pp. 35-40, Montreal, May, 2000.

[5] A. Chandra and K. Chakrabarty, "Combining low-power scan testing and test data compression for system-on-a-chip," in *Proceedings of IEEE/ACM Design Automation Conference*, pp. 166-169, Las Vegas, June, 2001.

[6] Il-soo Lee, Yong Min Hur, and Tony Ambler, "The Efficient Multiple Scan Chain Architecture Reducing Power Dissipation and Test Time," 13th Asian Test Symposium, pp. 94-97, 2004.

[7] Yongmin Hur, "Compression of test data for SOCs using a modified run-length method," in *IEEE International Test Synthesis Workshop*, Santa barbara, Apr. 2003.

[8] A. Chandra and K. Chakrabarty, "Test data compression for system-on-a-chip using Golomb codes," in *Proceedings of VLSI Test Symposium*, pp. 113-120, Montreal, Apr., 2000.

[9] A. Chandra and K. Chakrabarty, "Frequency-directed run-length(FDR) codes with application to system-on-a-chip test data compression," in *Proceedings of VLSI Test Symposium*, pp 42-47, Marina Del Rey, Mar., 2001.

[10] A. Jas, J. Ghosh Dastidar, and N. Touba, "Scan vector compression/decompression using statistical coding," in *Proceedings of VLSI Test Symposium*, pp. 114-121, San Diego, Apr, 1999.

[11] Mircea R. Stain and Wayne P. Burleson, "Bus-invert coding for low-power I/O," *IEEE Trans. VLSI Systems*, 3, pp. 49-58, 1995.

[12] I. Hamazaoglu and J. H. Patel, "Test set compaction algorithms for combinational circuits," in *Proceedings of International Conference on CAD*, pp. 283-289, San Jose, Nov., 1998.

[13] P. T. Gonciari, B. M. Al-Hashimi, and N. Nicolici, "Improving compression ratio, area overhead, and test application time for system-on-a-chip test data compression/decompression," in *Design, Automation and Test in Europe Conference*, pp. 604-611, Paris, Mar., 2002.

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