다목적 Error Correcting Code의 새로운 설계방법

A New Approach to Multi-objective Error Correcting Code Design Method

이희성·김은태 Heesung Lee and Euntai Kim

연세대학교 전기전자공학부

요 약

Error correcting codes는 일반적으로 soft error를 막기 위해서 사용된다. single error의 수정과 double error의 검출 (SEC-DED) 코드들은 이런 목적으로 사용된다. 본 논문에서는 이러한 회로의 크기, 지연시간, 전력 소비를 선택적으로 최소로 하는 SEC-DED의 설계방법을 제안한다. 이러한 SEC-DED의 설계는 비선형 최적화 문제로 포함되는데 우리는 다목적 유전자 알고리즘을 이용하여 이 문제를 해결한다. 제안하는 방법은 여러 가지 SEC-DED code들을 제공하여 사용자의 환경에 따라 알맞은 회로를 선택할 수 있도록 한다. 제안하는 방법을 효율적인 ECC코드로 알려져 있는 odd-column weight Hsiao code에 적용하여 그 효율성을 입중하였다.

Abstract

Error correcting codes (ECCs) are commonly used to protect against the soft errors. Single error correcting and double error detecting (SEC-DED) codes are generally used for this purpose. The proposed approach in this paper selectively reduced power consumption, delay, and area in single-error correcting, double error-detecting checker circuits that perform memory error correction. The multi-objective genetic algorithm is employed to solve the non-linear optimization problem. The proposed method allows that user can choose one of different non-dominated solutions depending on which consideration is important among them. Because we use multi-objective genetic algorithm, we can find various dominated solutions. Therefore, we can choose the ECC according to the important factor of the power, delay and area. The method is applied to odd-column weight Hsiao code which is well-known ECC code and experiments were performed to show the performance of the proposed method.

Key Words: Error correcting code, SEC-DED, Hsiao codes, genetic algorithm, multi-objective optimization

1. Introduction

As technology continues to scale with smaller features sizes, lower power supply voltages and higher operating frequencies, the soft error rate in logic circuits is rapidly increasing [1]. Concurrent error detection using error correcting codes (ECCs) at the outputs of a circuit provides means to detect soft errors quickly before they have a chance to propagate and compromise the data integrity of a system. Therefore, we can enhance system reliability and data integrity using the error correcting codes which commonly used to protect against soft errors. For this reason, such circuits are widely used in industry in all types of memories including caches and embedded memories.

On the other hands, a power reduction design crite rion has become very important in recent times [2]. With increasing miniaturization of devices, power has

접수일자: 2007년 12월 28일 완료일자: 2008년 6월 4일

This work was supported by the Ministry of Commerce, Industry and Energy of Korea.

become a first-order design consideration motivating researchers to look at techniques of reducing power consumption in all components of system design. Particularly, power reduction is an important consideration in ECC, since the ECC checker circuit is activated during reading and writing access to the memory, which happen frequently. Not only power consumption, but also area and delay are very important factors in ECC circuit design criterion. As power, delay and area have become an important consideration, researchers have proposed various methods to reduce power consumption and delay and area in error detection circuitry. Most of the works, however, have been developed for general circuits can be applied to the design of error detection circuitry in a straightforward manner.

In this paper, we proposed a new method to reduce power consumption and minimize the delay and size in specific memory ECC checkers. There are many ways to construct SEC-DED codes and implement the corresponding ECC circuitry. The proposed approach selects a parity check matrix that minimizes power, area and delay using multi-objective genetic algorithm (GA). GA provides an adaptive and robust computational proce-

dure modeled on the mechanics of natural genetic systems [3]. Through multi-objective GA, we can find various non-dominated optimal solutions of ECC circuitry design problems with respect to power, area, and delay. Therefore, the proposed method allows that ECC circuit user can choose one of various non-dominated solutions depending on which consideration is important among power, area and delay. The paper is organized as follows: Section 2 gives backgrounds about the ECC and multi-objective genetic algorithms. Section 3 gives the proposed implementing way to the memory ECC checkers. In Section 4, the experimental results and discussion are presented. We give our conclusions in Section 5.

2. Background

2.1 Error Correcting Code

Error correcting codes are commonly used to protect against soft errors. The codes are represented by a parity-check matrix, H which is used on every memory access (both read and write). Once H has been selected, the corresponding ECC circuitry for implementing the codes can be synthesized in a straghtforward way. Let's consider an (n,k) code, n is the code word length, k is the number of data bits and (n-k) is the number of parity check bits. The H-matrix defined as

$$H = \left[A^T \middle| I_{n-k} \right] \tag{1}$$

where A is a k-by-(n-k) parity check generator matrix and I_{n-k} is an (n-k)-by-(n-k) identity matrix. Therefore, the parity check matrix has (n-k) row, one for each check bit, and n columns, one for each bit in the codeword. To construct a SEC-DED codes, the H-matrix must be formed in a way that the minimum distance between any codes words is four, which implies that three or fewer columns of the H-matrix are linearly independent. Hsiao [4] shows that one way to satisfy this condition is to have the columns of the H-matrix meet the following constraints:

- 1) There are no all-0 columns.
- 2) Every column is distinct.
- 3) Every column contains an odd number of 1's

Therefore, there are many ways to construct ECC code that provide SEC-DED capability and different H-matrices result in different power, size and delay. When we design the Hsiao code, there are two degrees of freedom in selecting the H-matrix that can be used to reduce the power, size and delay. The first degree of freedom is simply permuting the columns of the parity check matrix. The second degree of freedom is selecting the odd weight columns that are included in the matrix. Therefore, if we select an appreciate H-matrix, power, size and delay reduction of the ECC can be obtained.

2.2 Multiobjective Genetic Agorithm

Genetic algorithms (GAs) are numerical optimization algorithms inspired by natural selection and natural genetics and these methods have been applied to a wide range of problems [5]. The GAs typically maintain a population of individuals which represents the set of solution candidates for the problem to be solved. The goodness of each candidate solution is evaluated based on its fitness value. The population of the GAs evolves by selection, crossover and mutation. In the selection process, some individuals are selected to be copied into a tentative next population. Individuals with higher fitness values are more likely to be selected for the next generation with the number of copies proportional to their fitness values. The selected individuals are altered to search for a global optimal solution in the mutation and crossover. Given below is the basic configuration of the GA.

```
procedure Genetic Algorithm

begin

initialize P(t);

while termination-condition not satisfied do

begin

evaluate P(t);

select P(t+1) from P(t);

crossover P(t+1);

mutation P(t+1);

t=t+1;

end

end
```

The multi-objective genetic local search algorithm tries to find all non-dominated solutions of an optimization problem with multiple objectives [6]. Let us consider the following multi-objective optimization problem with n objectives

$$\min f_1(x), f_2(x), ..., f_n(x)$$
 (2)

when the following inequalities hold between two solutions x_1 and x_2 , the solution x_2 is said to dominate the solution x_1 :

$$\forall i: f_i(x_1) \ge f_i(x_2) \text{ and } \exists j: f_i(x_1) > f_i(x_2)$$
 (3)

If a solution is not dominated by any other solutions of the multi-objective optimization problem, that solution is said to be a non-dominated solution. Examples of non-dominated solutions are shown in Fig. 1, where dominated solutions and non-dominated solutions are depicted by open circles and closed circles in a two-dimensional (2-D) objective space, respectively. The 2-D objective space in Fig. 1 corresponds to the following two objective optimization problem:

$$\min f_1(x) \text{ and } \min f_2(x)$$
 (4)

As is shown in Fig. 1, multi-objective optimization

problems usually have several non-dominated solutions. The aim of multi-objective genetic algorithm is not to determine a single final solution but to try to find all non-dominated solutions of the multi-objective optimization problem in (2).

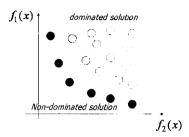


Fig. 1. Non-dominated solutions and dominated solutions

3. New Multi-Objective Design Method for ECC

In this paper, we design an ECC based on the mul ti-objective GA. Because GA is a good solution for the complicated combinational problem in a large search space, among a number of possible ECC codes, we can find the most efficient code in terms of the power, area and delay [7].

3.1 Encoding

The Hsiao code is composed of all low order odd weight columns and some of high order odd weight columns. Therefore, the chromosome includes both the permutation part of low order odd weight columns and the list part of selected high order odd weight columns. The input permutation part is encoded as a string of the mapping for the input memory bits position and an additional component representing the design of the Hmatrix. Because we use 64-bit architecture, we index the 56 possible weight 5 columns in increasing order of their binary representation. The chromosome is repre sented by both the permutation of the 64 with all possible weight-1 and weight-3 columns and the indices of the 8 weight-5 columns in the 56 possible ones. 8 weight-5 columns are selected to fill up the last 8 positions of the H-matrix which is selection part. Fig. 2 shows the structure of the chromosome for Hsiao code. In the general case, for architectures of other sizes, the chromosome would have a representation of a similar design choice of selecting some columns from a total set of possible odd weight columns.

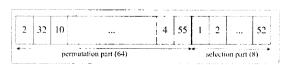


Fig. 2. Chromosome of the ECC code

3.2 Genetic Operator

The genetic operators are used to create new solutions in the new generation from the existing solutions in the current population. Basically, there are two types of genetic operators: crossover and mutation. Crossover takes two chromosomes and produces two new chromosomes. In this paper, we use cycle crossover [8] and arithmetic crossover. We apply the cycle crossover to the permutation part and arithmetic crossover to the selection part as shown in Fig. 3.

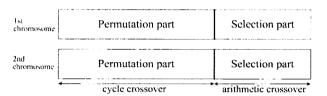


Fig. 3. Crossover

The absolute positions of the genes in the parent chromosomes denote the column of the parity check matrix and the cycle crossover preserves the important positions. The cycle crossover builds offspring in such a way that each position comes from one of the parents. For this reason, in our former work [9], we suggested an idea of combining cycle and arithmetic crossover and obtained new chromosomes which inherit the features of the parents.

3.3 Fitness Function

The fitness function is computed by combination of the delay in the circuit, the size of the circuit and the power dissipation. It is a weighted linear combination of the three components. It is inversely proportional to the power dissipated during ECC checking where we use 2-input XOR gates and the power dissipation occur when gates switch the output. And it is also inversely proportional to the delay and size which is modeled by the number of total gates in the circuit and variance between the depths of the XOR circuits. When we apply GA to the multi-objective optimization problem, we have to evaluate a fitness value of each solution. We define a fitness function of the solution by the following weighted sum of the objectives:

$$\min f(x) = -w_1 f_1(x) - w_2 f_2(x) - w_3 f_3(x) \tag{5}$$

where $f_1(x)$, $f_2(x)$ and $f_3(x)$ are normalized values of the power dissipation, size and delay, respectively, and $w_1.w_2$ and w_3 are non negative weights for the objectives, which satisfy the following relations:

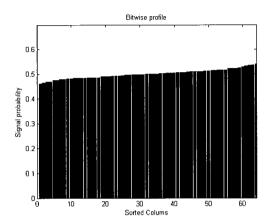
$$\begin{array}{l} w_i \geq 0 \ {\rm for} \ i = 1,2,3 \\ w_1 + w_2 + w_3 = 1 \end{array} \tag{6}$$

In previous method [10], they used fixed and constant weighs in (5). Therefore, the search direction by GA is fixed. To solve the problem and realize various search

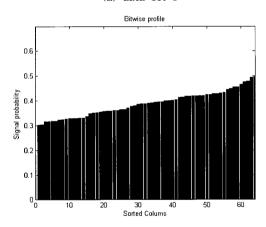
directions, we use the weight values which are determined as [11]

$$w_i = \frac{rand_i}{\sum_{i=1}^{3} rand_i} \text{ for } i = 1, 2, 3$$
 (7)

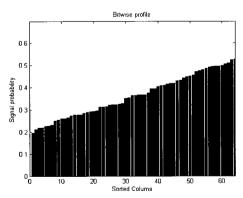
where rand, is non-negative random real numbers.



(a) data set 1



(b) data set 2



(c) data set 3

Fig. 4. Bitwise profile of the memory data

4. Experiments

In this section, we present some experiments that illustrate the performance of the suggested method. These experiments deal with synthetic data. We performed experiment on three synthetic 64 bit memory

Fig. 4 shows the characteristics of the three svnthetic data. While all bits of the data set 1 are likely to have an even distribution between zero and one, the high order bits of the data set 3 are more likely to be a zero than one and the low order bits are more likely to have an even distribution between zero and one. The characteristics of data set 2 lies between the characteristics of data set 1 and data set 3. The evolution parameters used in this paper are given in Table 1.

Table 1. Evolution parameters

Parameter	Value	
Max. generation number	200	
Population number	200	
Crossover rate	0.6	
Mutation rate	0.05	

In Table 2, the results of the proposed methods are given. We compare the proposed method with the previous method [10] in terms of the non-dominated solutions for power, delay and area. To estimate power consumption, delay and area, the circuit corresponding to each parity check matrix was synthesized by multiple output logic minimization with 2-input XOR gates. The power consumption is computed by the number of transitions in the outputs of the XOR gates. Further, the size and delay of circuit are checked by the number of total gates in the circuit and the variance between the depths of the XOR circuits, respectively.

Table 2. Non-dominated solutions of the proposed

method			
	Data set 1	Data set 2	Data set 3
Power	10549	10211	9791
Delay	8	8	8
Area	181	181	181
	Data set 1	Data set 2	Data set 3
Power	10805	10442	10293
Delay	8	8	8
Area	179	179	179
	Data set 1	Data set 2	Data set 3
Power	10837	10411	9880
Delay	7	7	7
Area	180	181	180

In Table 3, we give some solutions that have high fitness value and are contained in the last generated population of the previous genetic method. It can be seen that solutions of pervious method are dominated by those of proposed method in terms of the all ECC design factors. Therefore, through proposed method, we can choose the ECC according to the important factor of the power, delay and area.

Table 3. Dominated solutions of the previous method

	Data set 1	Data set 2	Data set 3	
Power	10656	10233	9946	
Delay	8	8	8	
Area	182	181	181	
	Data set 1	Data set 2	Data set 3	
Power	10752	10248	9795	
Delay	8	8	8	
Area	183	182	182	
	Data set 1	Data set 2	Data set 3	
Power	10812	10313	10134	
Delay	8	8	9	
Area	180	181	180	

5. Conclusion

In this paper, we optimize the *H*-matrix of the mem ory ECC checker using multi-objective GA with re ducing the power consumption and delay and area of the circuit. Once the H-matrix has been selected, the corresponding ECC circuitry for implementing the code can be synthesized. A design criterions that has become very important in recent times are power, delay and area. The proposed approach selects a parity check matrix that minimizes power, area and delay using multi-objective genetic algorithm. Because we use multi-objective genetic algorithm and employ special genetic operator for ECC design problem, we can find various dominated solutions comparison with previous method. Therefore, we can choose the ECC according to the important factor of the ECC design factors. The method is applied to odd-column weight Hsiao code which is well-known ECC code and experiments shows that our method can find non-dominated solutions comparison with those of the pervious method.

Referinces

[1] C. L. Chen and M. Y. Hsiao, "Error-Correcting Codes for Semiconductor memory applications: A State of the Art review," *IBM J. Res. Develop.*, vol. 28, pp. 124–134, July 1984.

- [2] K. Favalli and C. Metra, "Design of Low-Power CMOS Two-Rail Checkers," Journal of Microelectronics Systems Integration, vol. 5, no. 2, pp. 101-110, 1997.
- [3] L. Davis, *Handbook of Genetic Algorithms*, Van Nostrand Reinhold, 1991.
- [4] M. Y. Hsiao, "A class of optimal minimum odd-weight-column SECDED codes," *IBM J. Res. Develop.*, vol. 14, pp. 395-401, July 1970.
- [5] H. Lee, E. Kim, and M. Park, "A genetic feature weighting scheme for pattern recognition," *Integrated Computer-Aided Engineering*, vol. 14, pp. 161–171, 2007.
- [6] H. Ishibuchi and T. Murata, "A multi-objective genetic local search algorithm and its application to flowshop scheduling," *IEEE Trans. Systems, Man, and Cybernetics— part c*, vol. 28, pp. 392–403, 1998.
- [7] H. Lee, J. Lee, and E. Kim, "Multi-objective genetic design for error correcting code," *International Symposium on advanced Intelligent Systems*, pp. 792-795 Sep. 2007.
- [8] D. Coley, An Introduction to Genetic Algorithms for Scientists and Engineers, World Scientific, 1999.
- [9] H. Lee, J. Sung, and E. Kim, "Reducing power in error correcting code using genetic algorithm," in Proc. Int. Conf. Computer Information and Systems Science and Engineering, pp. 179-182, 2007.
- [10] S. Ghosh, S. Basu, and N. Touba, "Reducing Power Consumption in Memory ECC Checkers," *International Test Conference*, pp. 1322-1331, 2004
- [11] T. Murata and H. Ishibuchi, "MOGA: Multi-objective genetic algorithms," in Proc. 2nd IEEE Int. Conf. Evolutionary Computat., pp. 289 294. 1995.

저 자 소 개



이희성 (Heesung Lee)

2003년: 연세대학교 전기전자공학부

졸업(공학사)

2005년: 연세대학교 전기전자공학부 석사과정 졸업(공학석사)

2005년~현재:동 대학원 전기전자공학과

박사과정

관심분야 : Computational intelligence, 로봇 비전, 패턴 인식

E-mail : 4u2u@yonsei.ac.kr



김은태 (Euntai Kim)

1992년 : 연세대학교 전자공학과 졸업

(공학사, 전체수석)

1994년 : 연세대학교 전자공학과 석사

과정 졸업(공학석사)

1999년: 연세대학교 전자공학과 박사

과정 졸업(공학박사)

1999년 3월~2002년 2월: 국립한경대학교

제어계측공학과 조교수

2002년 3월~현재: 연세대학교 전기전자공학부 부교수 2003년: University of Alberta, visiting researcher 1998년~현재: IEEE TFS, IEEE SMC, IEEE CAS,

FSS 등에서 심의위원 활동 중

2003년:대한 전자공학회 해동상 수상

관심분야: Computational intelligence, 지능형 로봇

Phone : +82-2-2123-2863 E-mail : etkim@yonsei.ac.kr