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실리콘/수소/질소의 결합에 따른 MONOS 커패시터의 계면 특성 연구

(Interface Traps Analysis as Bonding of The Silicon/Nitrogen/Hydrogen in MONOS Capacitors)

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요 약

본 연구는 실리콘 기판과 실리콘 산화막 사이의 계면 트랩 밀도와 게이트 누설 전류를 조사하여, Metal-Oxide-Nitride-Oxide-Silicon (MONOS) 메모리 소자의 계면 트랩 특성의 수소-질소 열처리 효과를 조사하였다. 고속 열처리 방법으로 850도에서 30초 동안 열처리한 MONOS 샘플들을 질소 가스와 수소-질소 혼합 가스를 사용하여 450도에서 30분 동안추가 퍼니스 열처리 공정을 수행하였다. 열처리 하지 않은 것, 질소, 수소-질소로 열처리 한 세 개의 샘플 중에서, 커패시터-전압 측정 결과로부터 수소-질소 열처리 샘플들이 가장 적은 계면 트랩 밀도를 갖는 것을 확인하였다. 또한, 전류-전압 측정 결과에서, 수소-질소 열처리 소자의 누설전류 특성이 개선되었다. 위의 실험 결과로부터, 수소-질소 혼합 가스로 추가 퍼니스 열처리의해 실리콘 기판과 산화막 사이의 계면 트랩 밀도를 상당히 줄일 수 있었다.

Abstract

The effect of hydrogen-nitrogen annealing on the interface trap properties of Metal-Oxide-Nitride-Oxide-Silicon (MONOS) capacitors is investigated by analyzing the capacitors' gate leakage current and the interface trap density between the Si and SiO_2 layer. MONOS samples annealed at 850 ℃ for 30 s by rapid thermal annealing (RTA) are treated by additional annealing in a furnace, using annealing gases N_2 and 2% hydrogen and 98% nitrogen gas mixture (N_2-H_2) at 450 ℃ for 30 mins. Among the three samples as-deposited, annealed in N_2 and N_2-H_2, MONOS sample annealed in an N_2-H_2 environment is found to have the lowest increase of interface-trap density from the capacitance-voltage experiments. The leakage current of sample annealed in N_2-H_2 is also lower than that of sample annealed in N_2..

Keywords : MONOS, hydrogen-nitrogen annealing, radical-blocking oxide, NBTI/PBTI

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Ⅰ. Introduction

Metal/Oxide/Nitride/Oxide/Silicon (MONOS) structures have attracted a great deal of attention for next-generation flash memory applications, because of its advantages such as film scalability, process simplicity and power economy [1-3]. However, this

device has still suffered from reliability problem such as high voltage operation, slow program/erase (*P/E*) speed and poor retention characteristics [4]. One of the requirements to increase the reliability of the MONOS memory is to improve the insulation and reliability characteristics of the blocking oxide (or top oxide) layer, grown on the silicon-nitride (Si_3N_4) layer. The quality of the blocking oxide layer grown by conventional chemical vapor deposition (CVD) is not satisfactory in terms of its electrical and reliability properties, due to the native film properties such as the poor dielectric strength, high leakage current, high interface traps, bulk charges and low growth rate [5]. Recently, silicon-oxide (SiO_2) layer grown by radical oxidation has been a popular choice and was widely studied because of its high film density, smooth silicon (Si) and silicon-oxide (SiO_2) interface at low oxidation temperatures and uniform oxide thickness. Moreover, it has been verified that radical oxidation is quite effective in lowering the oxidation temperature [6].

In previous work[7], we proposed a highly reliable oxide grown by radical oxidation and compared that with the CVD method for creating the blocking oxide layer of MONOS capacitors. We found that sample with the radical blocking oxide had abundant memory-traps, low voltage operation, fast *P/E* speed and good retention characteristics when compared to the conventional CVD oxide[7~8]. However, information of interface traps between the Si and SiO_2 layer in our radical samples is still important for better a reliability characteristics because the interface traps degrade device reliability during *P/E* operations.

In this work, the passivation effect of interfacial traps between Si and SiO_2 layer were investigated in order to reduce the interface traps density (D_{it}) in our radical sample.

Ⅱ. Experiment Details

We prepared three MONOS samples with blocking oxide layers grown by radical oxidation. The key steps for fabricating the MONOS samples are as follows. First, a 2.4 nm-thick tunneling oxide layer was formed at 950 ℃ by using a radical oxidation technique. Then, a 9.6 nm-thick Si_3N_4 film of charge-trapping layer was subsequently deposited by low pressure chemical vapor deposition (LPCVD) at 750 ℃, via the reaction of dichlorosilane ($SiCl_2H_2$) and ammonia (NH_3) gases. Then, a 3.4 nm-thick radical blocking oxide layer was grown by radical oxidation using oxygen radical (O^*) gas. Each of the layers were determined by spectroscopic ellipsometry. Prior to post-annealing, the ONO structures were cleaned with a standard sulfuric acid and hydro-peroxide mixture for 10 minutes. After drying in a nitrogen ambient atmosphere, the ONO samples were furnace annealed using a nitrogen (N_2) and 2 % hydrogen and 98 % nitrogen mixture gas (N_2-H_2) at 450 ℃ for 30 minutes, respectively. Fig. 1 illustrates the interface state between Si and SiO_2 layer as annealing gases. After annealing the ONO samples,

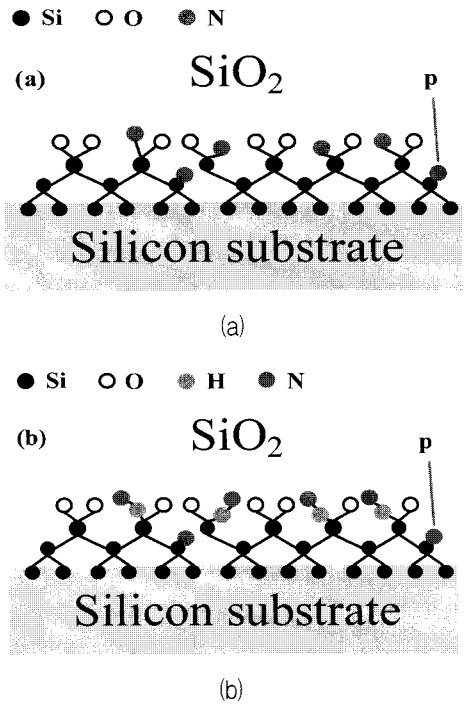

그림 1. 도식도: (a) 실리콘/실리콘산화막 계면의 실리콘-질소 결합 (b) 실리콘/실리콘산화막 계면의 실리콘-수소-질소 결합

Fig. 1. Schematic representation of the: (a) Si-N bonding at Si/SiO_2 interface and (b) Si-H-N bonding at Si/SiO_2 interface.

the 600 um diameter aluminum gate electrode was deposited on top of the blocking oxide layer using an e-beam evaporator. The electrical characteristics, such as capacitance-voltage (*C-V*) and current-voltage (*I-V*) were measured by using a *C-V*.

Ⅲ. Results and Discussion

In our earlier work, the effect of the radical blocking oxide on the switching behaviors of the MONOS memory devices was compared with CVD process. It was found that the radical blocking oxide device exhibited abundant memory-traps (or nitride-related traps), low voltage operation, fast *P/E* speed and long data retention characteristics, compared to the CVD blocking oxide device[5]. However, the low voltage operation of the radical blocking oxide device is hindered by a negative bias temperature instability (NBTI)[9~11]. This may cause a flat band voltage shift (ΔV_{FB}) due to the generated interface traps between the Si and SiO_2 layers as well as the injected positive oxide charge in silicon-nitride layer. Therefore, we investigate the hydrogen passivation effect to reduce the influence of generated interface traps and injected positive oxide charge on the flat band voltage shift.

Fig. 2 shows the capacitance-voltage (*C-V*) characteristics of the as-deposited MONOS capacitor (sample A) in comparison with the N_2 annealed capacitor (sample B) and N_2-H_2 annealed capacitor (sample C). We measured the high frequency *C-V* hysteresis for the three samples to compare their memory capacities. The voltage sweep was performed in the range [-6~6 V] at room temperature. The memory windows were 1.65, 2.2 and 2.0 V for the samples A, B and C, respectively. The sample B and C showed larger memory window than that of the sample A but the memory windows of the two samples appeared similarly[12]. It seems that the memory window size is not significantly affected by the annealing gas, because there was little difference between samples annealed in both N_2 and N_2-H_2 gases.

Fig. 3 shows the trapped charge density (N_T), which was evaluated by measuring the flat band voltage shift, as given by [13].

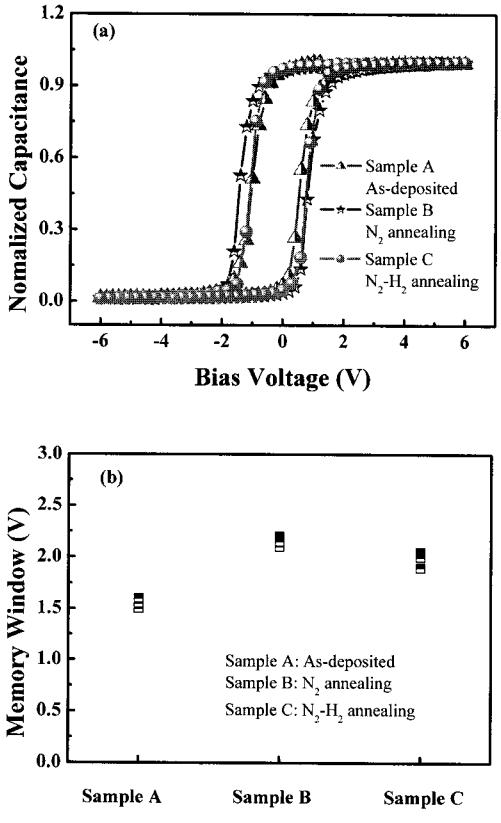

그림 2. MONOS 커패시터의 *C-V* 특성: (a) 곡선 (b) 메모리 윈도우.

Fig. 2. *C-V* characteristics of the MONOS capacitors: (a) hysteresis and (b) memory window.

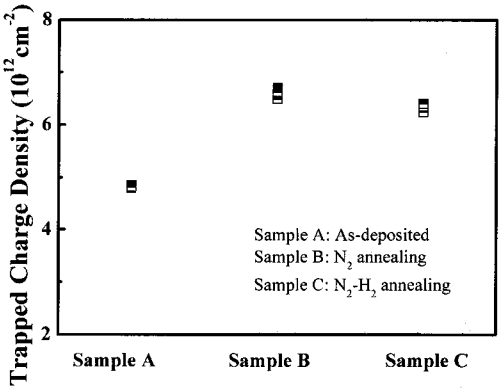

그림 3. 열처리 가스에 따른 MONOS 커패시터의 트랩 전하 밀도 특성.

Fig. 3. Trapped charge density of the MONOS capacitors as annealing gases.

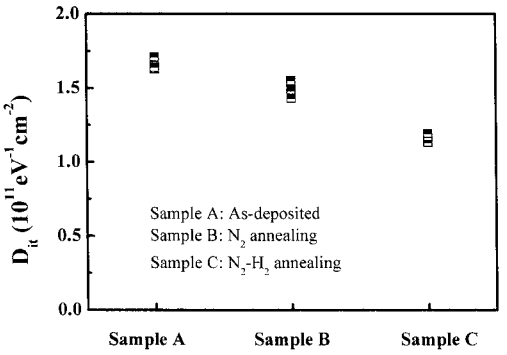

그림 4. 열처리 가스에 따른 MONOS 커패시터의 계면 트랩 밀도 특성.

Fig. 4. Interface traps density of the MONOS capacitors as annealing gases.

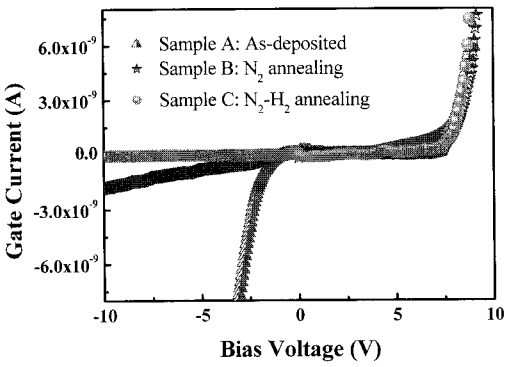

그림 5. 열처리 가스에 따른 MONOS 커패시터의 *I-V* 특성.

Fig. 5. *I-V* characteristics of the MONOS capacitors as annealing gases.

$$N_T = \frac{\Delta V_{FB}}{(q[(X_{Si3N4}/2\varepsilon_o\varepsilon_{Si3N4}) + X_{SiO2}/\varepsilon_o\varepsilon_{SiO2}])} \quad (1)$$

where X_{Si3N4} and X_{SiO2} represent the thicknesses of the charge storage (Si_3N_4) layer and blocking oxide (SiO_2) layer, respectively. In our case, X_{Si3N4} = 96 Å and X_{SiO2} = 34 Å. The terms ε_{Si3N4} and ε_{SiO2} are the dielectric constants of silicon-nitride and the blocking oxide, respectively. The N_T for the samples A, B and C were calculated as 4.8x10^{12} /㎠, 6.6x10^{12} /㎠ and 6.3x10^{12} /㎠, respectively. The results indicate that the annealing process is dominant parameter to increase both the N_T and memory window because nitrogen and hydrogen annealing process can increase the memory traps (nitride-related traps) sites in the Si_3N_4 and Si_3N_4/SiO_2.

On the other hand, Fig. 4 shows the interfacial trap generation (D_{it}) between the Si and SiO_2 layer as function of annealing gas. The interfacial trap density, D_{it}, was evaluated by measuring the high frequency *C-V* curve, as given by [14]

$$D_{it} = \frac{C_{OX}}{q}\left(\frac{dV_{FB}}{d\phi_S} - 1\right) - \frac{C_S}{q} = \frac{C_{OX}}{q}\frac{d(\Delta V_{FB})}{d\phi_S} \quad (2)$$

where C_{OX} and C_S represent the oxide capacitance and the substrate capacitance, respectively, and $\triangle V_{FB}$ is the flat band voltage shift of the experimental value from the ideal curve. D_{it} for the samples A, B and C, were calculated as 1.7 x10^{11}, 1.5 x10^{11} and 1.2 x10^{11} ($eV^{-1}cm^{-2}$), respectively. It appears that $\triangle D_{it}$ for sample C was reduced to about 30 % more than sample A. In this result, the reduced interface trap density in sample C might be due to the passivation effect via nitrogen-hydrogen bonding with the traps at the interface between the Si and SiO_2 layers. It has been reported that the silicon-nitrogen-hydrogen (Si-N-H) bonding with the traps are located at the interface between the Si and SiO_2 layers. According to the reference [15], the binding energies of Si/N/H alloys are subject to change depending on the bonding conditions; Interestingly, although the binding energy of Si-H bonding is 3.34 eV, which is smaller than 3.45 eV of the Si-N bonding, its binding energy is known to be increased up to 4.05 eV once Si-N-H bonding is formed[15]. Because a hydrogen-nitrogen (N_2-H_2) gas mixture was used for annealing the samples, the formation of Si-N-H bonding (or hydrogen passivation) would reduce the chance to generate interface traps in the MONOS structure[15~16].

Fig. 5 shows the gate leakage currents versus applied gate voltage (V_G) for the sample A, B and C. The gate leakage current of the samples A, B and C were -10 nA, -0.65 nA and -45 pA when V_G was -3.5 V. Specifically, we observed a sudden increase of current for sample A near -2 V. This experiment

illustrated that the gate leakage currents differed with respect to annealing gas, which was probably caused by modification of the interface traps in the Si and SiO_2 interfacial layer. We state that N_2-H_2 post-annealing is more effective in reducing the interfacial traps than treatments in nitrogen ambient gas only. In this result, we can predict that the change of the V_{FB} for the sample C is more stable than that of sample B, under the negative bias temperature stress.

Ⅳ. Conclusion

MONOS capacitor samples have been thermally annealed at in an N_2-H_2 gas mixture environment in order to reduce the interface traps density between the Si and SiO_2 layer. As a result, it was found that N_2-H_2 gas annealing is more effective than the N_2 gas annealing in reducing such interface traps, which was explained by the formation of Si-N-H bonding (or hydrogen passivation). The leakage current of the sample annealed with an N_2-H_2 gas mixture is also lower than that of the sample annealed with N_2. gas.

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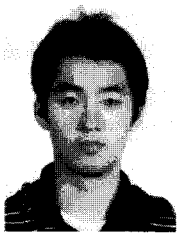

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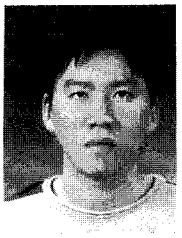

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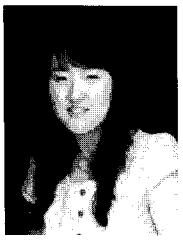

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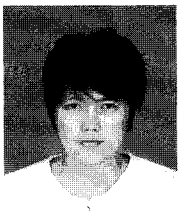

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