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S-파라미터 측정을 통한 MOSFET 캐리어 속도의 고온 종속 SPICE 모델링

(High Temperature Dependent SPICE Modeling for Carrier Velocity in MOSFETs Using Measured S-Parameters)

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요 약

0.18μm deep n-well 벌크 NMOSFET에서 측정된 차단주파수 f_T의 고온종속성을 모델화하기 위해, 측정된 S-파라미터를 사용한 정확한 RF 방법으로 30℃에서 250℃까지 전자속도 고온 데이터가 추출되었다. 이러한 추출데이터를 사용하여 개선된 온도종속 전자속도 방정식이 높은 온도의 범위에서 생기는 기존 방정식의 모델링 오차를 없애기 위해 개발되었으며 BSIM3v3 SPICE RF 모델에 구현되었다. 개선된 온도 종속 방정식은 기존 모델보다 30℃에서 250℃까지 측정된 f_T와 더 잘 일치하였으며, 이는 개선된 방정식의 정확성을 입증한다.

Abstract

In order to model the high temperature dependence of the cutoff frequency f_T in 0.18μm deep n-well isolated bulk NMOSFET, high temperature data of electron velocity of bulk MOSFETs from 30℃ to 250℃ are obtained by an accurate RF extraction method using measured S-parameters. From these data, an improved temperature-dependent electron velocity equation is developed and implemented in a BSIM3v3 SPICE model to eliminate modeling error of a conventional one in the high temperature range. Better agreement with measured f_T data from 30℃ to 250℃ are achieved by using the SPICE model with the improved equation rather than the conventional one, verifying its accuracy of the improved one.

Keywords : high temperature, MOSFET, carrier velocity, SPICE modeling, S-parameters

I. INTRODUCTION

With the rapidly growing personal wireless communication markets, bulk CMOS technology becomes very popular due to strong possibilities for integrating baseband, intermediate frequency, and RF module as one-chip[1]. It is recently reported that the use of deep n-well isolated bulk NMOSFETs with body-tied source is very promising for high temperature RF applications, because it has lower leakage current and better RF performance than Partially-Depleted SOI NMOSFETs[2]. In particular, deep n-well MOSFET technology might be emerging as commercially better solution, mainly due to lower cost than SOI. In general, the cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}) are used as measures that display RF performance of MOSFETs. Thus, accurate modeling of high temperature-dependent f_T should be performed to predict the high-speed and RF performance of MOSFETs in high temperature operation. The value

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of f_T determining the maximum device speed is ultimately limited by the carrier velocity (v_{eff}) under the velocity saturation region. Thus, v_{eff} is the most important parameter for SPICE modeling of f_T in MOSFET. Due to the reduction of v_{eff} at high temperatures, f_T decreases with increasing temperature[3~4]. In the BSIM3v3 SPICE model[5], the linearly decreasing temperature-dependent v_{eff} equation is used, but produces inaccuracy in modeling v_{eff} data in the wide range of high temperatures[6].

Therefore, in this paper, accurate high temperature SPICE modeling process in 0.18μm deep n-well isolated bulk NMOSFET from 30℃ to 250℃ is presented in detail by developing an improved temperature-dependent v_{eff} equation using a RF direct extraction method based on the extraction of the gate-source capacitance and transconductance from measured S-parameters.

Ⅱ. PARAMETER EXTRACTION

S-parameters are measured on multi-finger deep n-well isolated bulk NMOSFETs with various gate length L_g at the unit finger width of Wu=2.5μm and the number of gate finger of Nf=16 under the source-bulk tied configuration as the wafer is heated from 30℃ to 250℃ using a hot chuck. The accurate de-embedding procedure using "open" and "short" test patterns was carried out to remove pad and interconnection parasitics from measured S-parameters[7].

According to MOS device physics, a maximum value of f_T in the velocity saturation region is roughly expressed as $v_{eff}/(2\pi L_g)$. In order to model the temperature-dependent f_T behavior accurately, v_{eff} is extracted by using the following RF method.

In order to extract v_{eff} in the velocity saturation region, the following equation[8] is used.

$$v_{eff} = g_{mi}/K \qquad (1)$$

where g_{mi} is the intrinsic transconductance and K is obtained by the slope of the best regression line of C_{gs} versus L_g. The equation (1) allows us to extract v_{eff} without the difficult extraction of the parasitic gate-source capacitance Cp and the effective channel length L_{eff}. The velocity saturation condition of $\partial v_{eff}/\partial V_{gs} = \partial g_m/\partial V_{gs} = 0$ can be satisfied at the value of V_{gs} where g_m versus V_{gs} at high V_{ds} becomes a maximum value[8]. The bias of $V_{gs}=V_{ds}=1V$ is applied in this work to satisfy the condition of $\partial g_m/\partial V_{gs}=0$.

The values of g_{mi} and C_{gs} are extracted only using measured S-parameters without extra DC or C-V measurements. Fig. 1 shows a small-signal MOSFET equivalent circuit[9] used for the accurate extraction. In this figure, the transconductance is given by $g_m=g_{mi}\cdot\exp(-j\omega\tau)$ where τ is a phase delay. R_g, R_d and R_s are the gate, drain and source resistance, respectively. For the intrinsic elements, C_{gs} is the gate-source capacitance, C_{gd} is the gate-drain capacitance, C_{ds} is the drain-source capacitance, and R_{ds} is the drain-source channel resistance.

In order to extract g_{mi} and C_{gs} accurately, external parasitic elements in Fig. 1 should be removed from the measured S-parameters. Thus, in this study, the following accurate RF extraction technique has been applied. The drain resistance extraction based on zero-bias measurement[10] has been performed by finding y-intercept of the following equation approximated in the high frequency range:

$$\mathrm{Real}(Z_{22} - Z_{12}) \approx R_d + A_d \cdot \omega^{-2} \qquad (2)$$

where A_d is expressed as functions of intrinsic

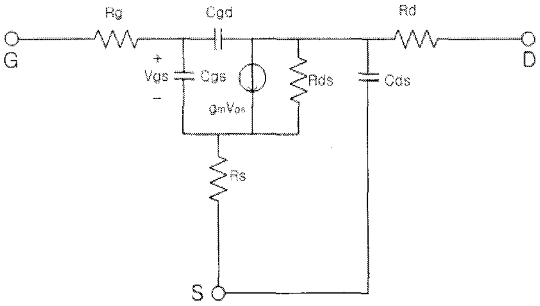

그림 1. MOSFET 소신호 모델. $g_m=g_{mi}\cdot\exp(-j\omega\tau)$
Fig. 1. A small-signal equivalent circuit model for a MOSFET. $g_m=g_{mi}\cdot\exp(-j\omega\tau)$.

parameters, and is a constant value at fixed bias.

After R_d was subtracted from measured S-parameters to obtain Y^c-parameters, C_{ds} is directly extracted by:

$$C_{ds} = (1/\omega) \cdot \mathrm{Imag}(\ Y^c_{22} + Y^c_{12}\ ) \tag{3}$$

After the extracted C_{ds} was subtracted from the Y^c-parameters to obtain Z^d-parameters, R_g is extracted by finding y-intercept of the following equation approximated at high frequencies:

$$\mathrm{Real}(\ Z^d_{11} - Z^d_{12}\ ) \approx R_g + A_g \cdot \omega^{-2} \tag{4}$$

where A_g is a function of intrinsic parameters, and independent of frequency.

The R_s value is extracted by obtaining y-intercept of $\mathrm{Real}(Z_{11} - Z_{12})$ vs. ω^{-2} for a test MOSFET where source and gate are interchanged. After Y^i-parameters are determined by subtracting R_s and R_g from the Z^d-parameters, g_{mi} and C_{gs} are extracted by the following analytical equations;

$$g_{mi} = |Y^i_{21} - Y^i_{12}| \tag{5}$$

$$C_{gs} = (1/\omega) \cdot \mathrm{Imag}(Y^c_{11} + Y^c_{12}) \tag{6}$$

As shown in Figs. 2 and 3, the extracted values of g_{mi} and C_{gs} are plotting as a function of frequency and seem to be nearly frequency-independent up to 10GHz, verifying the accuracy of the parameter extraction.

As the temperature increases, g_{mi} is greatly decreased in Fig. 2, but C_{gs} is very slightly decreased

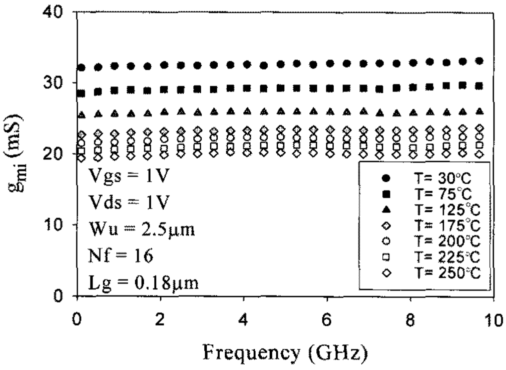

그림 2. 온도의 변화에 따라 추출된 g_{mi} 대 주파수 그래프

Fig. 2. The extracted data of g_{mi} versus frequency with varying temperature.(그림이 반전됨)

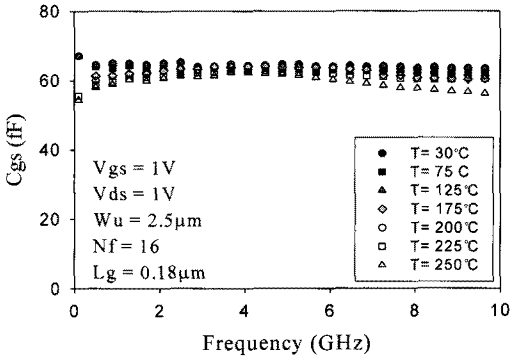

그림 3. 온도의 변화에 따라 추출된 C_{gs} 대 주파수 그래프

Fig. 3. The extracted data of C_{gs} versus frequency with varying temperature. (그림이 반전됨)

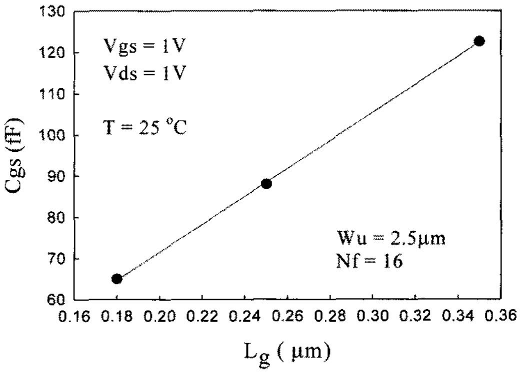

그림 4. Lg의 함수로 그린 추출된 C_{gs} 데이터

Fig. 4. Extracted data of C_{gs} as a function of Lg.(그림이 반전됨)

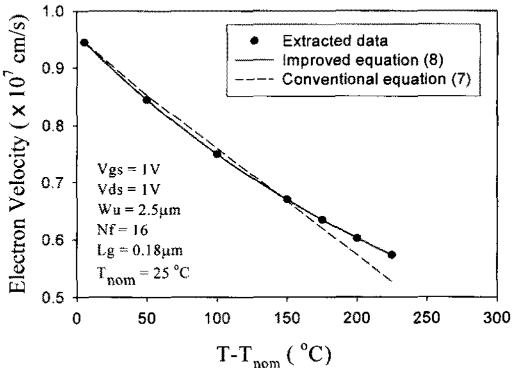

그림 5. 추출된 V_{eff}와 기존 및 개선된 방정식으로 모델된 V_{eff}와의 비교

Fig. 5. Comparison of extracted V_{eff} data with modeled curves using improved and conventional equations.(그림이 반전됨)

in Fig. 3. In the v_{eff} extraction, it is also assumed that the temperature-dependence of series resistances and C_{ds} are much smaller than that of g_{mi}. The value of K is determined from the slope of the best regression for C_{gs} versus L_g in Fig. 4 and the extracted values of v_{eff} using (1) are shown in Fig. 5.

Ⅲ. SPICE MODELING

Fig. 6 shows a modified BSIM3v3 RF model[11] suited for high-frequency circuit applications, where parasitic gate capacitances (C_{gsz}, C_{gdx}) and parasitic resistances (R_g, R_{sub}, R_{de}, and R_{se}) are externally added to an original BSIM3v3 SPICE model[5]. The parasitic elements are determined by optimizing these values to obtain the closest fit between measured and modeled S-parameters.

In order to model the temperature-dependence of v_{eff}, the following empirical equation is conventionally used in BSIM3v3 and BSIM4 models.

$$v_{eff}=V_{sat}(T)=V_{sat}(T_{nom})-A_T(T/T_{nom}-1) \qquad (7)$$

where $V_{sat}(T_{nom})$ is the saturation velocity at room temperature and A_T is the linear temperature coefficient for saturation velocity.

However, this conventional equation may be valid in the narrow range of temperature, but produces inaccuracy in modeling the reduced decreasing rate of v_{eff} data in the high temperature in Fig. 5. Thus, in order to improve this modeling of v_{eff} data, an exponentially decreasing temperature-dependent equation with a constant value is developed as follows:

$$v_{eff}=[V_{sat}(T_{nom})-V_{sat0}]e^{-BT\cdot(T/Tnom-1)}+V_{sat0} \qquad (8)$$

where V_{sat0} is the minimum saturation velocity at the infinite temperature and B_T is the exponential temperature coefficient for v_{eff}.

To verify the improved v_{eff} equation, the high temperature-dependent f_T data of bulk NMOSFETs with L_g=0.18μm are plotted in Fig. 7. As shown in Fig. 7, it is observed the decreasing rate of f_T becomes lower at higher temperatures beyond 125℃. The decreasing f_T at higher temperatures can be explained by the reduction of v_{eff} in Fig. 5. In Figs. 7 and 8, the BSIM3v3 RF model including the improved

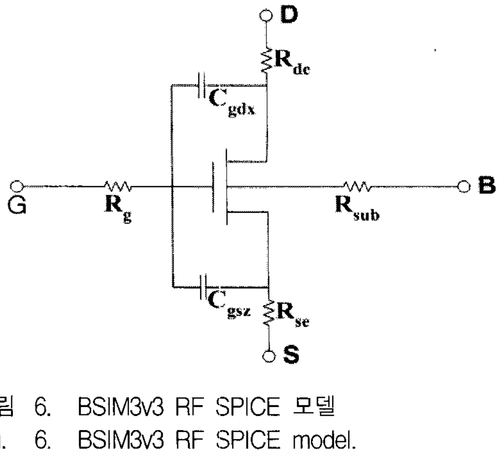

그림 6. BSIM3v3 RF SPICE 모델
Fig. 6. BSIM3v3 RF SPICE model.

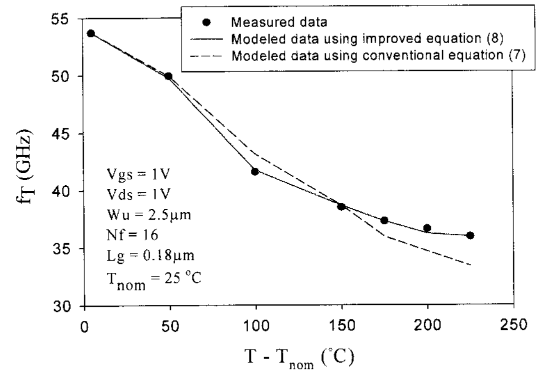

그림 7. 기존 및 개선된 방정식을 사용한 모델값과 측정 f_T 데이터
Fig. 7. Measured f_T data with modeled curves using improved and conventional equations.(그림이 반전됨)

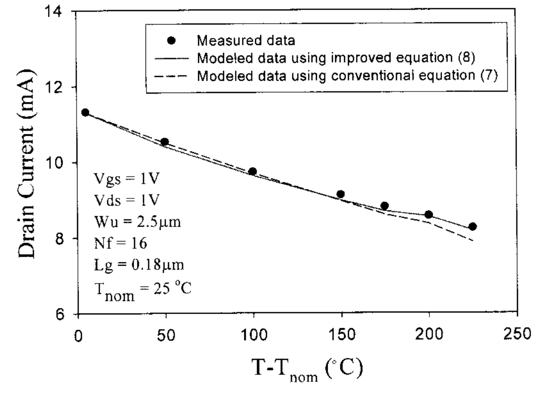

그림 8. 기존 및 개선된 방정식을 사용한 모델값과 측정 I_{ds} 데이터
Fig. 8. Measured I_{ds} data with modeled curves using improved and conventional equations.(그림이반전됨)

v_{eff} equation is verified to be accurate by finding better agreement with measured f_T and drain current I_{ds} data than the conventional one, respectively.

Ⅳ. CONCLUSIONS

In order to model the high temperature dependence of f_T from 30℃ to 250℃ on 0.18μm deep n-well isolated bulk NMOSFET, the high temperature data of v_{eff} have been extracted using a RF method based on the accurate small-signal modeling of measured S-parameters. To reduce the error of the conventional linear SPICE equation in modeling this temperature dependence, the improved temperature dependent v_{eff} one with exponentially decreasing behavior has been implemented in a modified BSIM3v3 SPICE RF model and its accuracy is validated by observing good agreements with extracted I_{ds} and f_T data from 30℃ to 250℃.

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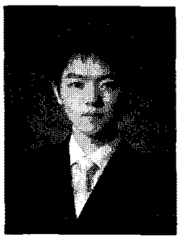

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