A Protective Layer on the Active Layer of Al-Zn-Sn-O Thin-Film Transistors for Transparent AMOLEDs

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Abstract

Transparent top-gate Al-Zn-Sn-O (AZTO) thin-film transistors (TFTs) with an Al_2O_3 protective layer (PL) on an active layer were studied, and a transparent 2.5-inch QCIF+AMOLED (active-matrix organic light-emitting diode) display panel was fabricated using an AZTO TFT backplane. The AZTO active layers were deposited via RF magnetron sputtering at room temperature, and the PL was deposited via two different atomic-layer deposition (ALD) processes. The mobility and subthreshold slope were superior in the TFTs annealed in vacuum and with oxygen plasma PLs compared to the TFTs annealed in O_2 and with water vapor PLs, but the bias stability of the TFTs annealed in O_2 and with water vapor PLs was excellent.

Keywords: oxide, thin-film transistor, protective layer, aluminum, tin, zinc

1. Introduction

Amorphous oxide semiconductors have attracted considerable attention because they have diverse applications to information displays, memory devices, and other electronics.[1-4] The main concern regarding such semiconductors is their application to the backplane of active-matrix organic light-emitting diode (AMOLED) displays.[5-6] The reliable thin-film transistor (TFT) backplane that shows good electrical performance is indispensable for the commercially available AMOLED displays. Oxide TFT is considered a prominent candidate for the driving device of AMOLED because it shows relatively high mobility, good uniformity, and stability. The conventional a-Si TFT can be fabricated with high uniformity and at a low cost, but its mobility and bias stability are poor, and the LTPS (low-temperature polysilicon) TFT is not ideal for large-size production due to its relatively poor uniformity and high cost.[5-6]

Oxide TFTs such as ZnO[7], In-Zn-O[8], Zn-Sn-O[9], and IGZO[10-11] TFTs have been widely studied. Oxide TFTs with an active layer composed of Al_2O_3-ZnO-SnO_2 (AZTO) and sputtered at room temperature have been reported by these researchers.[12] The AZTO material is very stable chemically, and the sputtering method has the advantages of low cost and large-area uniformity among the various existing deposition methods. Therefore, the AZTO TFT is a prominent device for driving the large-size AMOLED panel. The active-insulator interface is known to be very important for controlling the electrical characteristics and stability of TFTs.[13-14] The channel surface composed of an active-insulator interface is contaminated during the active-patterning process in the top-gate structure. Thus, the Al_2O_3 protective layer (PL) was deposited on the active layer for channel protection, and then the active layer was patterned via conventional photolithography and the wet etching process. The TFT characteristics are considered affected by the condition of the interface between the active layer and the PL. In this study, it was found that the top-gate AZTO TFT characteristics are dependent on the deposition process of the PL and on the annealing process of the active layer.

2. Experiment

Top-gate TFTs with active layers composed of Al_2O_3-

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ZnO-SnO_2 (AZTO) were fabricated. The schematic diagram of the top-gate AZTO TFT structure is shown in Fig. 1. A 100x100-mm^2 alkaline-free glass was used as a substrate after ultrasonic cleaning with acetone, isopropyl alcohol, and DI water, in sequence. Gate and source/drain electrodes were constituted with 150-nm-thick ITO (indium tin oxide). A 180-nm-thick Al_2O_3 gate insulator was formed at 150°C via atomic-layer deposition (ALD). An AZTO layer was formed via the co-sputtering of Al_2O_3-ZnO and SnO_2 targets with an off-axis-type RF magnetron sputter at room temperature. The sputtering was performed in an Ar and O_2 mixed-gas atmosphere and with 0.2 Pa chamber pressure. The PLs consisted of 9-nm-thick Al_2O_3 deposited via ALD using trimethyl aluminum (TMA) and water vapor, or TMA and oxygen plasma. All the patterning processes were performed using the photolithographic method and wet etching process. The annealing was performed at 300°C in a vacuum or O_2 atmosphere, using an electric oven. The electrical characteristics of the TFTs were measured with a semiconductor parameter analyzer (Agilent B1500A). The bias stabilities of the TFTs were measured with a semiconductor analyzer (HP 4145B). As the PL was basically deposited on the active layer before active patterning, the interface between the active layer and the gate insulator was not attacked by the chemical reactants used in photolithography and in the etching processes. The interface between the PL and the active layer is most important for the TFT channel characteristics. Two types of PL were prepared: one deposited at 200°C with water vapor as an oxygen precursor, and the other deposited at 200°C with oxygen plasma as an oxygen precursor. In each case, TMA was commonly used as an Al precursor. The active layers were deposited under the same sputtering chamber conditions but were annealed in two different atmospheres (oxygen and vacuum) at 300°C before PL deposition. Top-gate AZTO TFTs with Al_2O_3 first-gate insulators (FGIs) deposited via ALD at 200°C using the same processes and precursors as the PL were also prepared after active channel patterning and annealing. Active channel annealing was performed at 300°C in an oxygen or vacuum atmosphere, using an electric oven, before or after active patterning.

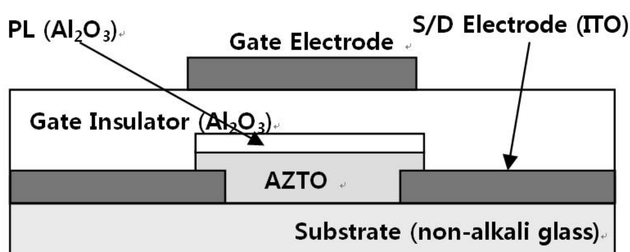

Fig. 1. Schematic diagram of the top-gate AZTO TFT.

3. Results and Discussion

The transfer characteristics of the AZTO TFTs with the PLs prepared through different processes are shown in the upper parts of Fig. 2-5, and the transfer curve shifts of the TFTs under +20 V gate bias stress are shown in the lower parts of the same figures. The AZTO TFTs annealed in O_2 and with water vapor PLs and those annealed in O_2 and with oxygen plasma PLs showed field effect mobilities (μ_{FET}) of 12.7 and 13.1 cm^2/Vs, subthreshold slopes (S/S) of 0.24 and 0.15 V/dec, and turn-on voltages (V_{on}) of -0.9 and -0.8 V, respectively. The AZTO TFTs annealed in vacuum and with water vapor PLs and those annealed in vacuum and with oxygen plasma PLs, on the other hand, showed 13.7 and 16.4 cm^2/Vs μ_{FET}, 0.57 and 0.18 V/dec S/S, and -8.5 and -0.2 V V_{on}, respectively. The mobilities and subthreshold slopes of the AZTO TFTs with oxygen plasma PLs were superior to those of the AZTO TFTs with water vapor PLs. The V_{on} values of the TFTs with oxygen plasma PLs were closer to 0 V compared to those of the TFTs with water vapor PLs. On the other hand, the V_{on} shifts (ΔV_{on}) under +20 V gate bias stress for 10,000 sec of the AZTO TFTs annealed in O_2 and with water vapor PLs and of those annealed in O_2 and with oxygen plasma PLs were 0.3 and 5.8 V, respectively. The V_{on} shifts of the TFTs annealed in vacuum and with water vapor PLs and of those annealed in vacuum and with oxygen plasma PLs were 0.3 and 8.9 V, respectively. The V_{on} shifts in the TFTs with water vapor PLs were very small. Contrary to the electrical characteristics, the bias stability of the TFTs with oxygen plasma PLs was relatively poor compared to that of the TFTs with water vapor PLs.

The mobilities and subthreshold slopes of the AZTO TFTs annealed in vacuum and with oxygen plasma PLs were better compared to those of the AZTO TFTs annealed in O_2 and with water vapor PLs, but the bias stability of the AZTO TFTs annealed in O_2 and with water vapor PLs was better than that of the AZTO TFTs annealed in vacuum and with oxygen plasma PLs. It is well known that S/S is dependent on the total trap density in the channel layer (N_{ss})

and at the interface (D_{it}), as follows:

$$S/S = \frac{qk_BT(N_{ss}t_{ch} + D_{it})}{C_i\log(e)}, \quad (1)$$

where q is the electron charge, k_B the Boltzmann's constant, T the absolute temperature, and t_{ch} the channel layer thickness.[15-16] The subthreshold slope is degraded with increasing active and interface traps; thus, the traps in the active layer and at the active/insulator interface were thought to be reduced in the case of the oxygen plasma PL. The S/S of the oxygen plasma PL was hardly affected by the pre-annealing process, but that of the water vapor PL was shown to be seriously dependent on the pre-annealing process. The oxygen plasma process is supposed to reduce the trap sites in the active layer and at the surface of active layer. The turn-on voltage became positive, with a positive gate bias, as shown in the lower parts of Fig. 2-5. The charge trapping at the insulator interface was found to be the main origin of the bias instability.[16-17] Therefore, the activation energy that carriers transmit over the interface and that are caught in the insulator is thought to be high in

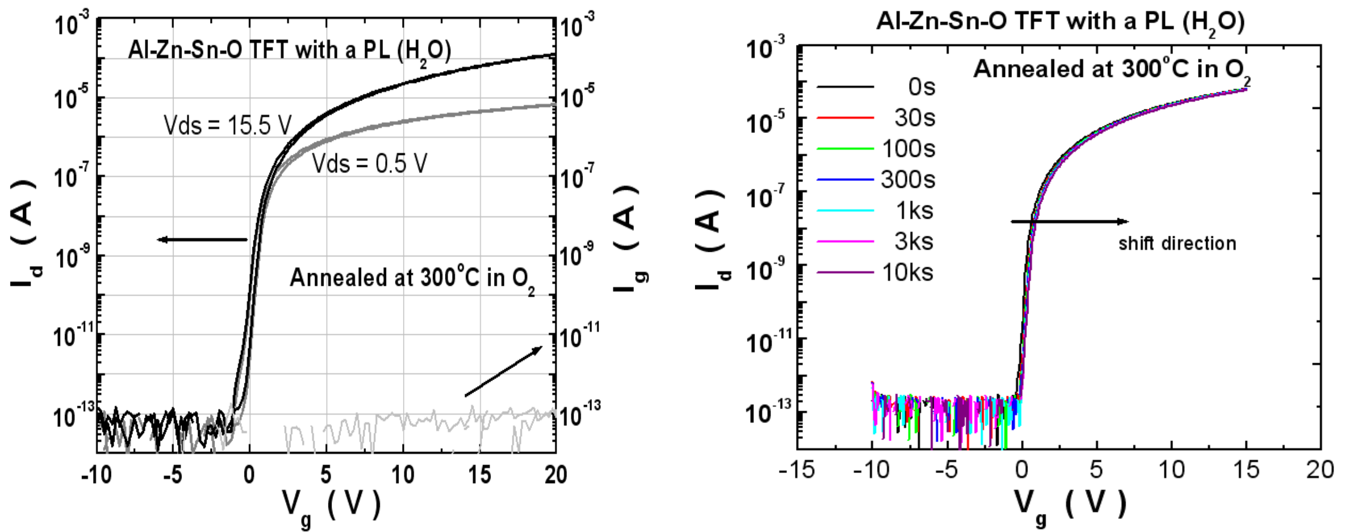

Fig. 2. Vg-Id characteristics (left) and transfer curve shifts (right) of the AZTO TFTs annealed in O_2 and with water vapor PLs.

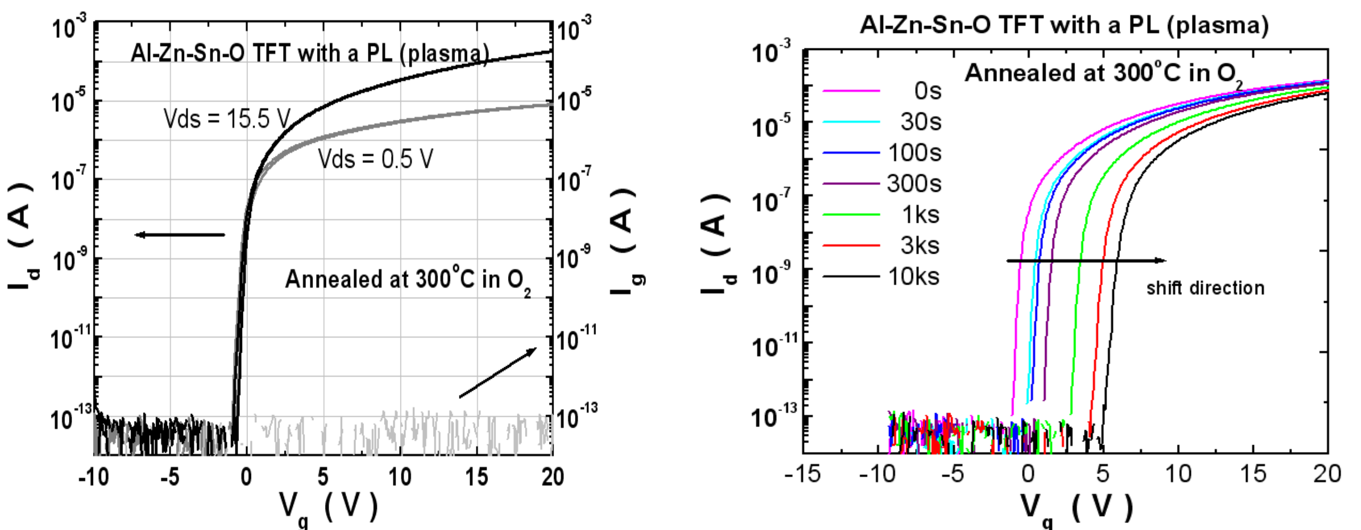

Fig. 3. Vg-Id characteristics (left) and transfer curve shifts (right) of the AZTO TFTs annealed in O_2 and with oxygen plasma PLs.

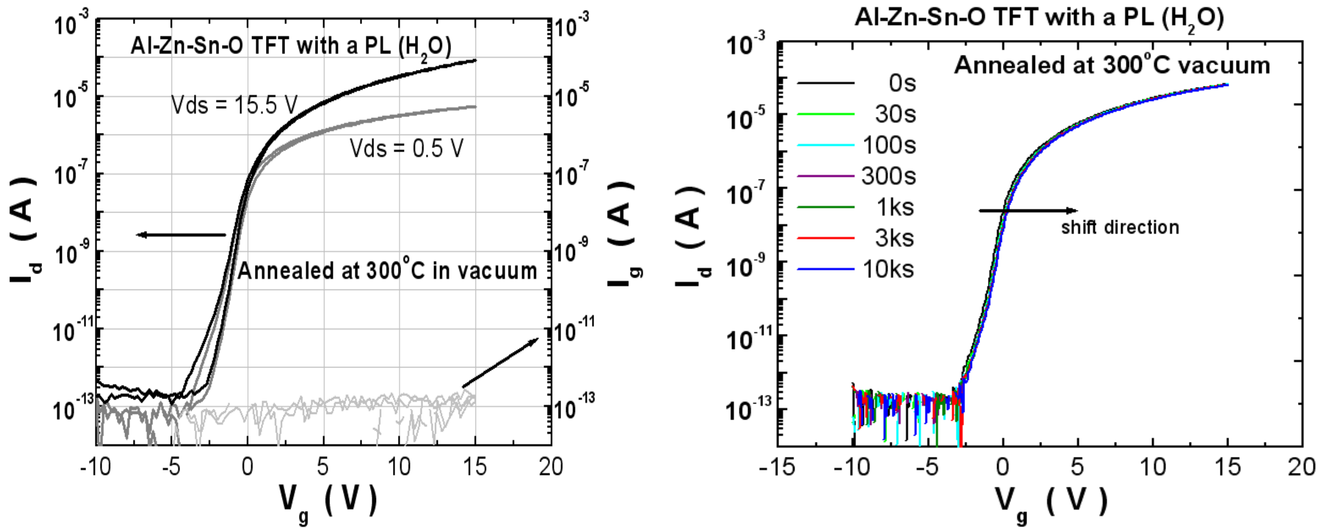

Fig. 4. Vg-Id characteristics (left) and transfer curve shifts (right) of the AZTO TFTs annealed in vacuum and with water vapor PLs.

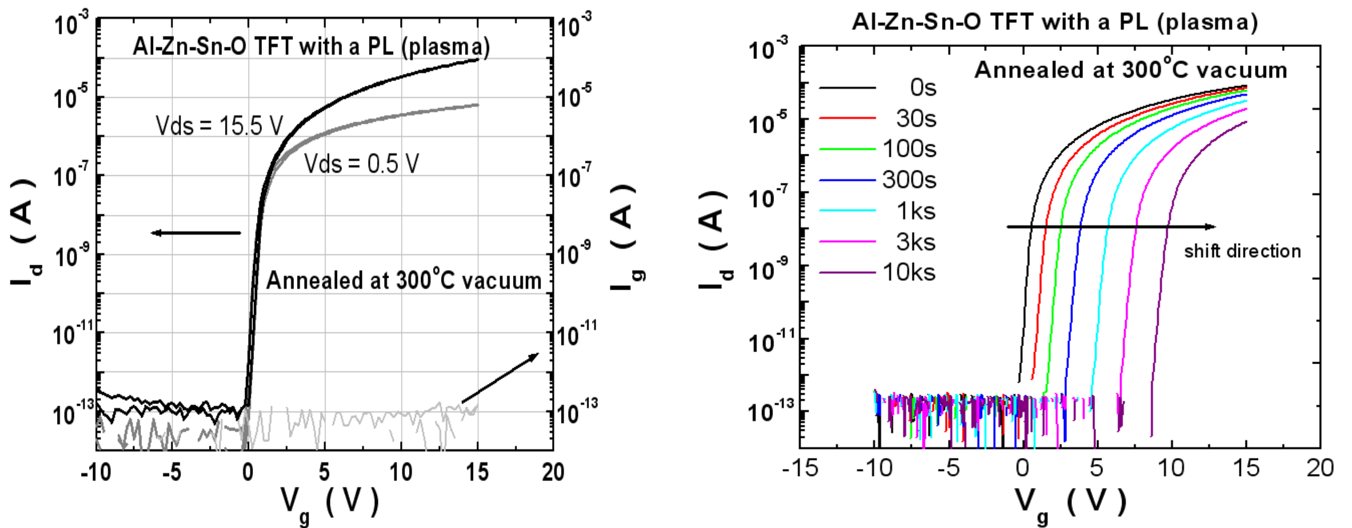

Fig. 5. Vg-Id characteristics (left) and transfer curve shifts (right) of the AZTO TFTs annealed in vacuum and with oxygen plasma PLs.

the case of the water vapor PL.[16] Based on the results of this study, it is considered that the water vapor PL increases the number of the active traps but suppresses the charge trapping at the insulator by the gate bias stress. The PL prepared through the water vapor process can thus be considered a more perfect insulator, with less insulator trap sites, than the oxygen plasma PL. Consequently, the charge trapping sites and mechanism causing bias instability are considered different from those causing subthreshold slope degradation for the top-gate AZTO TFTs.

The FGI effects were investigated and compared with the PL effects. The process and materials of the FGI were the same as those of the PL, but the FGI was deposited after active patterning. The μ_{FET} and the S/S at Vds=15.5 V and the Δ V_{on} under +20 V gate bias stress after 10 ks are summarized in Table 1. Both the mobility and the bias stability of the TFTs with FGIs were worse than those of the TFTs with PLs, as shown in Table 1. It was found that the active-patterning processes, such as photolithography, damage the active surface of the oxide TFTs and cause their electrical characteristics and bias stability to deteriorate. It is also very difficult to remove surface contamination, and surface contamination by chemicals can be fatally detrimental for the control of the TFT characteristics.

Table 1. μ_{FET}, S/S, and ΔV_{on} under +20 V gate bias after 10 ks of the AZTO TFTs with PLs and FGIs.

	After Patterning				Before Patterning			
	Vac Annealing		O_2 Annealing		Vac Annealing		O_2 Annealing	
	H_2O PL	Plsm PL	H_2O PL	Plsm PL	H_2O PL	Plsm PL	H_2O PL	Plsm PL
Mobility (cm^2/Vs)	7.2	9.8	3.3	8.4	13.7	16.4	12.7	13.1
S/S (V/dec)	5.1	0.13	6.2	0.15	0.57	0.18	0.24	0.15
Stability (ΔV_{on}, V)	0.5	14.3	0.6	14.1	0.3	8.9	0.3	5.8

The annealing of the active layer before PL deposition affected the final TFT characteristics. O_2 annealing before PL deposition was effective for the water vapor PL process but was not effective for the oxygen plasma PL process. The plasma process generally damages the channel surface,[18] but it can repair the damaged surface to improve the TFT characteristics in some cases.[19-20] As regards vacuum annealing and the FGI, the oxygen plasma process produced better effects on the electrical characteristics compared to the water vapor process. The oxygen plasma process cured the channel surface damaged by vacuum annealing or active patterning, and enhanced the mobility and subthreshold slope. On the other hand, the electrical characteristics of the O_2-annealed TFT were slightly degraded by the oxygen plasma process. Such process was thus found to degrade relatively perfect surfaces.

A 2.5-inch transparent AMOLED panel was successfully manufactured using a backplane with a stable top-gate AZTO TFT, as shown in Fig. 6. Its transmittance in the visible region was more than 60%. The TFT array of the backplane consisted of two transistors and one capacitor. It was annealed in an O_2 atmosphere and included a water vapor PL. The AMOLED specifications were QCIF+; 176 X 220, and monochrome.

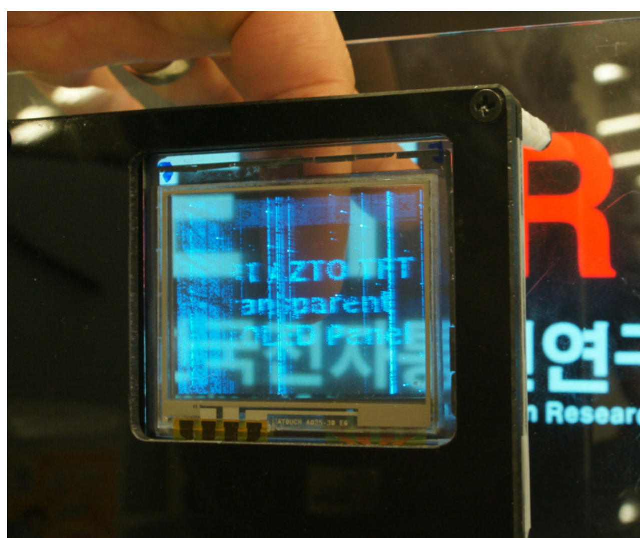

Fig. 6. AMOLED panel using the top-gate AZTO TFT backplane.

4. Summary

Stable AZTO TFTs with an active layer deposited at room temperature and processed at a low temperature were manufactured, and the origins of TFT characteristic change and bias instability were investigated using the different PL and active annealing processes. It was found that active-insulator interface control in the oxide TFT manufacturing process is very important for the improvement of the TFT characteristics and stability. The water vapor PL process after O_2 annealing was thought to be the best for the electrical characteristics and bias stability. The AZTO layer was deposited via sputtering, which is convenient for large-size commercial production. Room-temperature film deposition and low-temperature processing are significant advantages for the fabrication of flexible electronics. The AZTO TFT is considered an excellent candidate for application to large-size flexible displays and electronics with plastic substrates. The optimum conditions of its fabrication process are currently being developed for better performance, and its electrical characteristics are to be improved. The transparent 2.5-inch AMOLED panel driven by the AZTO TFT backplane prepared via a low-temperature process has also been manufactured.

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