A 2.4 /5.2-GHz Dual Band CMOS VCO using Balanced Frequency Doubler with Gate Bias Matching Network

Sung-Sun Choi, Han-Yeol Yu, and Yong-Hoon Kim

Abstract—**This paper presents the design and measurement of a 2.4/5.2-GHz dual band VCO with a balanced frequency doubler in 0.18 μm CMOS process. The topology of a 2.4 GHz VCO is a cross-coupled VCO with a LC tank and the frequency of the VCO is doubled by a frequency balanced doubler for a 5.2 GHz VCO. The gate bias matching network for class B operation in the balanced doubler is adopted to obtain as much power at 2nd harmonic output as possible. The average output powers of the 2.4 GHz and 5.2 GHz VCOs are -12 dBm and -13 dBm, respectively, the doubled VCO has fundamental harmonic suppression of -25 dB. The measured phase noises at 5 MHz frequency offset are -123 dBc /Hz from 2.6 GHz and -118 dBc /Hz from 5.1 GHz. The total size of the dual band VCO is 1.0 mm × 0.9 mm including pads.**

Index Terms—**CMOS, dual band, VCO, frequency doubler, gate bias matching network**

I. INTRODUCTION

The integrated multi-band RF transceiver has rapidly grown due to its convenience in many wireless applications. Until now, the multi-band RF systems for 2.4 GHz (2400~2483.5 MHz) and 5.2 GHz (5150~5350 MHz, 5725~5825 MHz) wireless local area network (WLAN) have been reported in [1-3]. Designing the multi-band RF transceiver using multiple terminals requires high cost by its large size. For minimal hardware implementtations, the suitable approach is to design the RF transceiver consisting of concurrent dual band circuits such as LNA, Mixer as shown in [1,2]. One of the major issues in the dual band RF system is the design of a dual band VCO. The dual band VCOs in the papers [1-3] were designed with a frequency divider, a switched resonator and a frequency doubler, respectively. The frequency divider method for the dual band VCO needs to design the VCO for higher frequency. However, as the frequency is higher, the quality factor of a LC tank is likely to decrease. It causes the degradation of the phase noise of the VCO. Another method using switched resonators is to convert the value of the capacitor or inductor in the LC tank using the switching transistors. Though the method makes the chip size of the dual band VCO smaller, the resistance of the switching transistors also causes the decreasing of the tank quality factor. The other method using a frequency doubler for the dual band VCO requires the VCO for lower frequency because the VCO for higher frequency can be achieved by using the frequency doubler. The method has the advantages of higher quality factor and lower power consumption of a divider in phase locked loop (PLL) with lower frequency band as the half frequency of the final frequency. So, this work concerns the design aspects of a dual band VCO utilizing a frequency doubler. We propose a fully integrated dual band VCO including a gate bias matching network in a balanced doubler for operation at 2.4 GHz ISM and 5.2 GHz UNII bands. The gate bias matching network in the doubler is used for class B operation to obtain much power at 2nd harmonic output. The proposed dual band VCO shown in Fig. 1 can be applicable to concurrent dual band (2.4 /5.2 GHz) systems as presented in Fig. 2.

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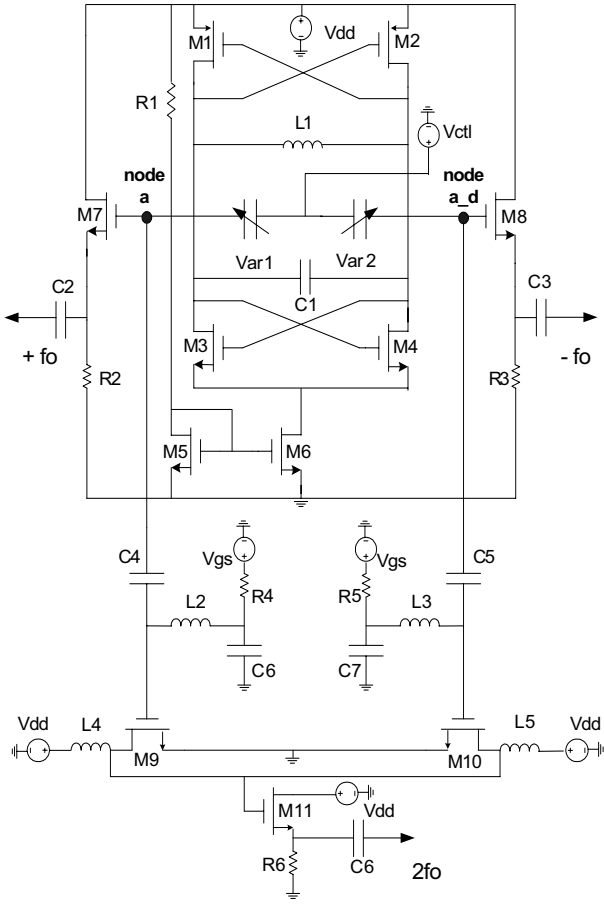


Fig. 1. Proposed 2.4 /5.2-GHz dual band VCO schematic.

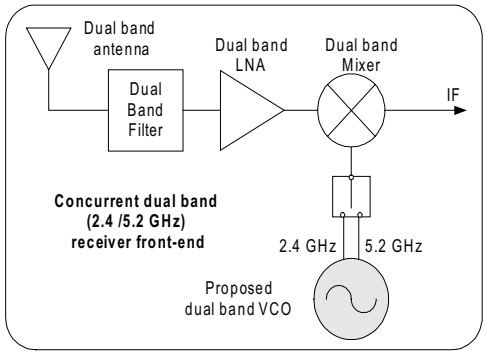


Fig. 2. Concurrent dual band (2.4 /5.2 GHz) receiver including proposed VCO.

II. VCO CIRCUITS DESIGN

1. 2.4 GHz VCO Circuit Design

The topology of the 2.4 GHz VCO is a cross-coupled VCO with a LC tank. The LC tank is composed of an inductor (L1), varactors (Var1 and Var2), a capacitor (C1) and parasitic capacitances of amplifier transistors (M1 ~ M4). The fixed MIM capacitor (C1) with high Q improves phase noise. The LC tank is difficult to maintain stable oscillation by itself due to the energy loss by the resistance of the LC tank. To overcome this, the complementary cross-coupled amplifiers (M1 ~ M4) are applied to the LC tank for providing a negative resistance and high transconductance (Gm). The output buffers (M7 and M8) are designed for driving the 50 ohm of the measurement equipment.

2. 5.2 GHz VCO Circuit Design

The frequency of the designed 2.4 GHz VCO is doubled by using the balanced doubler (M9 and M10) for the 5.2 GHz VCO. In the balanced doubler, the output power of the 2nd harmonic signal can be obtain owing to differential swing operation. At the output load of the balanced doubler, the odd harmonics are 180 degree out of phase and the even harmonics are in phase. So, the powers of the odd signals and even signals are cancelled and are added, respectively. The outputs of the 2.4 GHz VCO at node a and a_d in Fig. 1 are directly connected to the doubler without buffer amplifiers because of the current consumption affecting phase degradation [4].

In the circuit, we adopt the gate bias matching network which provides class B bias. By biasing the gate near the pinch off voltage (class B region), the doubler can generate as much power at the 2nd harmonic signal as possible [5]. The input impedance of the doubler including the gate bias part (Vgs) is designed about 50 ohm having adequate output power about 0 dBm at node a or a_d. The gate bias matching network is composed of capacitors, inductors, and resistors. These are used for dc blocking (C4 and C5), biasing for class B (L2 and L3), and RF shunt capacitance (C6 and C7). The resistors (R4 and R5) are implemented to prevent resonance probability between the RF shunt capacitance and the inductance of the dc probes [6]. The values of NMOS (M9 and M10) and the inductor loads (L4 and L5) are adequately selected for high gain. The output buffer (M11) is designed for isolating from a load circuit.

Compared with bipolar transistors, the device parameters of MOSFETs usually change widely according to process, supply voltage, and temperature (PVT) variations [7]. The Fig. 3 and Fig. 4 show the simulation results about the frequency and output power variations of the

proposed 5.2 GHz VCO according to PVT variations under worst (slow process, 1.62 V supply voltage, and 100 ° C temperature), typical (typical process, 1.8 V supply voltage, and 25 ° C temperature), and fast (fast process, 1.98 V supply voltage, and -40 ° C temperature) conditions, respectively. The Fig. 5 and Fig. 6 also show

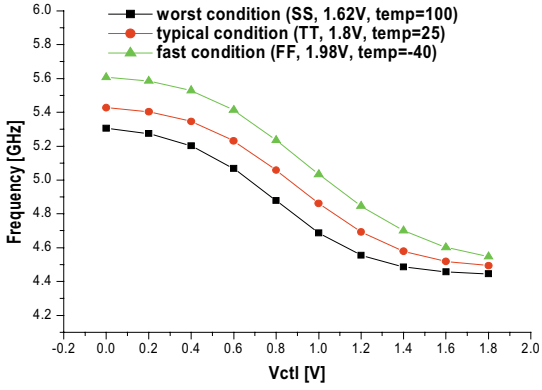


Fig. 3. 5.2 GHz VCO frequency variations according to PVT variations.

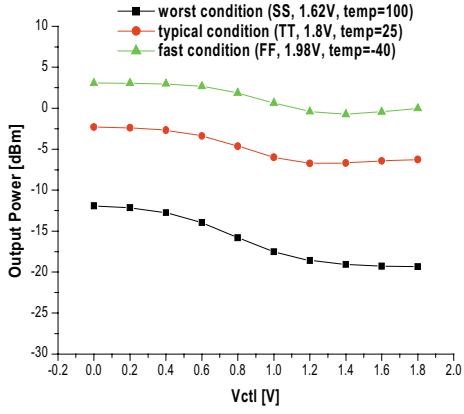


Fig. 4. 5.2 GHz VCO output power variations according to PVT variations.

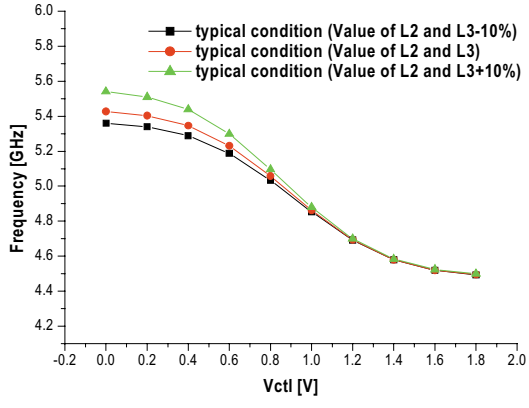


Fig. 5. 5.2 GHz VCO frequency variations according to L2 and L3 inductance variations.

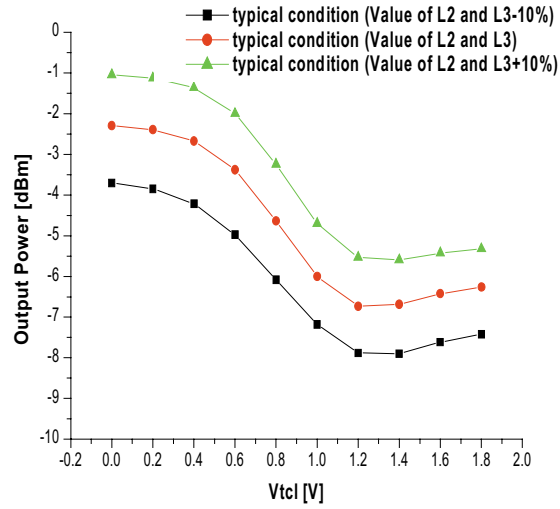


Fig. 6. 5.2 GHz VCO output power variations according to L2 and L3 inductance variations.

the simulation results about the frequency and output power variations according to the L2 and L3 inductance variations at gate bias of the frequency doubler under typical condition, respectively. The simulation results present that the frequency and output power of the proposed 5.2 GHz VCO are still sensitive by the variation of the gate bias due to the PVT variations and the L2 and L3 inductance variations. However, though the frequency and output power of the proposed 5.2 GHz VCO are some sensitive, the VCO can be solved by the help of the some control circuits like [7] and [8] to compensate the PVT variations.

III. Measurement Results

The photograph of the dual band VCO is shown in Fig. 7. Symmetric layout with low amplitude and phase error is considered for high harmonic suppression. The output ports of the VCO were measured using the E4407B spectrum analyzer.

The total current of the dual band VCO including buffers is 25 mA from 1.8 V power supply. The core currents of the 2.4 GHz and 5.2 GHz VCOs are 4 mA and 5.2 mA, respectively. The 2.4 GHz VCO tuning range is 2.68 ~ 2.20 GHz (19 %) with -11.43 ~ -12.44 dBm output power as shown in Fig. 8. And the 5.2 GHz VCO tuning range is 5.35 ~ 4.42 (19 %) with -8.2 ~ -17 dBm output power as shown in Fig. 9. The Fig. 10 presents the output power spectrum of the 5.26 GHz VCO with -25 dB fundamental suppression. The Fig. 11

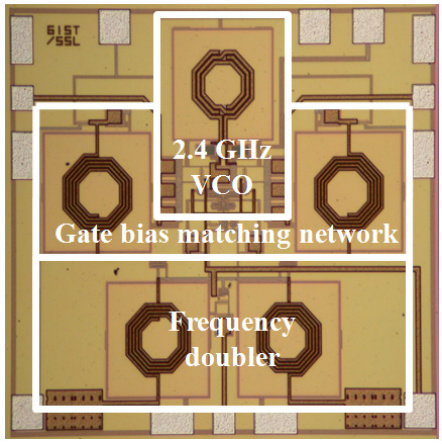


Fig. 7. Dual band VCO photograph ($1.0mm \times 0.9mm$).

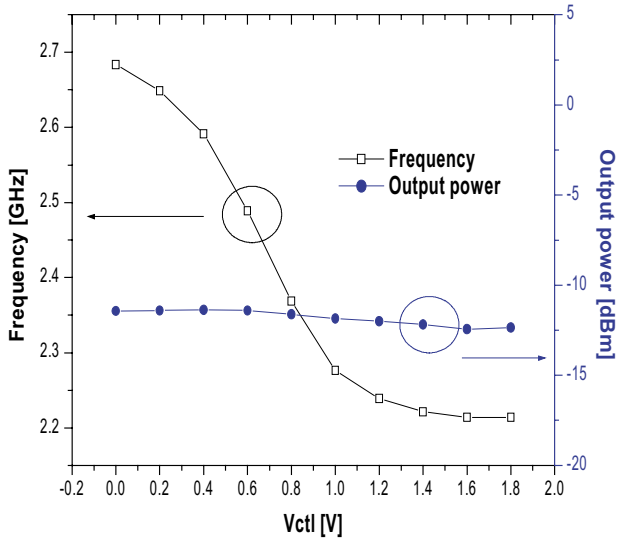


Fig. 8. 2.4 GHz VCO tuning range and output power at Vgs of 0.5 V.

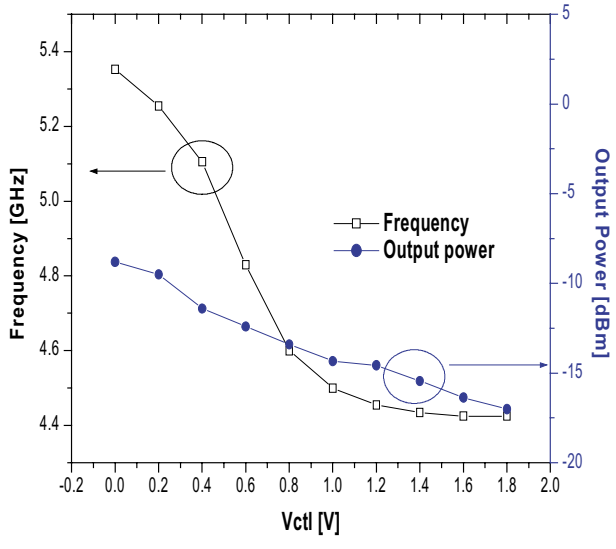


Fig. 9. 5.2 GHz VCO tuning range and output power at Vgs of 0.5 V.

shows the measured output power of the 5.35 GHz VCO and fundamental harmonic suppression according to the gate bias (Vgs) of the doubler under Vctl of 0 V. The measured optimum gate bias voltage to obtain the maximum 2nd output power is about 0.5 V. But, the output power of the 5.35 GHz VCO has about 6 dB difference between the simulation and measurement. The difference mainly causes by PVT variations, non-simulated inter-connection line loss, amplitude and phase error by the non-perfected symmetric layout, unstable Vdd power probing contact, and loss by assembly. The measured phase noise of 2.594 /5.086 GHz VCOs are shown in Fig. 12.

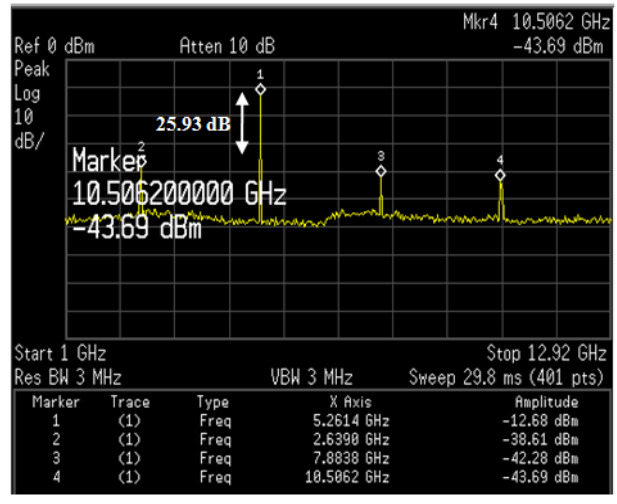


Fig. 10. 5.26 GHz VCO output power spectrum at span 12 GHz.

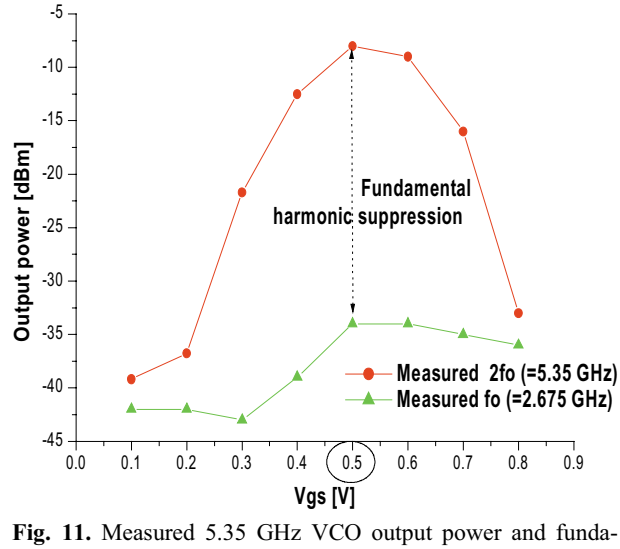
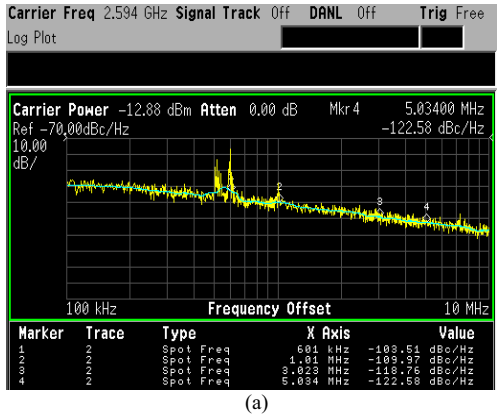
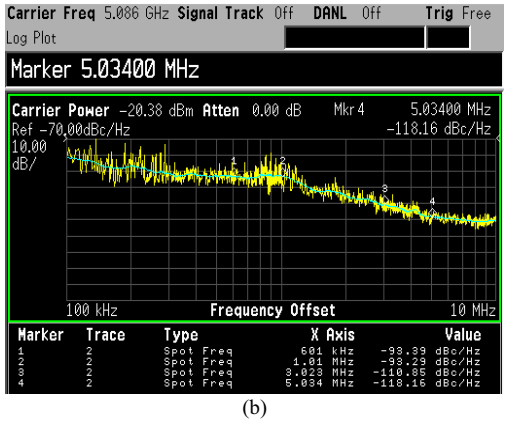


Fig. 11. Measured 5.35 GHz VCO output power and fundamental suppression according to Vgs under Vctl of 0 V.



(a)



(b)

Fig. 12. (a) Measured phase noise of 2.594 GHz VCO. (b) Measured phase noise of 5.086 GHz VCO.

The phase noises of the 2.594 GHz VCO are -119 and -123 dBc/Hz at 3 and 5 MHz offset frequency, respectively. And the phase noises 5.086 GHz VCO are -111 and -118 dBc/Hz at 3 and 5 MHz offset frequency, respectively. The phase noise of the 5.0 GHz VCO using the frequency doubler is about 6~8 dB worse than that of the 2.5 GHz VCO as expected in theoretical calculation. The dual band VCO performances were compared to the published dual band VCOs with frequency doubler and 5 GHz doubler in Table 1. The widely-used FoM for VCOs is defined as

$$FoM = L\{\Delta f\} - 20\log(\frac{f_0}{\Delta f}) + 10\log(\frac{P_{dc}}{1mW}) \qquad (1)$$

where, $L\{\triangle f\}$ is SSB phase noise measured at the offset frequency of $\triangle f$ from the oscillation frequency of f_o, and P_{dc} represents DC power dissipation in mW. As shown in Table 1, the proposed VCO has reasonable output power and good fundamental harmonic suppression.

Table 1. Comparison of the published DVCOs and frequency doubler

Ref.	This work	[9]	[10]	[11]
Circuit	DVCO*	DVCO*	DVCO*	Doubler
CMOS Tech.	0.18 μm	0.35 μm	0.18 μm	0.18 μm
Vdd [V]	1.8	2.0	1.8	1.8
Freq. [GHz]	2.4/5.2	2.3/4.6	2.4/5.2	5
Phase noise [dBc/Hz]	-123 /-118 @ 5 MHz	-112.2 /-98.38 @ 5 MHz	-135 /-126 @ 3 MHz	--/--
Fund. Supp. [dB]	<-25	--	--	<-20
P_{OUT} (average) [dBm]	-12 /-13	-10 /-25	0 / -11	--/--
Core P_{DC} (mW)	7.2/9.36	8/-	5.4/ 8	-
Total P_{DC} (mW)	45 (with buffer)	53 (with buffer)	-	18 (with buffer)
Size (mm^2)	0.9	-	0.4	-
FoM (dBc/Hz)	-168.73 /-168.44	-156.54 /	-188.3/ -183.7	-

*DVCO : dual band VCO

V. CONCLUSIONS

This paper presents a dual band VCO using 0.18 μm CMOS process. We propose that by using the frequency doubler with the gate matching network, the VCO can operate at both 2.4 and 5.2 GHz bands with reasonable output power and high fundamental harmonic suppression. The proposed VCO will be fit for a dual-band RF system for 2.4 GHz and 5.2 GHz.

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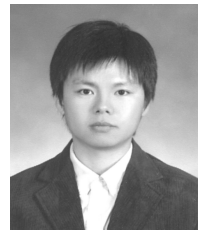

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