Symmetric and Asymmetric Double Gate MOSFET Modeling

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***Abstract*—An analytical compact model for the asymmetric lightly doped Double Gate (DG) MOSFET is presented. The model is developed using the Lambert Function and a 2-dimensional (2-D) parabolic electrostatic potential approximation. Compact models of the net charge and channel current of the DG-MOSFET are derived in section 2. Results for the channel potential and current are compared with 2-D numerical data for a lightly doped DG MOSFET in section 3, showing very good agreement.**

***Index Terms*—Device modeling, compact model, D G- MOSFET, circuit simulation**

I. INTRODUCTION

The semiconductor industry is able to achieve better electronics performance by shrinking transistors and putting more of them on to a chip. The silicon device technology faces a problem when the device scales down to nanometer channel length. Shrinking the MOSFET structure further causes an increase in short channel effects and the result is wasted power and heat. The DG-MOSFET has potential to overcome this short channel problem, [1]. Taur and Lu, [2-4,12], have derived expressions for the I-V characteristics for the symmetric and undoped DG-MOSFET device. The surface potential, channel charge and current models that were obtained in [2-4,12] require the solution of a transcendental equation (see equation (22) in Appendix A). In [5,6], this transcendental equation is solved *iteratively* with very fast convergence for circuit simulation application.

Most of the published compact modeling work is focused on symmetric and undoped DG-MOSFET devices (see [2-6, 10-13]), whereas real devices are lightly doped, about 10^{15} cm^{-3}, and *asymmetric*. In the numerical simulation of [14] it is shown that even a small doping density of 10^{15} cm^{-3} could cause a large shift in the surface potential. From the compact modeling point of view a *milli-volt* error in the surface potential is not acceptable. There are a limited number of asymmetric DG-MOSFET models in the literature such as [12, 13]. Although the real device asymmetry is due to different oxide thicknesses, flatband voltages and applied gate voltages at the two input gate terminals, most of the compact models usually consider the asymmetry arises only from different flatband voltages and oxide thicknesses at the two gates. In this paper, for asymmetric devices, we consider light channel doping density and different applied gate voltages in addition to different flatband voltages and oxide thicknesses.

The analytical *symmetric* and *asymmetric* lightly doped DG-MOSFET device compact model proposed here improves the compact model accuracy for circuit simulation application without any *iteration*. We consider a DG-MOSFET which has the geometry shown in Fig. 1. A parabolic electrostatic potential approximation across the device is assumed that is similar to [7]. Our compact

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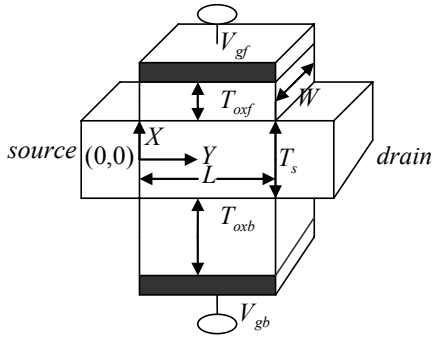

Fig. 1. The structure of asymmetric DG-MOSFET.

model is compared with 2-D numerical data [9] in section 3.

II. COMPACT DEVICE MODEL

The 2-D Poisson equation for the electrostatic potential $\psi(X,Y)$ in uniformly doped silicon is

$$\frac{d^2\psi}{dX^2}+\frac{d^2\psi}{dY^2}=\frac{q}{\varepsilon_s}\left(n_i e^{q(\psi-V)/kT}+N_a\right) \tag{1}$$

where the electron density is $n=n_i e^{(\psi-V)/V_{th}}$ A complete list of symbols used in this paper is given in Appendix B. The continuity of the electric displacement at the silicon/silicon-oxide interfaces gives the boundary conditions as

$$\begin{aligned}\varepsilon_s\frac{\partial\psi}{\partial X}\Big|_{X=\frac{T_s}{2}}&=\varepsilon_{ox}\left(\frac{V_{gf}-\psi_{sf}-\Delta\phi}{T_{oxf}}\right),\\ \varepsilon_s\frac{\partial\psi}{\partial X}\Big|_{X=\frac{-T_s}{2}}&=-\varepsilon_{ox}\left(\frac{V_{gb}-\psi_{sb}-\Delta\phi}{T_{oxb}}\right)\end{aligned} \tag{2}$$

Using the scaled variables below, the Poisson equation (1) is rewritten as

$$\frac{\partial^2 w}{\partial x^2}+\varepsilon^2\frac{\partial^2 w}{\partial y^2}=\frac{1}{\lambda}e^{(w-v)\ln\lambda}+1 \tag{3}$$

where $\varepsilon=\frac{L_d}{L}\sqrt{\ln\lambda/\lambda}$, $L_d=\sqrt{\frac{V_{th}\varepsilon_s}{n_i q}}$ is the intrinsic Debye length, $\lambda=N_a/n_i$, $X=xL_d\sqrt{\ln\lambda/\lambda}$, $Y=yL$ and $(\psi,V,\phi)=(w,v,\varphi)V_{th}\ln\lambda$

In this paper dimensional voltages and lengths, such as V_{gf} and T_s, are denoted by capital letters. Lower-case letters, v_{gf} and t_s, are used to denote the same quantities non-dimensionalised. Exact analytical solutions to (3) are not available. However, a numerical solution of (3) indicates that a parabolic potential approximation in x is a good approximation for low voltage application. A parabolic potential form in x has been used in [7] to model sub-threshold swing. Here we assume the form

$$w(x,y)=w_0(y)+b(y)x+c(y)x^2 \tag{4}$$

where $w_0(y)$ is the scaled potential along the mid-section, $x=0$.

Using the boundary conditions (2), (3) and (4) give

$$\begin{cases}b=\dfrac{\varepsilon_{ox}}{2\varepsilon_s}\left(\dfrac{v_{gf}-w_{sf}-\Delta\varphi_f}{t_{oxf}}-\dfrac{v_{gb}-w_{sb}-\Delta\varphi_b}{t_{oxb}}\right)\\ c=\dfrac{\varepsilon_{ox}}{2t_s\varepsilon_s}\left(\dfrac{v_{gf}-w_{sf}-\Delta\varphi_f}{t_{oxf}}+\dfrac{v_{gb}-w_{sb}-\Delta\varphi_b}{t_{oxb}}\right)\end{cases} \tag{5}$$

where the surface potentials are given by,

$$w_{sf}=w_0+b\frac{t_s}{2}+c\frac{t_s^2}{4},\ w_{sb}=w_0-b\frac{t_s}{2}+c\frac{t_s^2}{4} \tag{6}$$

Explicit solutions can be calculated for w_{sf} and w_{sb} from (6):

$$\begin{cases}w_{sf}=\dfrac{\gamma_{sf}w_0k_{1b}+(V_{gf}-\Delta\varphi_f)k_{2f}+(V_{gb}-\Delta\varphi_b)k_{3b}}{k_{4f}}\\ w_{sb}=\dfrac{\gamma_{sb}w_0k_{1f}+(V_{gb}-\Delta\varphi_b)k_{2b}+(V_{gf}-\Delta\varphi_f)k_{3f}}{k_{4b}}\end{cases} \tag{7}$$

where, γ_s is the surface potential correction factor and it is used as a fitting parameter with numerical data,

$$k_{1i}=1+\frac{t_s\varepsilon_{ox}}{8\varepsilon_s t_{oxi}+3t_s\varepsilon_{ox}} \tag{8}$$

$$k_{2i}=\frac{3t_s\varepsilon_{ox}}{8\varepsilon_s t_{oxi}}-\frac{t_s^2\varepsilon_{ox}^2}{64\varepsilon_s^2 t_{oxf}t_{oxb}+24t_s\varepsilon_s\varepsilon_{ox}t_{oxi}} \tag{9}$$

$$k_{3i}=\frac{3t_s^2\varepsilon_{ox}^2}{64\varepsilon_s^2 t_{oxi}^2+24\varepsilon_s\varepsilon_{ox}t_s t_{oxi}}-\frac{t_s\varepsilon_{ox}}{8\varepsilon_s t_{oxi}} \tag{10}$$

$$k_{4i} = 1 + \frac{3t_s\varepsilon_{ox}}{8\varepsilon_s t_{oxi}} - \frac{t_s^2\varepsilon_{ox}^2}{64\varepsilon_s^2 t_{oxf}t_{oxb} + 24\varepsilon_s\varepsilon_{ox}t_s t_{oxi}} \quad (11)$$

The mid-section electrostatic potential, $w_0(y)$, is determined from the ordinary differential equation:

$$\varepsilon^2\frac{d^2w_0}{dy^2} + Ew_0 - \frac{1}{\lambda}e^{(w_0-v)\ln\lambda} + K = 0 \quad (12)$$

where

$$E = -\frac{\varepsilon_{ox}}{\varepsilon_s t_s}\left(\frac{k_{1b}}{k_{4f}t_{oxf}} + \frac{k_{1f}}{k_{fb}t_{oxb}}\right) \quad (13)$$

$$K = \frac{\varepsilon_{ox}}{\varepsilon_s t_s}\left[\left(\frac{v_{gf}-\Delta\varphi_f}{t_{oxf}} + \frac{v_{gb}-\Delta\varphi_b}{t_{oxb}}\right) - \frac{(v_{gf}-\Delta\varphi_f)k_{2f} + (v_{gb}-\Delta\varphi_b)k_{3b}}{k_{4f}t_{oxf}} - \frac{(v_{gb}-\Delta\varphi_b)k_{2b} + (v_{gf}-\Delta\varphi_f)k_{3f}}{k_{4b}t_{oxb}}\right] - 1 \quad (14)$$

The second derivative terms $b''x$ and $c''x^2$ are neglected in (12); this equation is approximated by its behavior at the mid-section, $x=0$. The long channel approximation of the mid-section potential can be determined from (12) by taking $\varepsilon^2 \to 0$, which gives

$$w_0^* = -\frac{lambertW\left(-\frac{\ln\lambda}{\lambda E}e^{\left(-\frac{K}{E}-v\right)\ln\lambda}\right)}{\ln\lambda} - \frac{K}{E} \quad (15)$$

where W is the *Lambert function*, see [8]. We adopt $w_0 \to w_0^*/\alpha$, where α is a correction factor that is introduced to account for changes in the mid-section potential due to the parabolic potential approximation and 2-D effect.

$$\alpha = \alpha_0 + \frac{1}{l}(\alpha_1 + \alpha_2 v_{ds}) \quad (16)$$

where l and v_{ds} are the scaled dimensionless channel length and drain voltage respectively, α_i are used as fitting parameters with the numerical data and α has a very weak dependence on the drain voltage.

The total mobile charge per unit gate area for the asymmetric DG MOSFET is given by

$$Q(V) = \varepsilon_{ox}\left(\frac{V_{gf}-\psi_{sf}-\Delta\phi_f}{T_{oxf}} + \frac{V_{gb}-\psi_{sb}-\Delta\phi_b}{T_{oxb}}\right) \quad (17)$$

and the channel current is then expressed as

$$I_{ds} = \frac{\mu W}{L}\int_0^{V_{ds}}Q(V)dV = \frac{\mu W\varepsilon_{ox}}{L}\left\{\begin{array}{l}\left(\frac{V_{gf}-\Delta\phi_f}{T_{oxf}}\right)V_{ds} - \frac{(V_{gf}-\Delta\phi_f)k_{2f}V_{ds}}{k_{4f}} \\ -\frac{(V_{gb}-\Delta\phi_b)k_{3b}V_{ds}}{k_{4f}} + \frac{(V_{gb}-\Delta\phi_b)V_{ds}}{T_{oxb}} \\ -\frac{(V_{gb}-\Delta\phi_b)k_{2b}V_{ds} + (V_{gf}-\Delta\phi_f)k_{3f}V_{ds}}{k_{4b}} \\ -\left(\frac{k_{1b}}{T_{oxf}k_{4f}} + \frac{k_{1f}}{T_{oxb}k_{4b}}\right)\int_0^{V_{ds}}\psi_0^*dV\end{array}\right\} \quad (18)$$

where,

$$\int_0^{V_{ds}}\psi_0^*dV = \frac{-(V_{th}K\ln\lambda)V_{ds}}{E} + V_{th}^2\left[lambertW\left(\frac{\ln\lambda}{\lambda E}e^{\left(\frac{K\ln\lambda}{E}\frac{V_{ds}}{V_{th}}\right)}\right) - lambertW\left(\frac{\ln\lambda}{\lambda E}e^{\left(\frac{K\ln\lambda}{E}\right)}\right) + \frac{lambertW^2\left(\frac{\ln\lambda}{\lambda E}e^{\left(\frac{K\ln\lambda}{E}\frac{V_{ds}}{V_{th}}\right)}\right)}{2} - \frac{lambertW^2\left(\frac{\ln\lambda}{\lambda E}e^{\left(\frac{K\ln\lambda}{E}\right)}\right)}{2}\right]$$

Equation (18) above is applicable for both *symmetric* and *asymmetric* devices.

III. RESULTS AND CONCLUSIONS

In this section, symmetric device characteristics with the same front and back gate voltage V_{gs} are shown in Fig. 2-5. Solid lines show our compact model results and the circles are numerical simulation results from [9]. Our compact modeling comparison in Fig. 2-5 with the numerical data give excellent results. One of the advantages of our compact models is that it includes the channel doping density. The work in [14] indicates that the *undoped* assumption of the DG-MOSFET device channel is unsatisfactory. Even though doping of the DG-MOSFET is not desired and usually not used, there is always small unintentional doping density, ~10^{15} cm^{-3}, during fabrication [14].

The major advantages of our compact models are that it accounts for asymmetry due to different oxide thicknesses, flatband voltages and applied gate voltages at the two gate terminals. For all simulation results in this section a zero work function difference or flat band voltage is assumed.

Now we present results for our compact model together with comparisons for 2-D numerical I-V

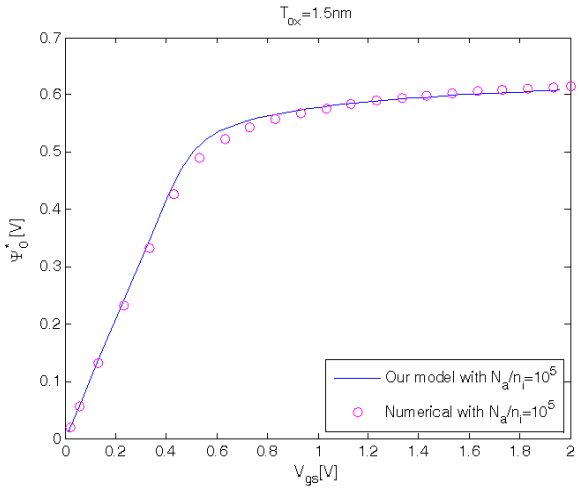

Fig. 2. Mid-section potential versus relative gate voltage at 5 nm silicon thickness and zero quasi-Fermi potential with, α0=0.96.

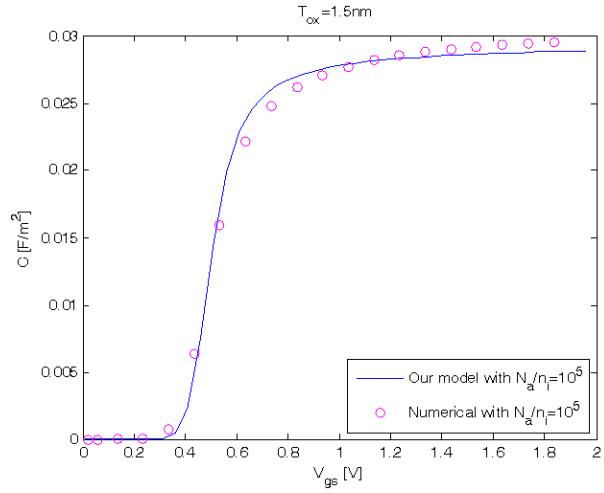

Fig. 5. Gate capacitance versus relative gate voltage at 5 nm silicon thickness and zero quasi-Fermi potential with α_0=0.96 and γ_s=0.768.

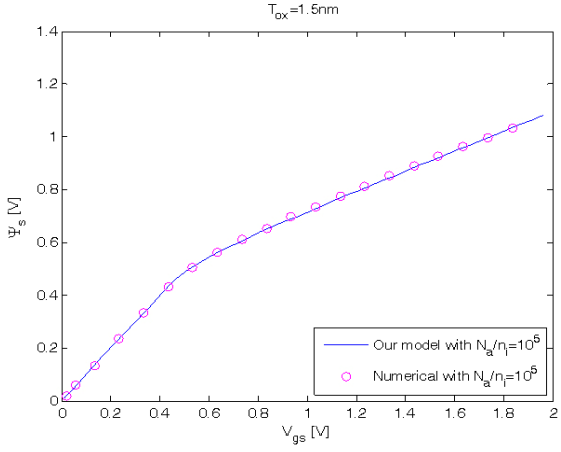

Fig. 3. Surface potential versus relative gate voltage at 5 nm silicon thickness and zero quasi-Fermi potential with α0=0.96 and γs=0.768.

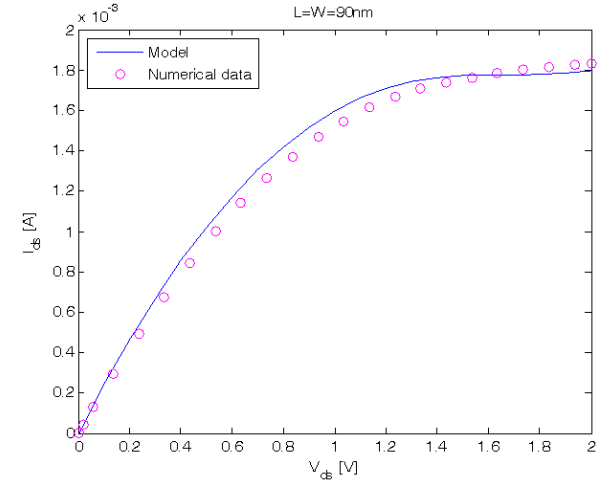

Fig. 6. Channel current versus source-drain voltage at 5 nm silicon thickness, α_0=0.96, α_1=O(10^{-2}), α_2=O(10^{-4}), 1.5 nm oxide thicknesses and V_{gs}=2 V (lightly doped, N_a/n_i=10^5, symmetric DG-MOSFET).

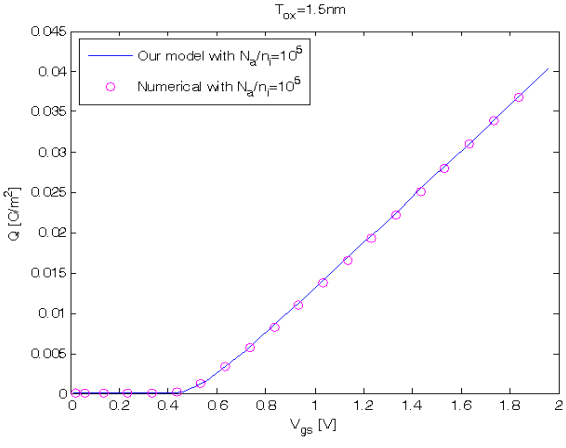

Fig. 4. The total channel charge density versus relative gate voltage at 5 nm silicon thickness and zero quasi-Fermi potential with α_0=0.96 and γ_s=0.768.

simulation. Fig. 6-9 show the symmetric device and Fig. 10 shows the asymmetric device simulations. Our simulation of the asymmetric device in Fig. 10 at a -1 V back gate bias indicates that the model gives a good approximation in the linear region. However, its accuracy deteriorates rapidly out of the linear region as saturation takes over. We believe this inaccuracy is due to our parabolic potential approximation. We also observed that the 2-D effect correction factor α has strong gate voltage dependence for the asymmetric device but has negligible channel length dependence in the linear region, see Table 1 and Fig. 10. Modeling these effects in the weak

inversion and saturation regions of the asymmetric device requires further study, and the derivation of (17) and (18) may have to be modified (work in progress.)

The numerical simulations of *I–V* characteristics for 2–D symmetric and asymmetric DG MOSFETs are determined by solving Poisson's equation and the electron continuity equation, as well as the drift–diffusion equation without considering quantum effects using the Sentaurus Device Simulator [9]. The temperature is fixed at 300 K without self-heating effects and the bandgap narrowing is ignored to simplify the intrinsic carrier concentration n_i as a function of bandgap energy. The drain current is assumed to be carried only by the electrons.

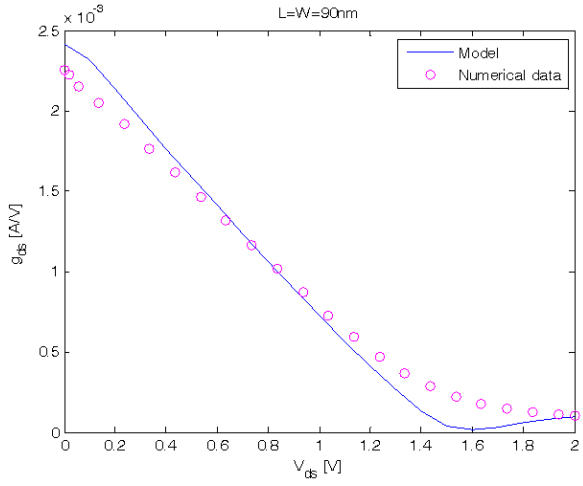

Fig. 7. Output conductance versus source-drain voltage at 5 nm silicon thickness, α_0=0.96, α_1=O(10^{-2}), α_2=O(10^{-4}), 1.5 nm oxide thicknesses and V_{gs}=2 *V* (lightly doped, $N_a/n_i=10^5$, symmetric DG-MOSFET).

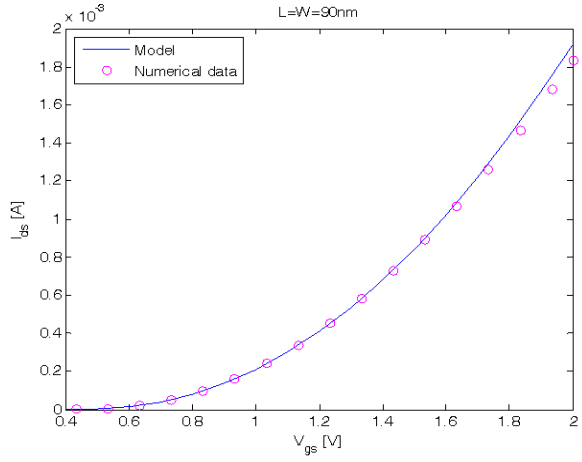

Fig. 8. Channel current versus gate voltage at 5 nm silicon thickness, α_0=0.96, α_1=O(10^{-2}), α_2=O(10^{-4}), V_{ds}=2 *V* and 1.5 nm oxide thicknesses (lightly doped, $N_a/n_i=10^5$, symmetric DG-MOSFET).

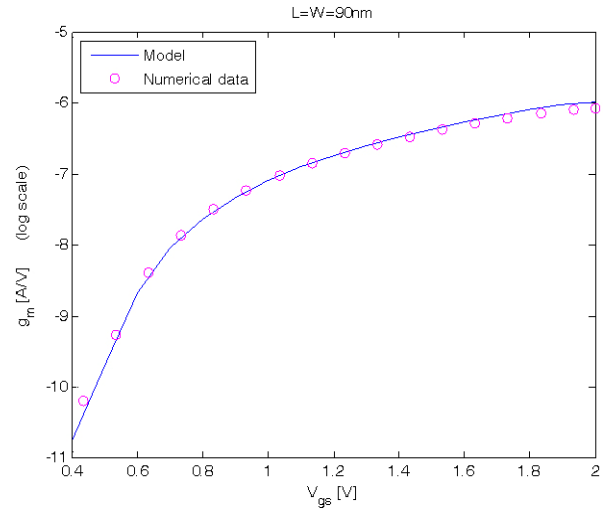

Fig. 9. Transconductance versus gate voltage at 5 nm silicon thickness, α_0=0.96, α_1=*O*(10^{-2}), α_2=*O*(10^{-4}), V_{ds}=2 *V* and 1.5 nm oxide thickness (lightly doped, $N_a/n_i=10^5$, symmetric DG-MOSFET).

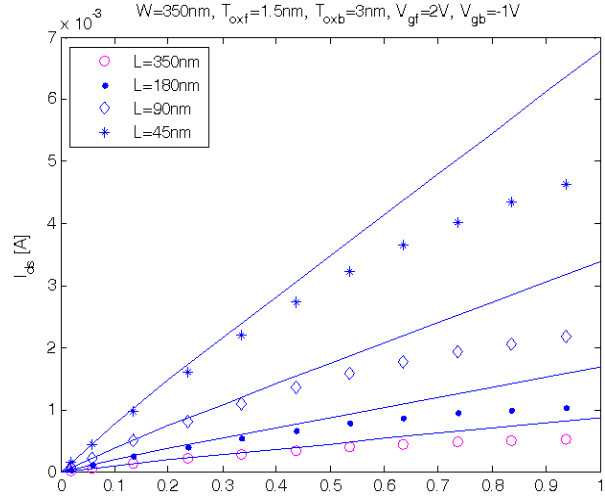

Fig. 10. Asymmetric DG-MOSFET channel current versus source-drain voltage in linear region at 20 nm silicon thickness and α_0=1.25, α_1=*O*(10^{-2}), α_2=*O*(10^{-4}).

Table 1. The first order mid-section potential correction factor dependence for asymmetric device with front gate voltage for V_{gb}=-1 V

V_{gf} (V)	α_0
1	2.5
1.5	1.5
2	1.25

APPENDIX A

The 1-D Poisson equation for undoped symmetric DG-MOSFET,

$$\frac{d^2\psi}{dX^2} = \frac{q}{\varepsilon_s}\left(n_i e^{q(\psi - V)/kT}\right) \tag{19}$$

In scaled variables (18) becomes

$$2\frac{d^2 w}{dx^2} = e^{(w-v)} \tag{20}$$

with the scaling: $(\psi, V) = (w, v)V_{th}$, $X = xL_D$ and $L_D = \sqrt{\frac{V_{th}\varepsilon_s}{2n_i q}}$

In (20), w, v are the scaled electrostatic and quasi-Fermi potentials, respectively, with v being dependent only on the source-to-drain coordinate, y, and governed by the standard drift-diffusion law. The solution to (20) is:

$$w(x) = v + w_0 - 2\ln(\cos(e^{w_0/2}x/2)) \tag{21}$$

where w_0 represents the minimum value of w at $x = 0$. The boundary condition at the oxide/silicon interface yields the transcendental equation

$$v_{gs} - \Delta\varphi - v = 2\ln(c_1\theta\sec(\theta)) + c_2\theta\tan(\theta) \tag{22}$$

where v_{gs} is the scaled gate voltage and θ, c_1, c_2 are defined by $\theta = \frac{1}{4}e^{w_0/2}t_s$, $c_1 = 4\frac{L_d}{T_s}$, $c_2 = 4\frac{\varepsilon_s}{\varepsilon_{ox}}\frac{T_{ox}}{T_s}$

APPENDIX B

List of symbols:

q represents electron charge,

ε_s, ε_{ox} semiconductor, silicon-oxide permittivities,

T_s silicon thickness,

T_{oxf}, T_{oxb} front, back oxide thicknesses,

L, W channel length, width,

X direction perpendicular to the channel at the mid-section,

Y direction along the channel from the source end,

n_i intrinsic density,

N_a silicon doping,

k Boltzmann constant,

T temperature,

μ constant electron mobility of 400 cm^2/Vs,

ψ electrostatic potentials,

V_{gf}, V_{gb} front, back gate voltages,

ψ_{sf}, ψ_{sb} front, back gate surface potentials,

$V_{th} = kT/q$ thermal voltage,

$\Delta\phi_f$, $\Delta\phi_b$ front, back gate work function differences or flat band voltages,

V_{gs} gate voltage relative to the flat band voltage for a symmetric device,

V quasi-Fermi potential, where $V=0$ at the source, $V=V_{ds}$ at the drain.

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Research activities include the development of wafer level reliability and quality assurance procedures, and CMOS semiconductor device modeling. The CMOS device modeling work is aimed at improving the accuracy of CMOS SPICE circuit simulations with deep-submicrometer feature size transistors. The research investigating physical wear-out models is intended for use in the implementation of reliability simulation of new IC designs. In addition, he is responsible for the technical interaction between MOSIS and the fabrication contractors in areas of new technology interfaces. Mr. Tyree received the MSEE degree from the University of California, Berkeley.

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