Temperature Stable Current Source Using Simple Self-Bias Circuit

Jin-Ho Choi, *Member, KIMICS*

Abstract— In this paper, temperature stable current and voltage references using simple CMOS bias circuit are proposed. To obtain temperature stable characteristics of bias circuit a bandgap reference concept is used in a conventional circuit. The parasitic bipolar transistors or MOS transistors having different threshold voltage are required in a bandgap reference. Thereby the chip area increase or the extra CMOS process is required compared to a standard CMOS process. The proposed reference circuit can be integrated on a single chip by a standard CMOS process without the extra CMOS process. From the simulation results, the reference current variation is less than ±0.44% over a temperature range from -20℃ to 80℃. And the voltage variation is from -0.02% to 0.1%.

Index Terms— temperature stable, current source, voltage source, reference circuit.

I. INTRODUCTION

Bandgap reference circuits to generate supply-voltage and temperature independent characteristics are frequently used in analog devices. But to obtain the constant current and voltage the parasitic vertical or lateral bipolar transistors are required or enhancement and depletion MOS transistors are required. To implement bandgap reference circuit by using these method the CMOS fabrication process have to be somewhat controlled. Thereby the process complexity and cost increase[1-5].

This work describes a reference circuit to supply constant current or voltage with temperature. The proposed circuit is fully compatible with a standard CMOS technology it can be integrated with CMOS analog or mixed-mode systems. In Section II the concept of the proposed reference circuit is described. And the reference circuit and the simulation results will be shown with temperature in Section III. Finally, the conclusions show in Section IV.

Manuscript received May 1, 2009 ; Revised June 8, 2009. Jin-Ho Choi is with the Department of Embedded IT, Pusan University of Foreign Studies, Busan, 608-738, Korea (Tel: +82-51-640-3194, Fax: +82-51-640-3038, Email: jhchoi@pufs.ac.kr)

II. REFERENCE CIRCUIT IMPLEMENTETION

Fig. 1 shows the concept of the proposed reference circuit. The bias circuit is conventional CMOS self-bias circuit. The output voltage V_{P_TEMP} has a positive temperature coefficient and V_{N_TEMP} has a negative temperature coefficient. The temperature dependent output voltages of the bias circuit are converted to the temperature dependent currents. The temperature stable current is obtained by the summation of I_{N_TEMP} and I_{P_TEMP}.

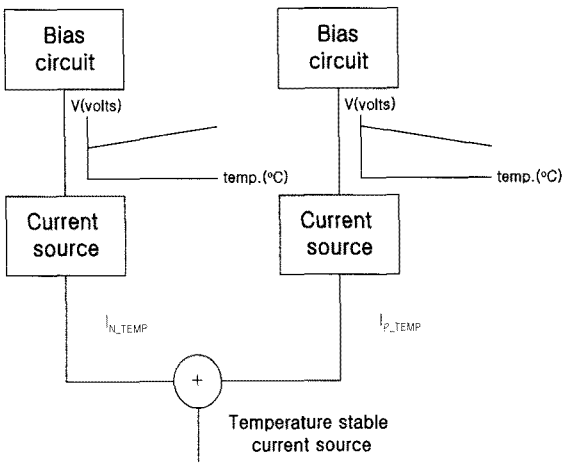


Fig. 1 Concept of the proposed current reference circuit

III. TEMPERATURE CHARACTERISTICS OF FLL CIRCUIT

Fig.2 shows the general CMOS bias circuit. If the resistor R1 is large enough MP1 and MP2 transistors

operate in the subthreshold region. When the channel width of MP1 transistor is n times that of from MP1 transistor, the current equation will be expressed by

$$n \times I_O \exp(-\frac{V_{GS1}}{V_t}) = I_O \exp(-\frac{V_{GS2}}{V_t}) \quad (1)$$

where V_t is the thermal voltage(=kT/q) and V_{GS1} and V_{GS2} are a gate-source voltage of MP1 and MP2 transistors, respectively. Equation (1) is re-expressed by

$$V_t \times \ln(n) = V_{GS1} - V_{GS2} \quad (2)$$

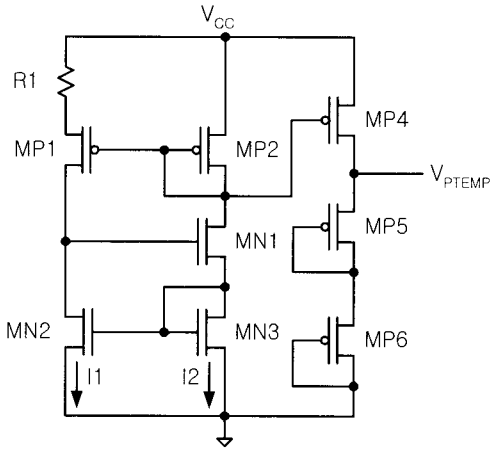
By the Kirchhoff's voltage law the relation of V_{GS1} and V_{GS2} is expressed as follows:

$$V_{GS2} = V_{GS1} - R_1 I_1 \quad (3)$$

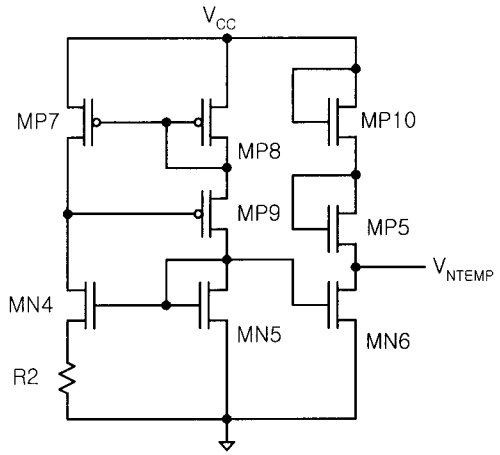
From Eq. (2) and Eq. (3) the current I_1 and I_2 is expressed by

$$I_1 = I_2 = \frac{V_t \times \ln(n)}{R_1} \quad (4)$$

The current I_1 and I_2 have the positive temperature characteristics. The simulation result is shown in Fig. 3, the output voltage, V_{P_TEMP}, increases with temperature. Fig. 2(b) shows the bias circuit, the circuit is constructed similar to the bias circuit of Fig. 2(a). But the output voltage V_{N_TEMP} decreases with temperature by the difference of circuit structure. The simulation result is shown in Fig. 3.



(a) positive temperature coefficient



(b) negative temperature coefficient

Fig. 2 The bias circuit (a) positive temperature coefficient (b) negative temperature coefficient

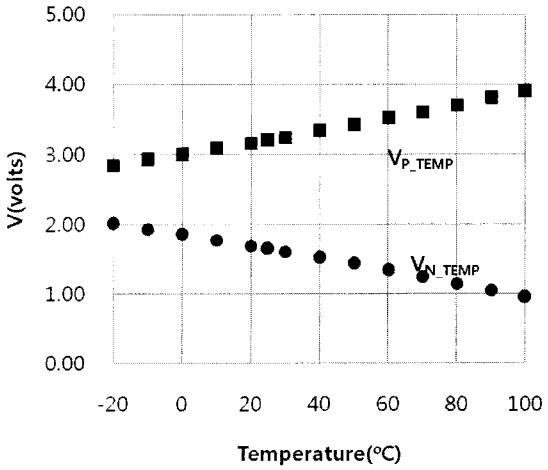


Fig. 3 V_{P_TEMP} and V_{N_TEMP} with temperature

Fig. 4(a) shows the V_{TEMP}, V_{TEMP} is calculated by the Eq. (5).

$$V_{TEMP} = V_{P\_TEMP} + V_{N\_TEMP} \quad (5)$$

And Fig. 4(b) shows the error, percentage of V_{TEMP} variation, over -20℃ to 100℃. The error is calculated by Eq. (6).

$$Error = \frac{V_{TEMP(25°C)} - V_{TEMP}}{V_{TEMP(25°C)}} \times 100(\%) \quad (6)$$

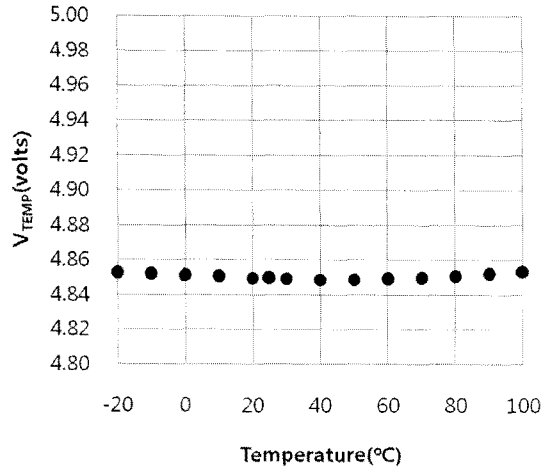


Fig. 4 V_{TEMP} with temperature

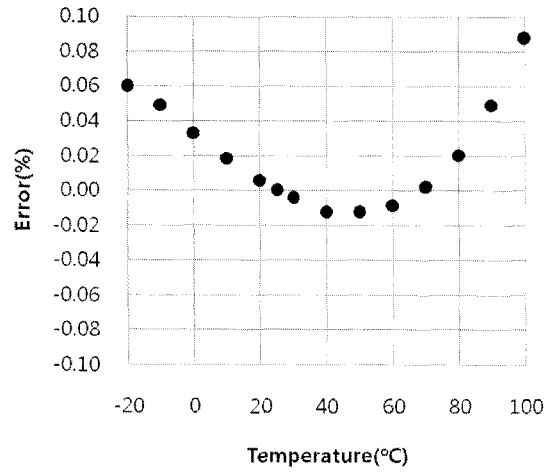


Fig. 5 Error with temperature

Fig. 6 shows the reference circuit to obtain the temperature stable current. The voltage at the node "P" is the same V_{P_TEMP} and the node "N" voltage is the same V_{N_TEMP}. Therefore the current I_{P_TEMP} and I_{N_TEMP} are linearly dependent V_{P_TEMP} and V_{N_TEMP}. The total current, I_{TOTAL}, is the sum of I_{P_TEMP} and I_{N_TEMP}.

Fig. 7 shows the simulation results I_{P_TEMP}, I_{N_TEMP} and I_{TOTAL} with temperature. And Fig. 8 shows the current variation over -20℃ to 100℃. The current variation is calculated by Eq. (7).

$$Error = \frac{I_{TOTAL(25°C)} - I_{TOTAL}}{I_{TOTAL(25°C)}} \times 100(\%) \quad (7)$$

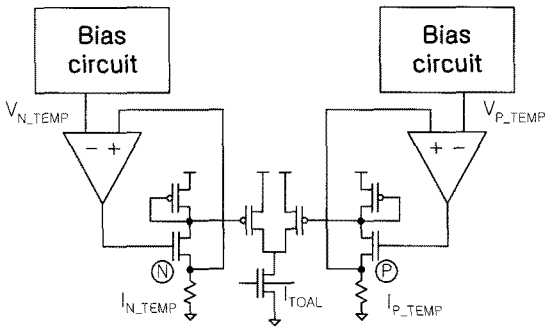


Fig. 6 temperature stable current source circuit

The current variation is less than ±0.44% for samples of temperature in range -20℃ to 80℃. But when the temperature is above 80 ℃ the error increases slightly.

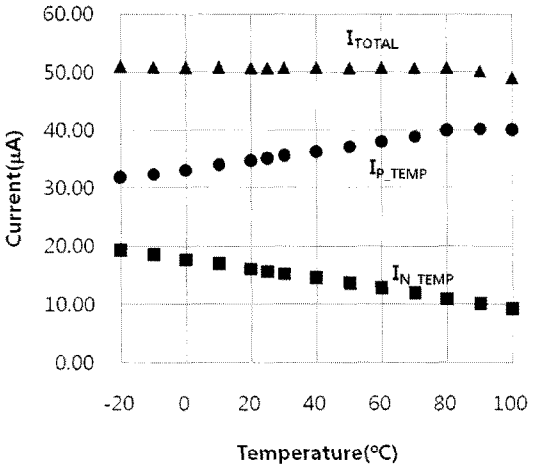


Fig. 7 I_{P_TEMP}, I_{N_TEMP} and I_{TOTAL} with temperature

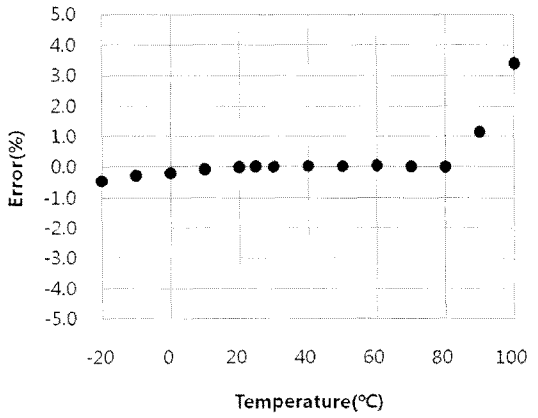


Fig. 8 Error with temperature

Fig. 9 shows I_{P_TEMP} variation for a supply voltage from 4volts to 6volts. Fig. 10 shows $\triangle I_{P\_TEMP}$ with a supply voltage. $\triangle I_{P\_TEMP}$ is calculated by using eq. (8).

$$\Delta I_{P\_TEMP} = \frac{I_{P\_TEMP(25^{\circ}C)} - I_{P\_TEMP(T)}}{I_{P\_TEMP(25^{\circ}C)}} \times 100(\%) \quad (8)$$

From the simulation results the variation is less than ±6% for a ±20% change of a supply voltage.

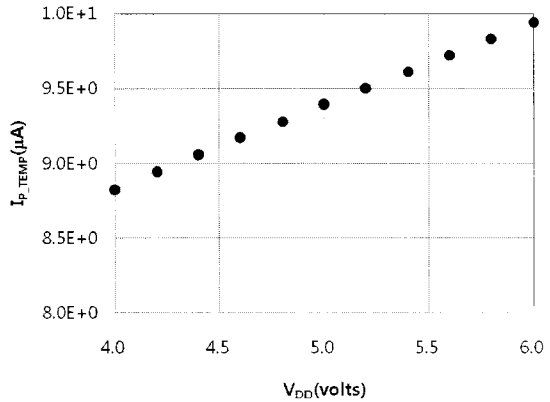


Fig. 9 I_{P_TEMP} with a supply voltage

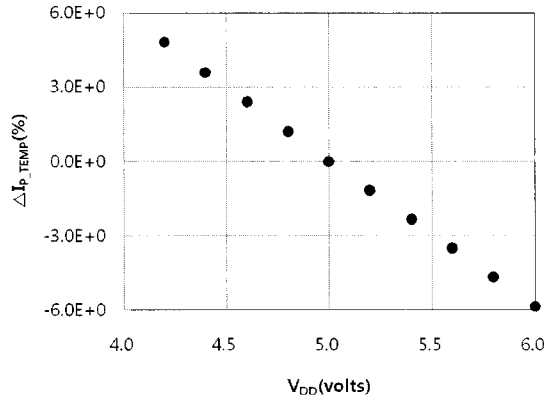


Fig. 10 $\triangle I_{P\_TEMP}$ with a supply voltage

IV. CONCLUSIONS

The temperature stable voltage source and current source are proposed using simple CMOS bias circuit. The voltage variation and current variation with temperature is small enough to use analog circuit. The proposed reference circuit can be integrated on a single chip without extra CMOS process compared to a conventional bandgap reference circuit.

REFERENCES

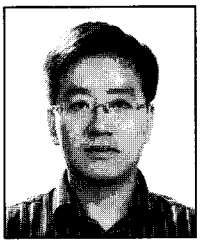
[1] Yueming Jiang and Edward K. F. Lee, "Design of Low-Voltage Bandgap Reference Using Transimpedance Amplifier," IEEE Trans. on Circuits and Systems-II Analog and Digital Signal Processing, vol. 47, no. 6, June 2000.

[2] Rahajandraible W, Auvergne D, Dufaza C et al, "Very Low Power High Temperature Stability Bandgap Reference Voltage," Solid-State Circuits Conference 2002, Sept. 2002.

[3] M. A. P. Pertijs, A. Niederkorn, et al, "A CMOS Smart Temperature Sensor with a 3σ Inaccuracy of ±0.5℃ from -50 to 120," IEEE J. Solid-State Circuits, vol. 40, no. 2, Feb. 2005.

[4] Hironori Banba, Hitoshi Shiga and Akira Umezawa et al, "A CMOS Bandgap Reference Circuit with Sub-1-V Operation," IEEE Journal of Solid-State Circuits, vol. 34, no. 5, May 1999.

[5] Seung-Hoon Lee and Yong JEE, "A Temperature and Supply-Voltage Insensitive CMOS Current Reference," IEICE Trans. Electron, vol. E32-C, no. 8, August 1999.



Jin-Ho Choi
Refer the (IJMICS) International Journal of Maritime Information and Communication Science, vol. 7, no. 1, March 2009. Since 1996, he has been a professor in Dept. of Embedded IT, Pusan University of Foreign Studies.