논문 2009-46SD-7-10

DisplayPort 적용을 위한 대역 확산 클록 발생기 설계

(Design of a Spread Spectrum Clock Generator for DisplayPort)

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요 약

본 논문에서는 CMOS 회로를 이용하여 디스플레이포트(DisplayPort)에 사용 가능한 스프레드 스펙트럼 클록 발생기(SSCG)를 제안하고 구현하였다. 스프레드 스펙트럼 클록 발생기를 1-1 MASH 시그마-델타 변조기(Sigma-delta modulator)를 이용한 분수형 분주기를 사용하여 분주비를 변화시켜 확산시키는 구조를 사용하였다. MASH 1-1 시그마-델타 변조기를 사용하게 되면 회로구성이 용이해지고 면적일 줄일 수 있는 장점이 있다. 시그마 델타 변조기를 이용한 스프레드스펙트럼 생성기의 장점은 확산비율과 변조율을 시그마 델타 변조기의 입력 값을 변조하여 정확하게 조절할 수 있다는 것이다. 확산비율과 변조율은 디스플레이포트 표준 스펙에 만족되도록 설계하였고, 디스플레이포트 링크심볼클록인 270㎒/162㎒ 듀얼 모드 클록에서도 만족하도록 설계하였다. 그리고 변조파형은 33KHz의 삼각파의 형태를 취하고 있고, 0.25%의 다운스프레드 스펙트럼 클록이 발생한다. 스프레드 스펙트럼 클록 발생기의 세부 설계블록들은 모두 풀커스텀 방식으로 설계하였다. 또한 0.18㎛ 1P-6M CMOS 공정을 사용하여 설계 및 제작되었으며, 레이아웃 된 전체 블록의 면적은 0.620㎜ X 0.780㎜이었다. 칩 측정결과 디스플레이포트 동작기준을 잘 만족함을 보였다.

Abstract

This paper describes design and implementation of a spread spectrum clock generator (SSCG) for the DisplayPort. The proposed architecture generates the spread spectrum clock using a sigma-delta fractional-N PLL. The SSCG uses a digital 2nd order MASH 1-1 sigma-delta modulator and a 9bit Up/Dn counter. By using MASH 1-1 sigma-delta modulator, complexity of circuit and chip area can be reduced. The advantage of sigma-delta modulator is the better control over modulation frequency and spread ratio. The SSCG generates dual clock rates which are 270㎒ and 162㎒ with 0.25% down-spreading and triangular waveform frequency modulation of 33㎑. The peak power reduction is 11.1dBm at 270㎒. The circuit has been designed and fabricated using in 0.18㎛ CMOS technology. The chip occupies 0.620㎜ X 0.780㎜. The measurement results show that the fabricated chip satisfies the DispalyPort standard.

Keywords: Spread Spectrum clock, SSCG, PLL, modulation ratio, DisplayPort

I. Introduction

The increasing speed of microprocessors, optical transmission links, intelligent hubs and routers are pushing the data rate into the giga bits-per-second range. As operating at high frequencies, currents and voltages present in the circuits and the signal traces leads to large Electro-Magnetic Interference (EMI)[1]. The EMI level of an electronic system should be restricted to a certain level for a stable operation with other electronic systems. The simplest way to reduce EMI seems to be a shielding; however, it cannot be applied to all system, especially to system-on-a-chip (SoC) level. One of the most

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※ This work is supported by the Ministry of Knowledge Economy (MKE) through System IC 2010, Human Resource Training Project for Strategic Technology from KOTEF, and IT-SoC program from ETRI. Authors also thank IDEC program.

접수일자: 2009년1월2일, 수정완료일: 2009년7월14일

efficient ways to reduce EMI is spreading out radiation energy around its peak frequency using a spread spectrum clock generator (SSCG) which makes a frequency modulation to the original system clock. A SSCG is an efficient way to reduce EMI radiation in modern mixed signal chip systems. There are many types of SSCGs in the literatures. Most SSCGs are designed by modulating the dividers in the PLL. A fractional-N PLL achieves the higher resolution with high operating frequency, and also reduces the drawbacks such as a spur using the digital sigma-delta modulation technique.

In this paper, a SSCG using a sigma-delta fractional-N PLL for the DisplayPort is presented. The DisplayPort SSCG requires both 270㎒ and 162㎒ operating frequencies. Also, it satisfies spread spectrum clock with 30~33㎑, and 0%~0.5% down-spread frequency modulation[2]. Two up/dn counters and multi-modulus dividers for two different clock modes should be included.

The outline of this paper is as follows. In the section Ⅱ, the proposed SSCG architecture is presented. Section Ⅲ describes the measured results and then conclusion is given in section Ⅳ.

Ⅱ. Proposed SSCG Architecture

1. TOP BLOCK

Fig. 1 shows the block diagram of the proposed SSCG. The SSCG is based on a fractional-N PLL using sigma-delta modulation technique to modulate the divider. The divided output clock is used in the up/dn counter. The up/dn counter produces a triangular waveform of 30~33㎑ and 0.25% down spread ratio frequency deviation. The output of the counter is used to control the sigma-delta modulator. The operating frequency is selected by "SEL" control signal and the SSC function is turned on or off by "SSC mode" control signal. These control signals are manually controlled.

The multi-modulus divider operates as 8-11 dividing mode with 270㎒ clock when "SEL" signal is

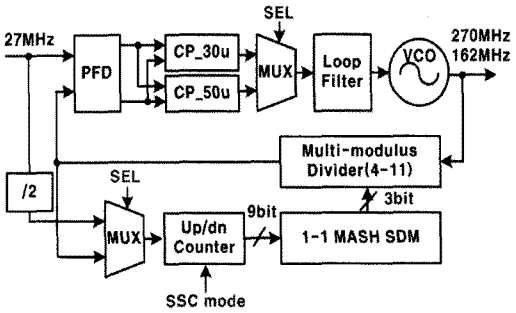

그림 1. 제안된 SSCG 회로의 블록다이어그램
Fig. 1. Block diagram of the proposed SSCG.

on. The multi-modulus divider operates as 4-7 dividing mode with 162㎒ clock for DisplayPort. Two different current charge pumps are implemented for adjusting loop bandwidths of each clock rates.

A. Voltage Controlled Oscillator

Fig. 2 shows the schematic of the VCO which consists of a 5-stage ring oscillator. The bias voltage

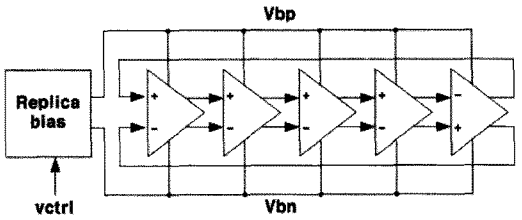

그림 2. 전압 제어 발진기의 블록다이어그램
Fig. 2. Block diagram of the Voltage Controlled Oscillator.

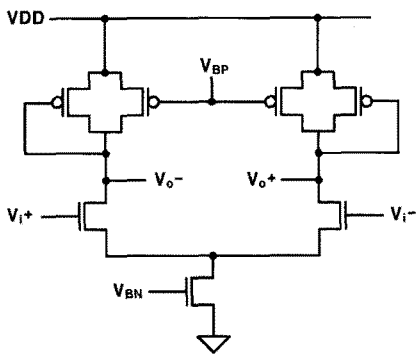

그림 3. 지연 셀의 블록다이어그램
Fig. 3. Block diagram of the Delay cell.

generator can adjust Vbn dynamically by its own negative feedback loop to compensate the PVT variation. The self biased technique can provide a wide frequency range, minimized supply and substrate noise[3]. The delay cell of the VCO shown in Fig. 3 is a source-coupled pair with symmetric active loads for the better linearity of the VCO gain and wider swing.

B. Charge pump

The schematic in Fig. 4 shows a charge pump. A unity-gain buffer is used to clamp the terminal voltages of current sources during the zero-current pumping period. In this way, voltage glitches on the loop filter due to charge sharing can be eliminated. Both the up and the down current can be either connected to the output or drained to a dummy reference voltage by the four switches. To minimize clock feed-through, all switches are implemented by TG (transmission gate) and every switch has its own control signal. The relative timing of the charge pump switches is optimized to avoid glitches at the output node.

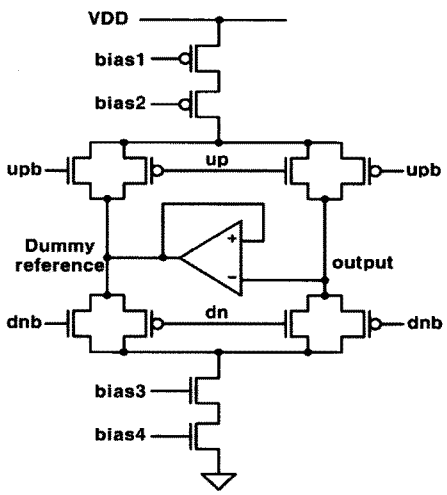

그림 4. 전하펌프의 블록다이어그램
Fig. 4. Block diagram of the Charge pump.

C. 2nd order MASH sigma-delta modulator

Usually a fractional-N PLL achieves the fine resolution at higher operating frequencies. A sigma-delta modulator makes the average input value unchanged and modulates the quantization noise to a higher frequency. In conventional sigma-delta digital-to-analog converters, the output of modulators is followed by a low pass filter in order to remove quantization noise. In this system, the out-band quantization noise are filtered by the PLL. The higher order sigma-delta modulator can suppress the quantization noise effectively. But the single-loop architecture may have instability. MASH architecture can solve instability problem and can be easily implemented using all digital architectures. Thus, it can be integrated into a single chip and is insensitive to process variation.

The 2nd order MASH sigma-delta modulator is used for the proposed design. The 2nd order MASH 1-1 sigma-delta modulator implemented by cascading two first order sigma-delta modulator is illustrated in Fig 5. By performing linear analysis on this model, the input/output relationship of the modulator can be written as follow;

$$Y(z) = F(z) + Q_2(z)(1 - z^{-1})^2 \quad (1)$$

where F(z), Y(z), and $Q_2(z)$ are the Z-transform of the input, output, and quantization noise from two stages, respectively. It is shown that the quantization error is shaped and pushed to high frequency by placing two zeros at the origin. Then the closed loop behavior of PLL filters the quantization noise.

Fig. 6 shows the realization of MASH 1-1 sigma-delta modulator. The proposed SSCG uses 14bit

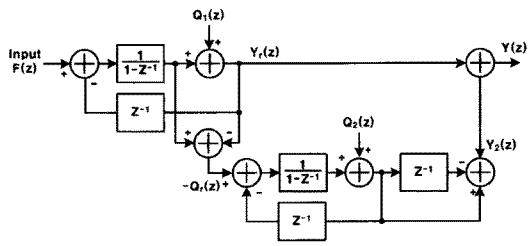

그림 5. 2차 MASH 1-1 시그마-델타 변조기
Fig. 5. 2nd order MASH 1-1 sigma-delta modulator.

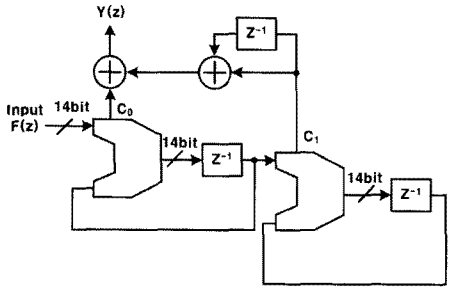

그림 6. 디지털 MASH 1-1 시그마-델타 변조기
Fig. 6. Digital MASH 1-1 sigma-delta modulator.

accumulators.

D. Up/Dn counter

The DisplayPort requires spreading clock spectrum with 30~33㎑ modulation frequency and less than 0.5% down-spread frequency modulation[2].

The up/dn counter is used to satisfy required specifications. For down-spreading operation, the up/dn counter's reset value is set to $111111111_{(2)}$. When the "SEL" is on, the counter iterates increasing and decreasing from $111111111_{(2)}$ to $001101011_{(2)}$ at 270MHz clock mode. When the "SEL" is off, counter iterates from $111111111_{(2)}$ to $100111000_{(2)}$ at 162MHz mode. At 162㎒ clock mode, the input clock of the up/dn counter is divided by 2. The output of the up/dn counter oversampled by the sigma-delta modulator can produce a triangular waveform. The counter value could be determined as follows;

- 270MHz clock mode

$$27Mhz \times 10\left(1-\frac{405}{16384}\right)=27Mhz \times 10 \times 0.975 \quad (2)$$

$$37.037ns \times 810 = 30us \quad (3)$$

- 162MHz clock mode

$$27Mhz \times 6\left(1-\frac{200}{16384}\right)=27Mhz \times 6 \times 0.987 \quad (4)$$

$$37.037ns \times 2 \times 400 = 30us \quad (5)$$

E. Multi-Modulus Divider

The Multi-modulus divider generates a sequence with multi-bit states by MASH 1-1 sigma-delta modulator. The output of the second order MASH 1-1 sigma-delta modulator is spread to n-1, n, n+1, and n+2. The n values of the proposed SSCG are varying from 5 to 9 for different clock outputs. In other words, the divider is working as the 4 to 7 divider for 270㎒ and the 8 to 11 divider for 162㎒ respectively. When the "SEL" is on, the multi-modulus divider operates at the 8 to 11 dividing mode, otherwise the multi-modulus divider operates at the 4 to 7 dividing mode. The multi-modulus divider is designed using Verilog coding and logic synthesis.

III. Measurement Result

The proposed SSCG for DisplayPort has been implemented with TSMC CMOS 0.18㎛ 1-Poly 6-Metal process.

Fig. 7 shows the microphotograph of the chip which occupies 620㎛ x 780㎛. It is implemented by full-custom design method. Fig. 8 shows the simulated modulation profile of the proposed SSCG circuit.

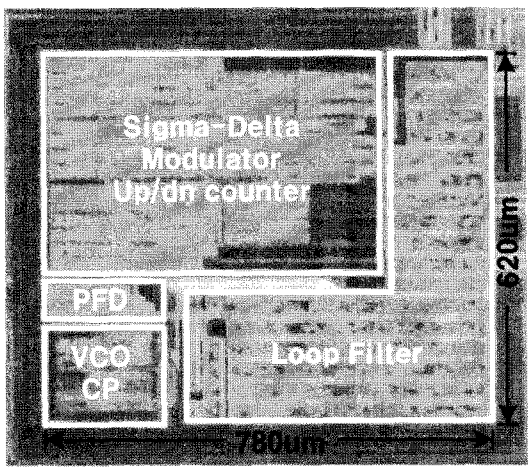

그림 7. 칩 사진
Fig. 7. Microphotograph of the chip.

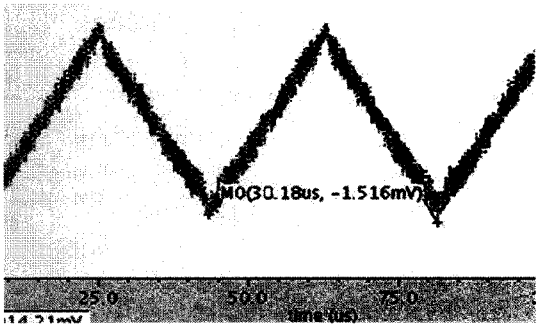

그림 8. 위상 고정이후 삼각 변조 파형(시뮬레이션)
Fig. 8. Triangular modulation profile after phase locked (simulated).

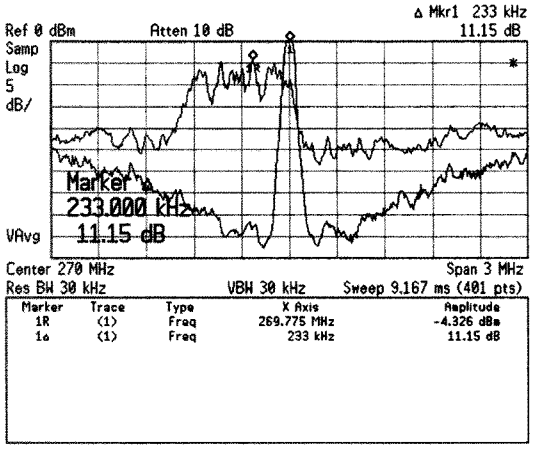

그림 9. 설계된 SSCG의 270㎒ dBm 측정파형
Fig. 9. Measured spectrum dBm of the 270㎒ output signal with spread spectrum.

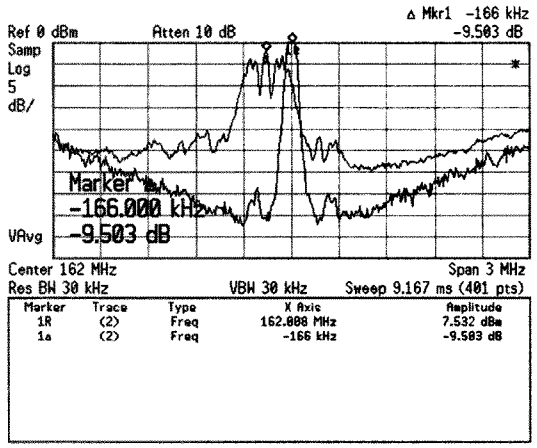

그림 10. 설계된 SSCG의 162㎒ dBm 측정파형
Fig. 10. Measured spectrum dBm of the 162㎒ output signal with spread spectrum.

표 1. 제안된 SSCG 회로의 성능 요약
Table 1. Proposed SSCG performance summary.

SSCG Frequency	270MHz 162MHz	DisplayPort spec.
Technology	TSMC 0.18um CMOS	-
Modulation Profile	33㎑ triangular	30㎑~33㎑
Frequency Deviation	0.25%(270㎒) 0.21%(162㎒)	< 0.5%
Peak Power Reduction	11.15dB(270㎒) 9.50dB(162㎒)	-
jitter (peak-peak) @270MHz	13.3ps @ Non-SSCG 35.6ps @ SSCG	-
Loop Bandwidth	250㎑	< 4㎒
Supply Voltage	1.8V	-
Power Dissipation	40mW	-
SSCG area	620um x 780um	-

Fig. 9 and Fig. 10 show the measured results of the output signals with a spectrum analyzer. Fig. 9 shows the spectrum of 270㎒ SSCG output after spreading. Comparing with the non-SSCG, the peak power reduction is about 11dB with 0.25% spread ratio. Fig. 10 shows the comparison between the non-spread clock and the spread clock at 162㎒. Comparing with the non-SSCG, the peak power reduction is about 9.5dB with 0.2% down spread ratio.

The measured peak-peak jitter is 13.3ps with non-SSCG mode and 35.6ps at 270MHz with SSCG mode. The proposed SSCG performances are summarized in Table 1.

IV. Conclusion

A 270㎒/162㎒ SSCG for DisplayPort has been designed and implemented using a 0.18㎛ CMOS process. The spread spectrum clock generator uses a fractional-N frequency synthesizer to achieve specified spreading spectrum ratio with triangular waveform modulation. The spread spectrum clock generator consists of a fractional-N PLL, up/dn counter, and second order sigma-delta modulator. The prototype chip occupies 0.620㎜ x 0.780㎜. The peak

power reduction of 11dB is achieved and power dissipation of the chip is 40㎽ at 270㎒ mode.

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