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메모리 인터페이스를 위한 적응형 프리엠퍼시스를 가지는 8-Gb/s/채널 비균형 4-레벨 펄스진폭변조 입출력회로

(An 8-Gb/s/channel Asymmetric 4-PAM Transceiver with an Adaptive Pre-emphasis for Memory Interface)

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요 약

고속 메모리의 인터페이스를 위한 8 × 8-Gb/s/채널 4-레벨 펄스진폭변조 입출력회로를 1.35V의 공급전압을 가지는 70nm DRAM 공정을 이용하여 설계하였다. 4-레벨 펄스진폭변조를 위한 3 가지의 eye opening에서 상위와 하위 eye의 전압과 시간의 마진을 증가시키기 위해 비균형 4-레벨 펄스진폭변조의 신호전송 기법을 제안한다. 제안한 기법은 수신 단에서의 기준 전압 노이즈 영향을 33% 감소시키며, 이를 통계적인 수식을 통해 분석한다. 일반적인 직렬 인터페이스 대비 신호 손실이 적은 DRAM 채널의 ISI(신호간의 간섭)를 줄이기 위해 수신 단에서 단일 비트 펄스의 테스트 신호를 적분함으로 ISI를 측정하는 적응형 프리앰퍼시스 기법을 구현한다. 또한, 이를 위해 정해진 테스트 패턴에 의해 최적의 ISI를 측정하기 위한 적분 클럭의 시간 보정기법을 제안한다.

Abstract

An 8 × 8-Gb/s/channel 4-PAM transceiver was designed for high speed memory applications by using 70nm DRAM process with 1.35V supply. An asymmetric 4-PAM signaling scheme is proposed to increase the voltage and time margin of upper and lower eyes in 3-class eye opening. A mathematical basis shows that this scheme statistically reduces 33% of reference noise effect in a receiver. Also, an adaptive pre-emphasis scheme, which utilizes a lone-bit pulse with integrator at the receiver, is introduced to reduce ISI for a simple DRAM channel. In this scheme, an integrating clock timing calibration by using a pre-determined pattern is proposed for the optimum ISI measurement.

Keywords : DRAM, pulse amplitude modulation (PAM), transceiver, inter-symbol-interference (ISI), pre-emphasis

I. Introduction

As the interface speed of a memory system increases, design techniques often used in high-speed serial links become more attractive for a high speed memory interface system. For example, the design techniques such as data training, transmitter (TX)/receiver (RX) equalization, circuit with inductor, and data coding have been adopted or considered[1~3]. In this context, a pulse amplitude modulation (PAM) is another candidate for a high speed memory interface system[4].

In general, 4-PAM signaling increases timing margin at the receiver by reducing the *Nyquist* frequency by half for the interface channel. However, in terms of voltage margin, 4-PAM signaling is effective when more than 10dB of channel loss, mostly caused by dielectric loss and skin effect, is expected by doubling the signaling speed[4]. This is

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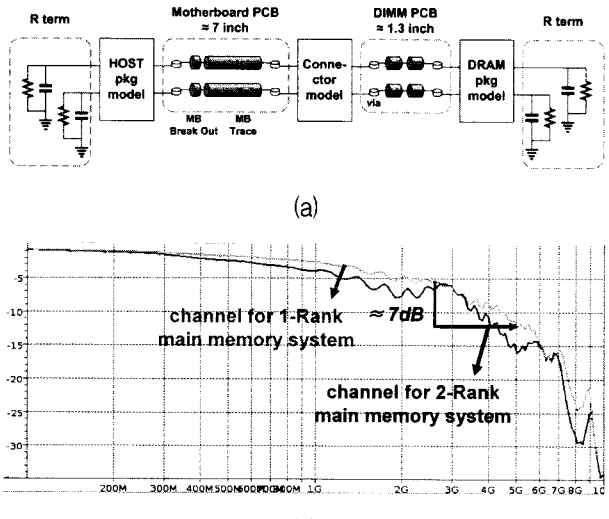


그림 1. (a) 주 메모리 DRAM 시스템의 채널 모델 (b) 1-Rank와 2-Rank 메모리 채널의 주파수 응답

Fig. 1. (a) Channel model of main memory DRAM system (b) Frequency response of 1-Rank and 2-Rank memory channels.

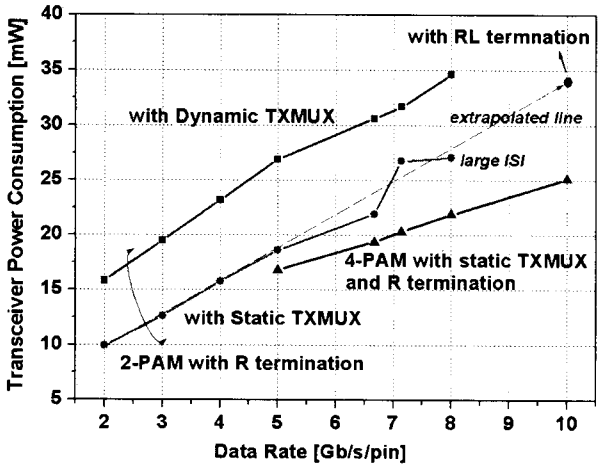


그림 2. 클럭 트리를 제외한 입출력회로의 전력 소모

Fig. 2. Power consumption of transceiver except clock tree.

because 4-PAM scheme itself reduces the voltage margin by 1/3.

For a main memory (DRAM-dynamic random access memory) interface where its data rate is not exceeding 1.6-Gb/s/pin and multi-drop interface should be supported, the signal integrity is more affected by channel noise sources such as cross-talk by near-by channel and reflection by impedance mismatches than by intrinsic channel attenuation itself. Also, the short point-to-point channel for graphic application does not ultimately limit the 2-PAM signaling by adopting TX/RX equalization. For these reasons, the multi-level signaling for a DRAM interface was not adopted for now.

However, the data rate of a main memory interface continuously increases. Also, the differential signaling should have at least twice data rate of single-ended signaling to improve the efficiency of pin cost. Thus, the impact of intrinsic channel loss becomes as significant as to consider multi-level signaling. According to Hspice simulation of a memory channel with 1-DIMM (dual in line memory module) shown in Fig. 1(a), the channel loss increases by 7 (1-Rank) to 10dB (2-Rank) as signaling speed is doubled from 2.5 to 5 GHz, as shown in Fig. 1(b). Another important advantage of using 4-PAM signaling is its better power efficiency. Fig. 2 shows the simulated power consumption of differential 2-PAM and 4-PAM transceiver with respect to its data rate. As the data rate increases beyond 5-Gb/s/channel, the power efficiency of 4-PAM transceiver increases with respect to 2-PAM transceivers. This is because 2-PAM transceivers (two types of *4:1 TXMUX* and *termination*) need more power to compensate for the loss of SNR by heavy inter-symbol-interference (ISI) in their internal nodes. Also, 4-PAM signaling reduces the power consumption of clock tree because of the low operation frequency compared to 2-PAM.

An asymmetric 4-PAM signaling scheme, which allows better voltage and timing margin at 8-Gb/s/cahnnel data rate by controlling eye opening of each signal level asymmetrically, is proposed in this paper. Also, a simple adaptive pre-emphasis scheme which utilizes 1-bit lone pulse is introduced for the DRAM application.

II. Asymmetric 4-Pam Transceiver Design

1. Conventional 4-PAM Transceiver

Fig. 3 shows the block diagram of conventional 4-PAM for one channel. TX is composed of two drivers with different current source, as shown in

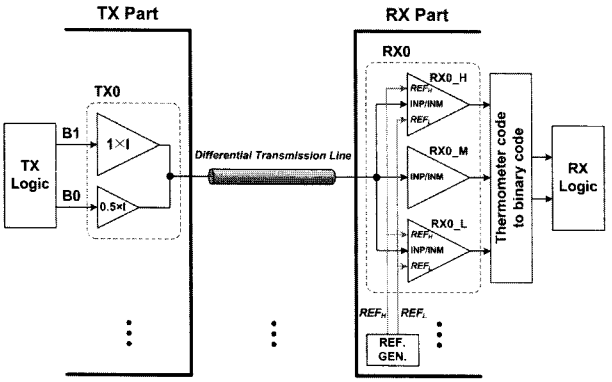


그림 3. 전통적인 4-레벨 펄스진폭변조를 위한 입출력 회로의 블럭도

Fig. 3. Block diagram of conventional 4-PAM transceiver.

Fig. 4(a). Generally, a driver for least significant bit (LSB) has the current source of a half compared to most significant bit (MSB). Also each driver uses a differential amplifier for differential signaling. RX is composed of three unit receivers for 4-PAM, as shown in Fig. 3. RX with reference shown in Fig. 4(b) is used for *RX0_H* and *RX0_L* in Fig. 3. RX shown in Fig. 4(c) is used for only *RX0_M* to determine MSB. Additionally, a logic decoder block is required to convert from thermometer code to binary code for 4-PAM.

Fig. 5 is the conceptual eye diagram of 4-PAM[4]. In the conventional 4-PAM with ΔV_2, ΔV_1, and ΔV_0 of the same voltage amplitude (ΔV), the reference noise makes to decrease the voltage margin in *RX0_H* and *RX0_L*. Eq. (1)~(4) show the voltage margin about four cases in *RX0_H*. When the deterministic noise magnitude of references (REF_H, REF_L) is 3α, the voltage margin of worst case is $\Delta V-6\alpha$. The voltage margin in *RX0_H* is equal to that of in *RX0_L*. However, in the case of *RX0_M*, the voltage margin of worst case is ΔV because *RX0_M* does not use any reference, as shown in Fig. 4(c) (Eq. (5)~(8)). Also, the time margin was determined in *RX0_H* and *RX0_L* because T_{eye2} is smaller than T_{eye1} due to the feature of 4-PAM. As a result, the voltage and time margin in 4-PAM are determined by the performance of RX with reference and the input signal integrity in front of it.

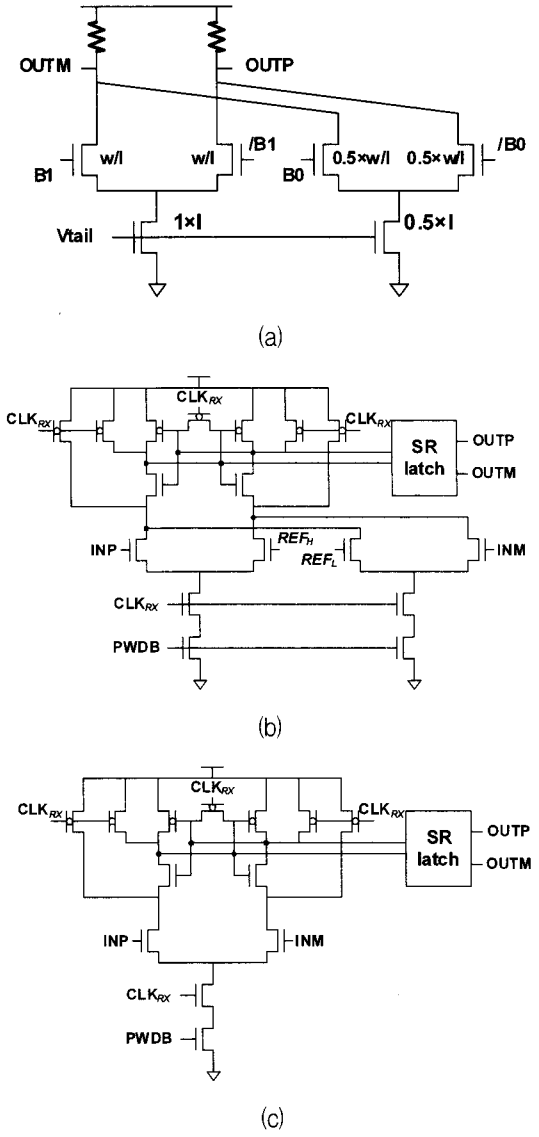


그림 4. 4-레벨 펄스진폭변조 입출력회로를 위한 (a) 송신회로 (b) 기준전압을 가지는 수신회로 (c) 기준전압이 없는 수신회로

Fig. 4. (a) Transmitter (b) Receiver with reference (c) Receiver without reference for 4-PAM transceiver.

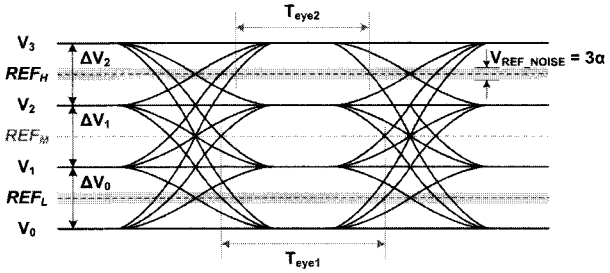


그림 5. 전통적인 4-레벨 펄스진폭변조의 개념적인 eye diagram

Fig. 5. Conceptual eye diagram of conventional 4-PAM

$$V_{MARGIN-CASE1-RX0\_H} = |(V_3 - REF_H) - (V_0 - REF_L)| - 2\times 3\alpha = |(0.5\cdot\Delta V) - (-0.5\cdot\Delta V)| - 6\alpha = \Delta V - 6\alpha \quad (1)$$

$$V_{MARGIN-CASE2-RX0\_H} = |(V_2 - REF_H) - (V_1 - REF_L)| - 2\times 3\alpha = |(-0.5\cdot\Delta V) - (0.5\cdot\Delta V)| - 6\alpha = \Delta V - 6\alpha \quad (2)$$

$$V_{MARGIN-CASE3-RX0\_H} = |(V_1 - REF_H) - (V_2 - REF_L)| - 2\times 3\alpha = |(-1.5\cdot\Delta V) - (1.5\cdot\Delta V)| - 6\alpha = 3\cdot\Delta V - 6\alpha \quad (3)$$

$$V_{MARGIN-CASE4-RX0\_H} = |(V_0 - REF_H) - (V_3 - REF_L)| - 2\times 3\alpha = |(-2.5\cdot\Delta V) - (2.5\cdot\Delta V)| - 6\alpha = 5\cdot\Delta V - 6\alpha \quad (4)$$

$$V_{MARGIN-CASE1-RX0\_M} = |V_3 - V_0| = 3\cdot\Delta V \quad (5)$$

$$V_{MARGIN-CASE2-RX0\_M} = |V_2' - V_1'| = 1\cdot\Delta V - 4\alpha \quad (6)$$

$$V_{MARGIN-CASE3-RX0\_M} = |V_1' - V_2'| = 1\cdot\Delta V - 4\alpha \quad (7)$$

$$V_{MARGIN-CASE4-RX0\_M} = |V_0 - V_3| = 3\cdot\Delta V \quad (8)$$

2. Proposed Asymmetric 4-PAM Transceiver

To reduce the above mentioned issue, the asymmetric 4-PAM scheme is proposed, as shown in Fig. 6. It has the level of V_1 and V_2 adjusted by $2a$ and the level of reference adjusted by $1a$, when the deterministic noise magnitude of references is $3a$. In this case, the power consumption of transceiver is equal to the conversional 4-PAM because the amplitude of the maximum full swing from V_0 to V_3 is not changed.

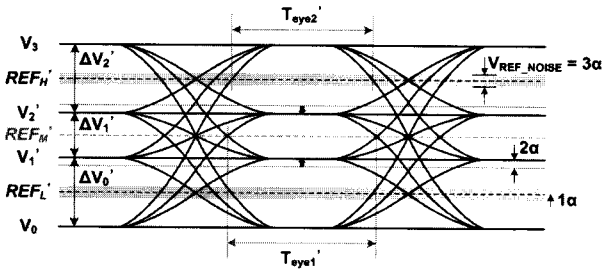


그림 6. 비균형 4-레벨 펄스진폭변조의 개념적인 eye diagram

Fig. 6. Conceptual eye diagram of asymmetric 4-PAM.

The optimal level of V_1' and V_2' for asymmetric 4-PAM is determined by the condition which the magnitude of center eye is equal to that of upper or lower eye including the effect of reference noise. Eq. (9) is the generalized formula for N-PAM.

$$\Delta V - \beta = (\Delta V + \frac{\beta}{N-2}) - 2\times\delta,\ \beta = \frac{2\delta\cdot(N-2)}{N-1} \quad (9)$$

where β is the summation of magnitude which the level of V_1 and V_2 is controlled. N is the multi-level number of PAM and δ is the noise magnitude of reference signal. When δ is $3a$ in 4-PAM, β is determined to $4a$. Eq. (10)~(17) show the voltage margin about four cases in *RX0_H* and *RX0_M* in the asymmetric 4-PAM with reference noise of $3a$.

$$V_{MARGIN-CASE1-RX0\_H} = |(V_3 - REF_H') - (V_0 - REF_L')| - 2\times 3\alpha = |(0.5\cdot\Delta V + 1\alpha) - (-0.5\cdot\Delta V - 1\alpha)| - 6\alpha = \Delta V - 4\alpha \quad (10)$$

$$V_{MARGIN-CASE2-RX0\_H} = |(V_2' - REF_H') - (V_1' - REF_L')| - 2\times 3\alpha = |(-0.5\cdot\Delta V - 1\alpha) - (0.5\cdot\Delta V + 1\alpha)| - 6\alpha = \Delta V - 4\alpha \quad (11)$$

$$V_{MARGIN-CASE3-RX0\_H} = |(V_1' - REF_H') - (V_2' - REF_L')| - 2\times 3\alpha = |(-1.5\cdot\Delta V + 3\alpha) - (1.5\cdot\Delta V - 3\alpha)| - 6\alpha = 3\cdot(\Delta V - 4\alpha) \quad (12)$$

$$V_{MARGIN-CASE4-RX0\_H} = |(V_0 - REF_H') - (V_3 - REF_L')| - 2\times 3\alpha = |(-2.5\cdot\Delta V + 1\alpha) - (2.5\cdot\Delta V - 1\alpha)| - 6\alpha = 5\cdot\Delta V - 8\alpha \quad (13)$$

$$V_{MARGIN-CASE1-RX0\_M} = |V_3 - V_0| = 3\cdot\Delta V \quad (14)$$

$$V_{MARGIN-CASE2-RX0\_M} = |V_2' - V_1'| = 1\cdot\Delta V - 4\alpha \quad (15)$$

$$V_{MARGIN-CASE3-RX0\_M} = |V_1' - V_2'| = 1\cdot\Delta V - 4\alpha \quad (16)$$

$$V_{MARGIN-CASE4-RX0\_M} = |V_0 - V_3| = 3\cdot\Delta V \quad (17)$$

The voltage margin of worst case is ΔV-$4a$. The voltage margin of $2a$ was increased compared to the conventional 4-PAM. Also the time margin in *RX0_H* increase from T_{eye2} to T_{eye2}' due to reference level shifting (REF_H', REF_L').

For the proposed asymmetric 4-PAM scheme, the transmitter has the method to adjust the current

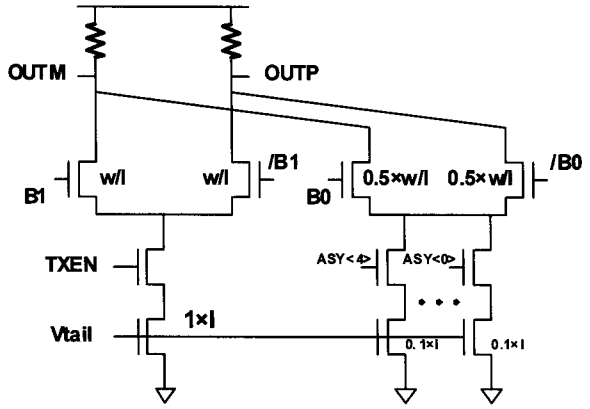
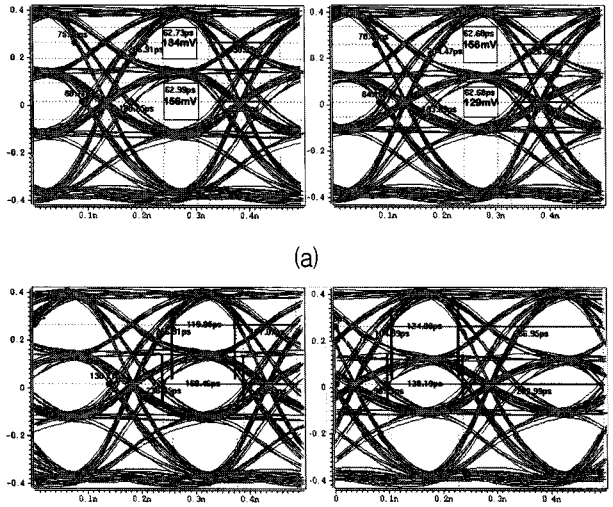


그림 7. 비균형 4-레벨 펄스진폭변조를 위한 송신회로
Fig. 7. Transmitter for asymmetric 4-PAM.



(a)

(b)

그림 8. 전통적인 4-레벨 펄스진폭변조와 비균형 4-레벨 펄스진폭변조의 시뮬레이션 결과
(a) 전압 마진
(b) 시간 마진 @ rectangle eye mask
Fig. 8. Simulation results of conventional 4-PAM and asymmetric 4-PAM.
(a) voltage margin
(b) time margin at rectangle eye mask

strength of TX driver for LSB (*B0*), as shown in Fig. 7. 5-bit digital code was used to control the level of V_1' and V_2' according to the magnitude of RX reference noise. Also, the decoupling capacitor was additionally added for stable digital code level.

Fig. 8 is the simulation results of the conventional 4-PAM and proposed asymmetric 4-PAM scheme. The simulation was achieved in the condition of the channel shown in Fig. 1(a) and the data rate of 8-Gb/s/channel. Fig. 8(a) shows the voltage margin

표 1. 전통적인 4-레벨 펄스진폭변조와 비균형 4-레벨 펄스진폭변조의 eye 마진
Table 1. Eye margin of conventional 4-PAM and asymmetric 4-PAM.

Eye mask : Rectangle		eye_center	eye_upper		
			diff_ref. noise (00mV)	diff_ref. noise (30mV)	diff_ref. noise (60mV)
voltage margin [mV]	Symmetric 4-PAM	***156***	134	***104***	74
	Asymmetric 4-PAM	***129***	156	***126***	96
time margin [ps] (target :62.5ps)	Symmetric 4-PAM	62.99	62.73		
	Asymmetric 4-PAM	62.68	62.68		

Eye mask : Diamond		eye_center	eye_upper		
			diff_ref. noise (00mV)	diff_ref. noise (30mV)	diff_ref. noise (60mV)
voltage margin [mV]	Symmetric 4-PAM	***214.6***	217.4	187.4	***157.4***
	Asymmetric 4-PAM	***182.8***	241.9	211.9	***181.9***
time margin [ps]	Symmetric 4-PAM	150.46	***119.05***		
	Asymmetric 4-PAM	138.19	***124.09***		

for eye mask of rectangle with time margin of about 62.5ps. Fig. 8(b) shows the time margin for eye mask of diamond. Table 1 is the summary of simulation results shown in Fig. 8. The voltage margin and time margin of the asymmetric 4-PAM increase compared to the conventional 4-PAM when the reference noise exists in RX. Actually, the magnitude of RX reference noise is about 30mV in DDR3 SDRAM.

III. TX Pre-Emphasis for DRAM Channel

In high speed serial links, the complex algorithm and hardware is generally used to reduce ISI [5]. However, in the channel with the monotonically decreasing frequency response, as shown in Fig. 1,

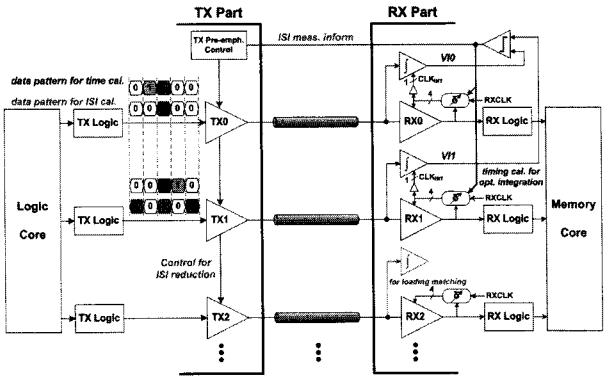


그림 9. ISI 제거를 위한 간략화된 블록도
Fig. 9. Simplified block diagram for ISI reduction.

the ISI of channel can be measured by comparing the pulse width between 1-bit lone pulse and toggle pattern with minimum ISI.

Fig. 9 is the simplified block diagram for the proposed ISI reduction. For this scheme, two TXs (*TX0, TX1*) repeatedly transmit the pre-determined patterns of 1-bit lone pulse ("00100") and toggle pattern ("10101"), respectively. The voltage levels of "0" and "1" are V_0 and V_3 in Fig. 6. RX part measures the channel ISI by integrating the pulse width of the pre-determined patterns supplied from two TXs. The RX part returns the comparison result between two integrated values (*VI0, VI1*) to TX part. Then, the pre-emphasis of TX is controlled by the feedback result from RX part until two integrated values at each RX input are equal. The 1-tab TX FIR controlled by 5-bit digital code was designed for a DRAM channel with smaller loss than a serial interface channel. The current integrator was used to measure the pulse width[6]. The integrating clock for the current integrator used one clock among 4-phase clock for RX with clock scheme of a quad data rate, as shown in Fig. 9.

The timing calibration of the integrating clock (CLK_{INT}) for the current integrator is required for exact integration of pulse width independent of the normal operation. For this timing calibration process, Two TXs repeatedly transmit "0110" patterns with 1UI delay difference about through each channel. Fig.

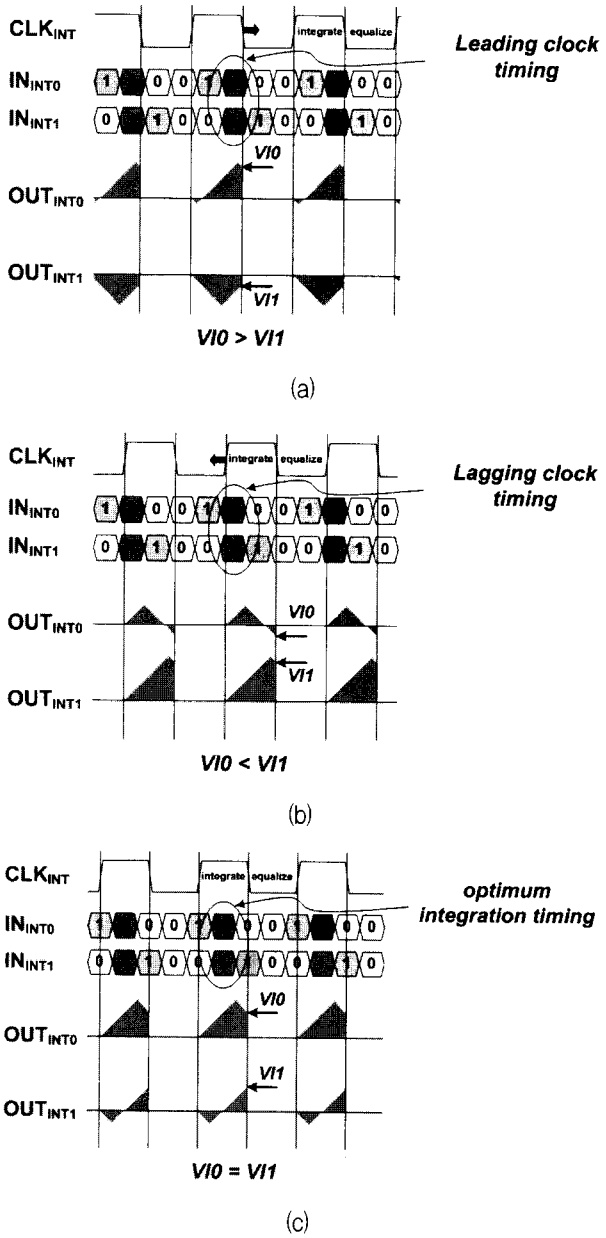
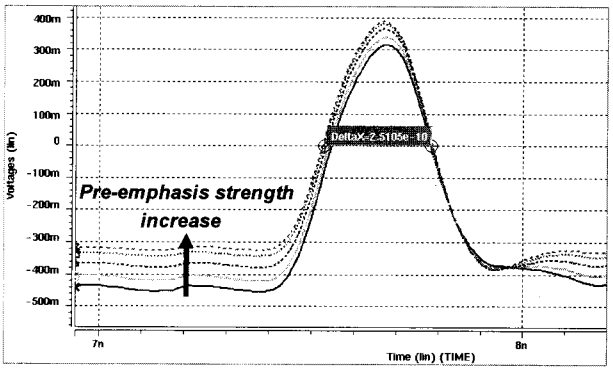


그림 10. 적분 클럭을 위한 타이밍 다이어그램
(a) leading 클럭 타이밍 (b) lagging 클럭 타이밍 (c) 최적의 클럭 타이밍

Fig. 10. Timing diagram for integrating clock.
(a) leading clock timing (b) lagging clock timing (c) optimum clock timing



(a)

TX pre-emphasis strength [dB]	1.5	3	4.5	6
Pulse width of data "H' [ps]	234.29	241.93	***251.05***	261.01
Pulse width/1UI	0.93716	0.96772	***1.0042***	1.04404

(b)

그림 11. (a) 1-비트 펄스 응답 (b) 송신회로의 프리엠퍼시스 강도에 따른 1-비트 펄스 폭

Fig. 11. (a) 1-bit pulse response (b) 1-bit pulse width according to TX pre-emphasis strength.

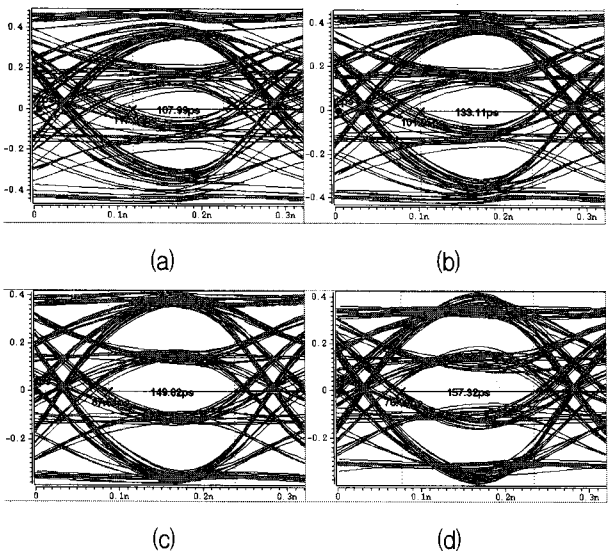


그림 12. 송신회로 프리엠퍼시스 강도에 따른 4-레벨 펄스진폭변조의 eye 다이어그램 (a) 1.5dB (b) 3.0 dB (c) 4.5dB (d) 6.0dB

Fig. 12. 4-PAM eye diagram according to TX pre-emphasis strength (a) 1.5dB (b) 3.0 dB (c) 4.5dB (d) 6.0dB

10 shows the integrated values of *VI0* and *VI1* by timing relation between data pattern and integrating clock. The timing of the integrating clock is adjusted until the integrated values (*VI0, VI1*) of two patterns are equal.

In a DRAM channel shown in Fig. 1(a), the pulse width measured at RX input increase as the strength of TX pre-emphasis increase, as shown in Fig. 11. The measured pulse width of 1-bit pulse was about 1UI when TX pre-emphasis was 4.5dB. This simulation result for optimum TX pre-emphasis is equal to the result of eye diagram generated by random data transmitted from TX, as shown in Fig. 12.

Ⅳ. Conclusion

An 8-channel, 8-Gb/s/channel asymmetric 4-PAM transceiver was designed for a main memory DRAM by using 70nm DRAM process with 1.35V supply. The proposed asymmetric 4-PAM has the larger voltage magnitude of upper and lower eyes than the voltage magnitude of center eye. This scheme reduced 33% of the effect of reference noise in a receiver and increased time margin compared to a conventional 4-PAM. Also, the adaptive TX pre-emphasis scheme for a main memory DRAM was proposed. For this scheme, the ISI detection scheme with clock time calibration was proposed and was achieved by measuring 1-bit lone pulse.

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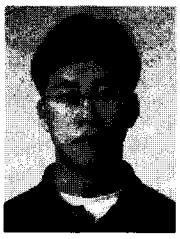

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