

# Non-Overlapped Single/Double Gate SOI/GOI MOSFET for Enhanced Short Channel Immunity

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**Abstract**— In this paper we analyze the influence of source/drain (S/D) extension region design for minimizing short channel effects (SCEs) in 25 nm gate length single and double gate Silicon-on-Insulator (SOI) and Germanium-on-Insulator (GOI) MOSFETs. A design methodology, by evaluating the ratio of the effective channel length to the natural length for the different devices (single or double gate FETs) and technology (SOI or GOI), is proposed to minimize short channel effects (SCEs). The optimization of non-overlapped gate-source/drain i.e. underlap channel architecture is extremely useful to limit the degradation in SCEs caused by the high permittivity channel materials like Germanium as compared to that exhibited in Silicon based devices. Subthreshold slope and Drain Induced Barrier Lowering results show that steeper S/D gradients along with wider spacer regions are needed to suppress SCEs in GOI single/double gate devices as compared to Silicon based MOSFETs. A design criterion is developed to evaluate the minimum spacer width associated with underlap channel design to limit SCEs in SOI/GOI MOSFETs.

**Index Terms**—Silicon-on-Insulator (SOI), Germanium-on-Insulator (GOI), single gate MOSFET, double gate MOSFET, gate-underlap design, source/drain (S/D) profile optimization, short channel effects (SCEs), low-voltage applications

## I. INTRODUCTION

Over the past few years fully depleted (FD) Silicon-on-Insulator (SOI) based single and multiple gate MOSFETs have emerged as possible candidates for device scaling at the end of ITRS roadmap [1]. Amongst the many possible candidates for scaling, double-gate silicon (DG) MOSFETs are considered to possess appropriate features to constitute devices for nanoscale circuit design because of the excellent suppression of short-channel effect (SCEs), lower gate leakage current, higher on-current, and better subthreshold slope values [2, 3]. DG MOSFETs can be fabricated with their channel in the plane of the wafer or as vertical structures. DG devices in the standard configuration have exhibited record currents [4] whereas other topologies such as the pillar FET [5] or the FinFET [6-9] are much easier to integrate. As the body thickness is controlled by lithographic and etching processes, it will be increasingly difficult to fabricate vertical devices with ultra thin silicon films. The problem of access resistance is more severe in vertical FETs because they lack the equivalent of deep source/drain region that makes the formation of low resistance silicide contacts possible [10, 11]. The planar fabrication approach does allow fabricating ultra thin body devices, a key requirement for suppressing SCEs. Controlling the width uniformity of a relatively tall fin structure (50-60 nm) and then attaining a smooth fin surface on the roughest plane (110) on the silicon substrate are the crucial challenges. It has also been shown that fins with tapered bottom profile degrades SCEs, produces a non-uniform current flow and current crowding in the vertical direction [12]. In addition, the mobility of an aggressively scaled channel greatly depends on surface roughness-induced scattering.

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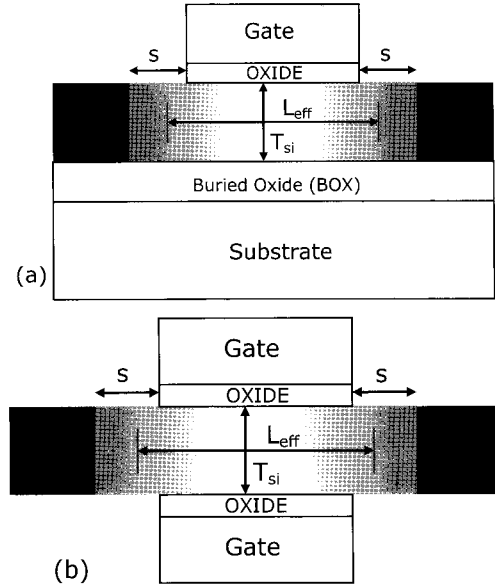
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In addition to changing the transistor architecture, channel engineering has been an attractive option to enhance device performance. One such concept of channel engineering is the use of “non-overlapped” or “underlapped” gate–source/drain structure with low-doped/intrinsic channel [13] to facilitate MOS scaling to nanoscale gate lengths. In gate-underlap architecture, source/drain (S/D) extension region profiles are designed such that the extension region doping does not approach the gate edge i.e. the channel and extension regions adjacent to the gate will be without any dopant. The concept of underlapped channel design has been experimentally applied in bulk – MOSFETs [14] and vertical FinFETs [15], multi-bridge-channel FETs [16], for digital applications and planar single gate (SG) SOI MOSFETs [17] for ultra-low-voltage analog/rf applications. Published work on underlap MOSFETs has shown great potential for digital [18-29] and analog/rf applications [30-33].

Recently, Germanium (Ge) has re-attracted interest for high-performance devices because of its much higher intrinsic electron and hole mobility compared with silicon [34-36]. The major problem of Ge CMOS device fabrication is the thermal and chemical instability of Ge oxides as gate dielectrics since Ge native oxides give rise to rough surface and high density of interface states [37, 38]. The best dielectrics for use in Ge MOSFETs are Ge oxynitrides, which have better stability than native Ge oxides [39]. The recent development of dielectric films with high dielectric constants to replace  $\text{SiO}_2$  in Si MOSFETs becomes promising in implementing such dielectrics in Ge MOSFETs. Single gate Ge MOSFETs with various gate dielectrics (Ge oxynitride and high- $\kappa$ ) have been manufactured and measured recently [40-44]. The improved performance of Ge MOSFETs with greater mobility than Si MOSFETs was demonstrated using high- $\kappa$  gate dielectrics [35]. Therefore, it is worthwhile to raise the possible advantages of replacing Si with Ge in future DG MOSFETs. In this paper, Ge based SG or DG devices have been referred as Germanium-on-Insulator (GOI).

In this paper, we use the expression of effective channel length for gate–source/drain underlap devices and natural/characteristic length scale for single and double gate SOI/GOI MOSFETs to evaluate the design criterion to suppress SCEs. Our earlier work [29] highlighted the usefulness of lateral S/D doping gradient



**Fig. 1.** Schematic diagram of (a) single gate (SG) SOI MOSFET and (b) double gate (DG) SOI MOSFET.

along with S/D roll-off width to suppress short channel effects in SOI devices. In this work, we highlight the usefulness of underlap channel profile to suppress short channel effects in GOI based SG/DG MOSFETs. Optimal design guidelines are proposed for 25 nm underlap channel single/double gate SOI/GOI MOSFETs to suppress SCEs based on the ratio of effective channel length to natural/characteristic length. The present work provides valuable design insights in the performance of nanoscale DG SOI/GOI devices with optimal S/D engineering and serves as a tool to optimise important device and technological parameters for low power 45 and 32 nm technology nodes.

## II. RESULTS AND DISCUSSION

### 1. Natural length scale ( $\lambda$ ) and effective channel length ( $L_{eff}$ )

As demonstrated in [2, 45-50] and our earlier paper [29], the natural length governs the influence of lateral field on the channel potential and influences the extent of short channel effects (SCEs) inherent to a structure. The natural length depends on device geometry and boundary conditions. Using the same approach as described in our earlier work [29], the eigenvalue equation

determining the natural length for single gate (SG) SOI MOSFETs is given as

$$\tan(k_{nSG\_SOI} \varepsilon_{si}) = \frac{(C_{fox} + C_{box}) k_{nSG\_SOI} \varepsilon_{si}}{k_{nSG\_SOI}^2 \varepsilon_{si}^2 - C_{fox} C_{box}} \quad (1)$$

where  $k_{nSG\_SOI}$  are the eigenvalues for single gate SOI devices,  $C_{fox} (= \varepsilon_{ox}/T_{fox})$  is the front oxide capacitance,  $C_{box} (= \varepsilon_{ox}/T_{box})$  is the back/buried oxide capacitance,  $T_{si}$  is the silicon film thickness,  $T_{fox}$  is the front oxide thickness,  $T_{box}$  is the buried oxide thickness and  $\varepsilon_{ox}$  is the permittivity of oxide. The relationship between eigenvalue and natural length is described later. Similarly, for a double gate (DG) SOI MOSFETs, the eigenvalue equation is obtained as

$$\tan(k_{nDG\_SOI} \varepsilon_{si}) = \frac{(2 C_{ox}) k_{nDG\_SOI} \varepsilon_{si}}{k_{nDG\_SOI}^2 \varepsilon_{si}^2 - C_{ox}^2} \quad (2)$$

where  $k_{nGG\_GOI}$  is the eigenvalue for double gate SOI device. For Germanium-on-Insulator (GOI) based SG and DG devices the eigenvalue equation is obtained as

$$\tan(k_{nSG\_GOI} \varepsilon_{Ge}) = \frac{(C_{fox} + C_{box}) k_{nSG\_GOI} \varepsilon_{Ge}}{k_{nSG\_GOI}^2 \varepsilon_{Ge}^2 - C_{fox} C_{box}} \quad (3)$$

$$\tan(k_{nDG\_GOI} \varepsilon_{Ge}) = \frac{(2 C_{ox}) k_{nDG\_GOI} \varepsilon_{Ge}}{k_{nDG\_GOI}^2 \varepsilon_{Ge}^2 - C_{ox}^2} \quad (4)$$

where  $k_{nSG\_GOI}$  and  $k_{nGG\_GOI}$  are the eigenvalues for single and double gate GOI devices, respectively. The natural length ( $\lambda_n$ ) can be obtained for SG/DG SOI/GOI MOSFETs as  $\lambda_n = n\pi/k_n$  [50] where  $k_n$  represents the eigenvalue determined from eqns. (1)–(4) for different types of devices.

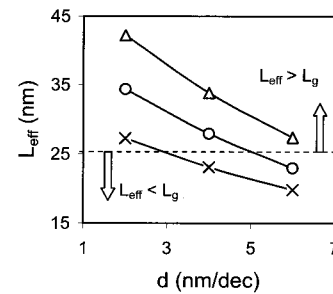
To design a device free of short channel effects (SCEs), the minimum channel potential should be as small as possible [2, 29, 48-50]. This minimum channel potential can be decreased by increasing the channel doping or by reducing the natural length ( $\lambda_n$ ) (or increasing the eigenvalue,  $k_n$ ). Reduction of  $\lambda_n$  reduces the minimum channel potential in a much efficient manner as compared to increasing the doping which is mainly done to adjust the threshold voltage. Since  $\lambda_n$  depends on  $T_{si}$  and  $T_{ox}$ , it provides a measure of short channel effects in a given structure and thus can be interpreted as the short channel immunity factor of a given structure [29].

A smaller value of  $\lambda_n$  implies thin silicon film, thin gate oxide, lower permittivity for channel material i.e. improved gate controllability and advanced device architecture (double instead of single). Thus, as device dimensions penetrate into nanoscale regime, a smaller value of  $\lambda_n$  is required to operate the device as in the long channel regime by increasing the  $L_{eff}/\lambda_n$  ratio [2, 29, 48-50]. Since the first root of eigenvalue equations described above is sufficient to describe SCEs in different devices, we will only focus on the lowest eigenvalue ( $\lambda_1 = n\pi/k_1$ ) in our analysis.

In the present work, we have modeled the effective channel length in gate-source/drain underlap devices (SG/DG SOI/GOI FETs) using the expression presented in [24] and is given as

$$L_{eff} = L_g + 2s \left( 1 - \sqrt{\frac{2/\ln(10)}{s/d}} \sqrt{\ln\left(\frac{N_{SDO}}{\eta_{SD}}\right)} \right) \quad (5)$$

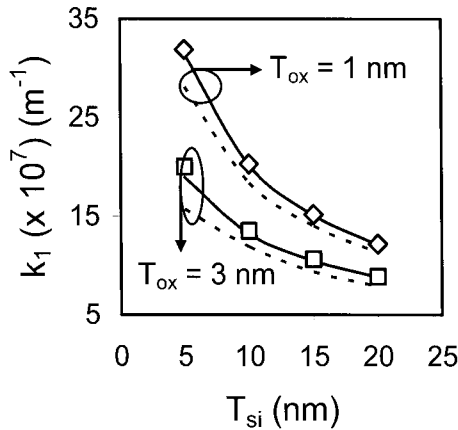
where  $\eta_{SD}$  is the S/D doping level at which  $L_{eff}$  is extracted,  $L_g$  is the gate length,  $s$  is the S/D roll-off width (also called as the spacer width),  $d$  is the S/D doping gradient (expressed in nm/decade) evaluated at the gate edge as  $d = 1/dN_{SD}(x)/dx$ . S/D profile was modeled using the expression  $N_{SD}(x) = N_{SDO} \exp(-x^2/\sigma^2)$  where  $N_{SDO}$  is the peak S/D doping and  $\sigma$ , lateral straggle parameter, governs the S/D profile roll-off ( $\sigma = \sqrt{2sd/\ln(10)}$ ) [24] in the channel direction. Although underlap design can limit SCEs due to longer  $L_{eff}$  (as compared to conventional overlap design), an underlap device with a very wide spacer can result in an additional parasitic series resistance. This series resistance will not significantly degrade the device performance if operated at lower drive currents and voltages i.e. underlap design is most useful for low voltage/power applications.



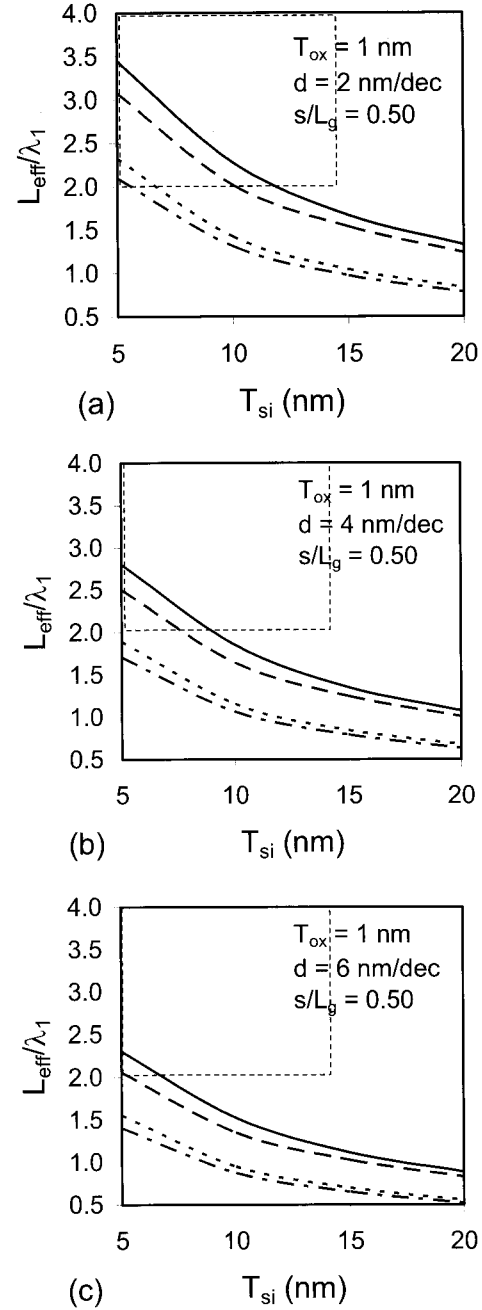
**Fig. 2.** Variation of effective channel length ( $L_{eff}$ ) with S/D doping gradient ( $d$ ) for various values of spacer widths. Notations:  $\times$ — $\times$ :  $s/L_g = 0.25$ ,  $o$ — $o$ :  $s/L_g = 0.50$ ,  $\Delta$ — $\Delta$ :  $s/L_g = 0.75$ .

Fig. 2 shows the variation of effective channel length ( $L_{\text{eff}}$ ) on S/D doping gradients. A variation of S/D roll-off widths ( $s$ ) along with lateral S/D doping gradient ( $d$ ) results in the modulation of effective channel length ( $L_{\text{eff}}$ ) in a nanoscale non-classical (gate underlap) single and double gate MOSFET. Wider roll-off widths along with steeper doping gradient (lower  $d$  values) result in a longer  $L_{\text{eff}}$  whereas a shorter spacer width along with gradual doping gradient (higher  $d$  values) yields shorter  $L_{\text{eff}}$ . It is important to note that the optimisation of  $s$  and  $d$  for short channel immunity must be considered along with transistor structural parameters for single and double gate MOSFETs.

Fig. 3 shows the comparison between the eigenvalues determined by our approach and using the expression in [50]. Our results are in good agreement with those derived by Frank *et al.* [50] by solving the 2D Poisson's equation in the oxide and silicon regions. This shows that for the device parameters considered in the present work, solving the 2D Poisson's equation only in the silicon film itself is sufficient to provide a reasonable estimation of SCEs in DG MOSFETs. We have restricted our analysis to a dielectric with permittivity of  $3.9 \epsilon_0$  ( $\epsilon_0$  is the permittivity of free space) as gate dielectric and therefore eqns. (2)–(5) are reasonable to estimate the natural/characteristic length in a given structure.



**Fig. 3.** Dependence of lowest eigenvalue ( $k_1$ ) for DG MOSFET on silicon film thickness ( $T_{\text{si}}$ ) for various values of gate oxide thickness ( $T_{\text{ox}}$ ). Symbols represent  $k_1$  values calculated for DG SOI MOSFETs by equation in [50] whereas solid lines represent  $k_1$  values for DG SOI MOSFETs evaluated by eq. (3) and dotted lines denote  $k_1$  values for DG GOI MOSFETs calculated by eq. (5) in the present work. Notations:  $\diamond$   $T_{\text{ox}} = 1$  nm and  $\square$   $T_{\text{ox}} = 3$  nm.  $T_{\text{box}} = 25$  nm for SG devices.



**Fig. 4.** Dependence of  $L_{\text{eff}}/\lambda_1$  ratios for SG/DG SOI/GOI MOSFET on silicon film thickness ( $T_{\text{si}}$ ) for (a)  $d = 2$  nm/dec, (b)  $d = 4$  nm/dec and (c)  $d = 6$  nm/dec. Notations: — DG SOI FET, --- DG GOI FET, ..... SG SOI FET and -.- SG GOI MOSFET.  $T_{\text{box}} = 25$  nm for SG devices. The dashed rectangle denotes the region where  $L_{\text{eff}}/\lambda_1 > 2$ .

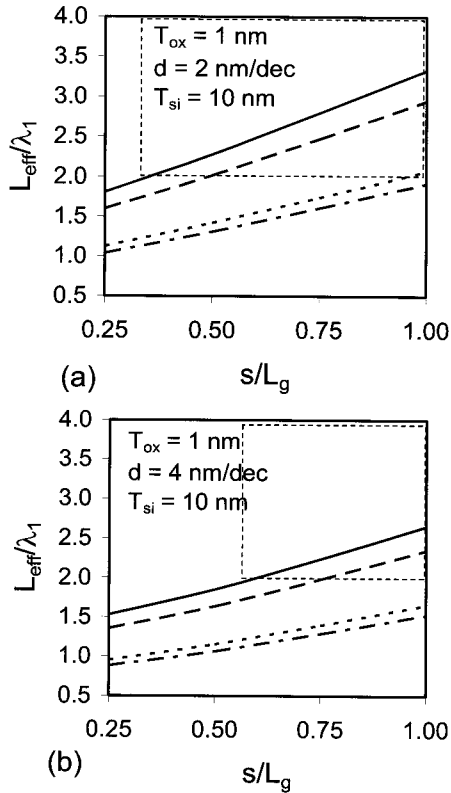
Fig. 4 shows the dependence of  $L_{\text{eff}}/\lambda_1$  on silicon film thickness ( $T_{\text{si}}$ ) for various doping gradients and devices. Largest  $L_{\text{eff}}/\lambda_1$  ratio is obtained at lower  $d$  values because of the greater contribution of spacer regions to the effective channel length. The lower permittivity of Si

yields lower natural length scale ( $\lambda_1$ ) value as compared to that achieved with Ge i.e.  $(\lambda_1)_{\text{DG-SOI}}/(\lambda_1)_{\text{DG-GOI}} \cong 0.88$  at  $s/L_g = 0.50$  and is independent of  $d$ . Similar values ( $\sim 0.88$ ) are also observed for SG devices. Since SG/DG devices should be designed such that  $L_{\text{eff}}/\lambda_1 > 2$  to avoid short channel effects, S/D design with  $d = 6$  nm/dec (S/D dopant spill into the channel as spacer is not wide enough) will not be useful in nanoscale devices.

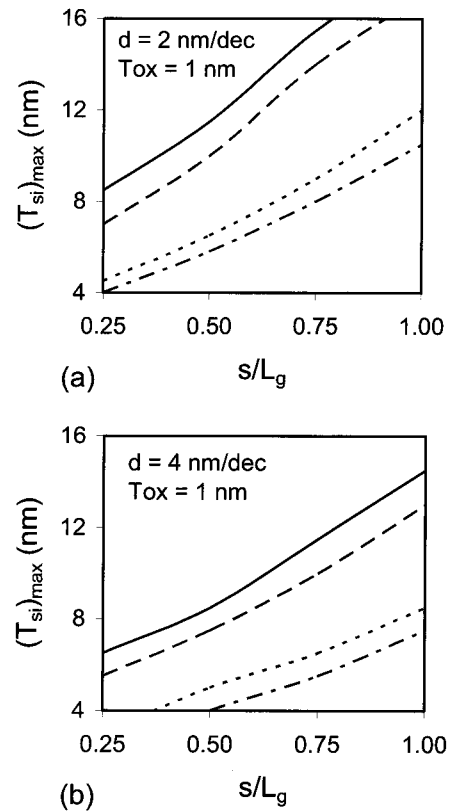
Fig. 5 shows the dependence of  $L_{\text{eff}}/\lambda_1$  on  $s/L_g$  values for two different doping gradients and various devices (SG/DG and SOI/GOI). Wider spacers or larger  $s/L_g$  values result in longer effective channel length values and lead to higher  $L_{\text{eff}}/\lambda_1$  values for all devices. SG underlap devices designed with gradual S/D profiles i.e. higher  $d$  values will exhibit significant SCEs as  $L_{\text{eff}}/\lambda_1$  is lower than 2 even for  $s/L_g \sim 1$ . DG SOI devices should be designed with  $s/L_g > 0.4$  in order to achieve  $L_{\text{eff}}/\lambda_1 = 2$  at  $d = 2$  nm/dec whereas to attain the same degree

of suppressed SCEs in DG GOI devices ( $L_{\text{eff}}/\lambda_1 = 2$ ),  $s/L_g$  should be maintained around 0.5. Therefore, GOI devices will require wider spacers in comparison to SOI MOSFETs for attaining the same degree of short channel immunity. At higher S/D gradients, DG SOI devices should be designed such that  $s/L_g > 0.6$  whereas GOI based DG devices should have a minimum spacer width of  $0.7L_g$ .

Fig. 6 shows the requirement for selecting silicon film thickness for various  $s/L_g$  and  $d$  values such that  $L_{\text{eff}}/\lambda_1 = 2$  i.e. devices are designed to be immune from SCEs. As shown in the figure, DG SOI MOSFETs show greater flexibility in the choice of  $T_{\text{si}}$  as compared to SG devices. For a typical S/D profile with  $d = 2$  nm/dec and  $s/L_g = 0.5$ , DG SOI devices require maximum  $T_{\text{si}}$  of  $\sim 13$  nm whereas DG GOI devices should be designed with  $(T_{\text{si}})_{\text{max}}$  of 10 nm to achieve similar levels of short channel immunity. In case of SG devices, the range of  $T_{\text{si}}$  values is limited to 6 and 5 nm in SOI and GOI devices, respectively. The maximum allowable  $T_{\text{si}}$  value reduces



**Fig. 5.** Dependence of  $L_{\text{eff}}/\lambda_1$  ratios for SG/DG SOI/GOI MOSFET on spacer to gate length ratio ( $s/L_g$ ) for (a)  $d = 2$  nm/dec and (b)  $d = 4$  nm/dec. Notations: — DG SOI FET, - - DG GOI FET, ..... SG SOI FET and - · - · SG GOI MOSFET.  $T_{\text{box}} = 25$  nm for SG devices.



**Fig. 6.** Maximum allowable film thickness  $(T_{\text{si}})_{\text{max}}$  as a function of spacer to gate length ratio ( $s/L_g$ ) for (a)  $d = 2$  nm/dec and (b)  $d = 4$  nm/dec. Notations: — DG SOI FET, - - DG GOI FET, ..... SG SOI FET and - · - · SG GOI MOSFET.  $T_{\text{box}} = 10$  nm for SG devices.

if a gradual S/D profile ( $\sim 4$  nm/dec) is used instead of a steeper S/D profile. It is evident from these results that in order to improve the scalability and short channel immunity in SG devices, silicon film thickness must be reduced and/or spacer width be increased (at a constant  $d$ ). Reducing film thickness involves the problem of producing a thin, defect free and uniform mono-crystalline silicon layer ( $<10$  nm), which is a technological issue. The use of underlap design is beneficial as it allows the use silicon films  $> 8$  nm in SOI/GOI DG devices without compromising the electrostatic integrity of the device.

In order to design devices with suppressed SCEs,  $L_{\text{eff}}/\lambda_1$  should be greater or equal to 2 [29]. The first step in selecting the device and S/D profile parameters is the evaluation of  $L_g/\lambda_1$ . If this ratio is 2, the device will be immune from SCEs and underlap channel design should be avoided as it will add extra series resistance (due to the contribution of non-overlapped gate-S/D regions) which will degrade the performance for above threshold operation. If the term  $L_g/\lambda_1$  is less than 2, the additional contribution of S/D regions to achieve  $L_{\text{eff}}/\lambda_1 = 2$  should be computed as  $\Theta = 2 - (L_g/\lambda_1)$ . The minimum spacer width,  $(s)_{\text{min}}$  associated with the underlap profile to achieve immunity from SCEs can be computed as

$$(s)_{\text{min}} = \frac{\lambda_1 \Theta}{2} + \sqrt{(s)_{\text{min}}} \left( \sqrt{\ln\left(\frac{N_{\text{SDO}}}{\eta_{\text{SD}}}\right)} \sqrt{\frac{2d}{\ln(10)}} \right) \quad (6)$$

$\lambda_1$  in the above equation depends on device geometry and will be different for SG/DG SOI/GOI devices. This equation allows for an efficient estimation of the S/D profile requirements to limit SCEs for a given topology. As shown in Fig. 7, lower  $(s)_{\text{min}}$  values are required for thin silicon films and lower S/D doping gradients. Selecting a device geometry (SG or DG) or even a technology (SOI or GOI) will only change the value of  $\Theta$  but the variation of  $(s)_{\text{min}}$  with  $\Theta$  will remain the same i.e.  $(s)_{\text{min}}$  data points lie on the same curve (for a given  $d$  value). For example designing DG devices with  $T_{\text{ox}} = 1$  nm and  $T_{\text{si}} = 10$  nm results in  $\lambda_1$  of 15.5 nm and 20.8 nm for SOI and GOI technology, respectively. These values translate into  $\Theta$  values of 0.384 and 0.798 which correspond to  $(s)_{\text{min}}$  of 9.6 nm (SOI) and 18.2 nm (GOI) respectively for  $d = 2$  nm/dec. It is advisable to compute

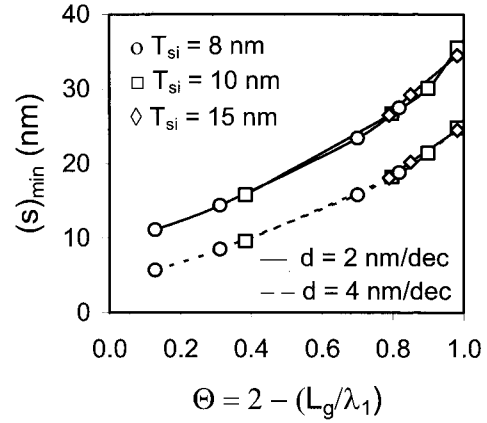


Fig. 7. Minimum spacer width to achieve immunity from short channel effects as a function of  $d$  and  $T_{\text{si}}$ .

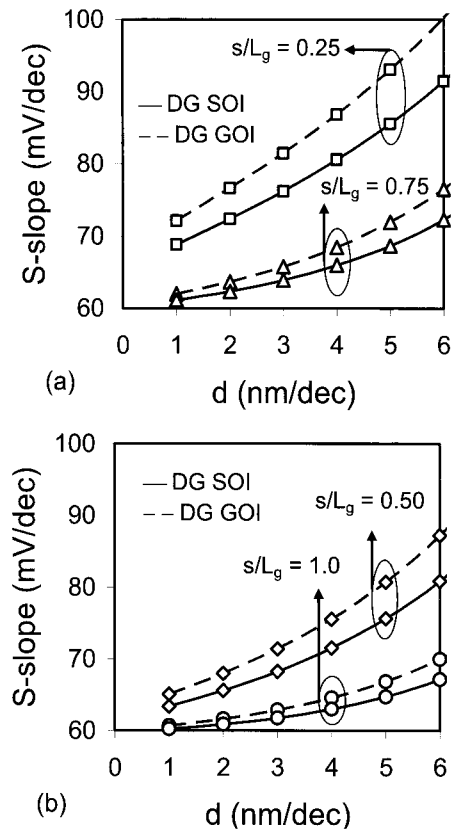


Fig. 8. Dependence of Subthreshold slope ( $S$ -slope) on doping gradient for DG SOI and DG GOI devices for (a)  $s/L_g = 0.25$  and  $s/L_g = 0.75$  and (b)  $s/L_g = 0.50$  and  $s/L_g = 1.0$ . Parameters:  $T_{\text{ox}} = 1.3$  nm,  $N_a = 10^{15} \text{ cm}^{-3}$ ,  $T_{\text{si}} = 10$  nm and  $V_{\text{ds}} = 50$  mV. The reference  $S$ -slope values for DG SOI devices are taken from [24].

$s$  in a given underlap design instead of  $d$  as it is dependent on the process and quite difficult to change. Equation (6) provides a simple and effective method of estimating the minimum spacer width for a given device/technology and yielding a device design with

immunity from short channel effects.

By adopting the similar procedure as described in [24, 46-47], the expression of minimum channel potential ( $\Psi_m$ ) can be derived i.e. eq. (A3) of [24]. The carrier density ( $n_m$ ) at the position of minimum channel potential ( $x_{\min}$ ) is given as  $n_m = (n_i^2/N_a)\exp(q\Psi_m/kT)$  where  $n_i$  is the intrinsic carrier concentration,  $N_a$  is the film doping,  $q$  is the electron charge,  $k$  is the Boltzmann constant and  $T$  is the temperature. Assuming that the Subthreshold slope ( $S$ -slope) is related to carrier concentration at  $x_{\min}$  (and hence to the  $\Psi_m$ ) [46-47, 51-53],  $S$ -slope can be obtained as  $\partial V_{gs}/\partial \log I_{ds} \approx \ln(10) \partial V_{gs}/\partial \ln(n_m) \approx \ln(10) (kT/q) (\partial \Psi_m/\partial V_{gs})^{-1}$ . This expression for evaluating  $S$ -slope has been widely used in several prior published papers [24, 46-47, 51-55].

The threshold voltage ( $V_{TH}$ ) can be defined as the gate voltage at which the minimum sheet density of inversion carriers reaches a value  $Q_{TH}$  [56] adequate for identifying the turn-on condition, which can be approximated as

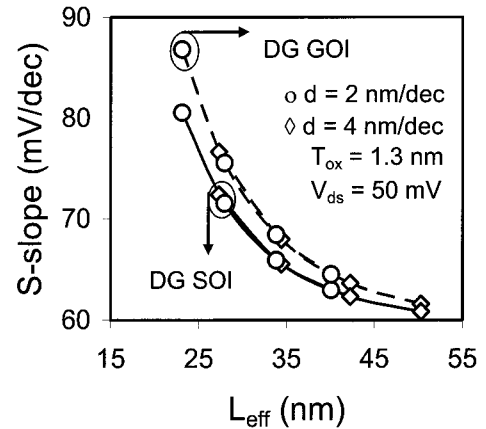
$$Q_{TH} = \int_0^{T_{si}} n_i \exp(q\Psi_m/kT) dy$$

At the position of minimum channel potential,  $Q_{TH}$  can be approximated [56] as  $\Psi_m = \left( \frac{kT}{q} \right) \left( \ln \left( \frac{Q_{TH}}{n_i T_{si}} \right) \right)$ , with  $Q_{TH} = 5.5 \times 10^{10} \text{ cm}^{-2}$  [55]. In terms of the classical method of determining the threshold voltage i.e. by equating the minimum channel potential,  $\Psi_m$  to  $\kappa\phi_f$  (where  $\kappa$  is a fitting parameter,  $\phi_f$  is the Fermi potential),  $Q_{TH}$  value reported above corresponds to  $\kappa = 1.35$ . The parameter  $Q_{TH}$  (or  $\kappa$ ) relates to the current level used in experimental characterization of threshold voltage. It should be noted that  $\kappa$  is lower than the classical value of 2 for bulk MOS devices. The use of minimum channel potential, obtained via the analytical solution of the Poisson's equation, to evaluate threshold voltage is a well defined technique and has been reported in several published papers [24, 51-57].

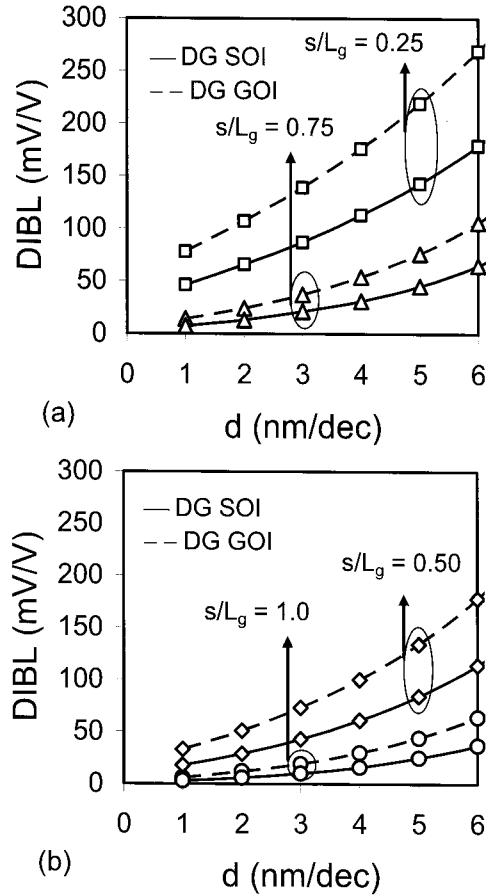
The natural length analysis is extended to evaluate the Subthreshold slope ( $S$ -slope) and Drain Induced Barrier Lowering ( $DIBL$ ) for DG devices using the expressions proposed by Kranti *et al.*, [24]. For a fair comparison between DG SOI and DG GOI MOSFETs, all device

parameters are kept the same for both types of devices, except for the Ge intrinsic doping concentration of  $n_{iGe} = 2 \times 10^{13} \text{ cm}^{-3}$  affecting the built-in potential across the source/drain-channel junctions and the dielectric constant  $\epsilon_{Ge} = 16\epsilon_0$  ( $\epsilon_0$  is the permittivity of free space) affecting the natural channel length  $k_{nDG\_GOI}$ . As shown in Fig. 8, S/D doping gradient must be maintained below 3 nm/dec for GOI devices whereas higher  $d$  value of 4 nm/dec is required to achieve  $S$ -slope lower than 80 mV/dec for  $s/L_g = 0.25$ . An increase in  $s/L_g$  to 0.50 relaxes the constraint on  $d$  from 3 to 5 for GOI and from 4 to 5 for SOI devices to achieve  $S$ -slope of 80 mV/dec. Wider spacers ( $s/L_g > 0.5$ ) can achieve lower  $S$ -slope values independent of  $d$ . Targeting an S/D process with  $d = 3 \text{ nm/dec}$ ,  $s/L_g = 0.25$  can achieve  $S$ -slope = 80 mV/dec whereas larger spacers  $\sim 0.35L_g$  would be more appropriate for GOI devices for the same  $S$ -slope values.

Fig. 9 shows the dependence of  $S$ -slope on effective channel length ( $L_{eff}$ ) for SOI and GOI devices. Underlap design with gradual  $d$  values at narrow spacers achieves higher  $S$ -slope values due to a lower  $L_{eff}$  because of dopant spill into the channel. S/D design with  $d = 2 \text{ nm/dec}$  and  $s/L_g = 0.25$  yields  $L_{eff} = 24 \text{ nm}$  resulting in  $S$ -slope values of 87 mV/dec and 81 mV/dec for GOI and SOI DG MOSFETs i.e. 6 mV/dec higher  $S$ -slope for GOI devices. For longer channel lengths ( $\sim 40 \text{ nm}$ ), the difference between  $S$ -slope values for GOI and SOI



**Fig. 9.** Dependence of Subthreshold slope ( $S$ -slope) on effective channel length ( $L_{eff}$ ) for DG SOI and GOI devices. The maximum  $S$ -slope value corresponding to a particular  $d$  value corresponds to  $s/L_g = 0.25$  whereas the minimum  $S$ -slope value signifies  $s/L_g = 1.0$ . The reference  $S$ -slope values for DG SOI devices are taken from [24]. Parameters are same as in Fig. 8.



**Fig. 10.** Dependence of Drain Induced Barrier Lowering (*DIBL*) on doping gradient for DG SOI and DG GOI devices for (a)  $s/L_g = 0.25$  and  $s/L_g = 0.75$  and (b)  $s/L_g = 0.50$  and  $s/L_g = 1.0$ . Parameters are same as in fig. 8. The reference *DIBL* values for DG SOI devices are taken from [24].  $DIBL = |(V_{th1} - V_{th2}) / (V_{ds1} - V_{ds2})|$  where  $V_{th1}$  and  $V_{th2}$  are threshold voltages extracted at drain bias of ( $V_{ds1}$ ) 50 mV and ( $V_{ds2}$ ) 1.0 V.

devices reduces to 2 mV/dec with both exhibiting ideal values of 60 mV/dec for  $L_{eff} > 50$  nm.

Fig. 10 shows the dependence of *DIBL* on S/D doping gradient ( $d$ ) for SOI and GOI devices. A target *DIBL* = 100 mV/V for nanoscale devices can be achieved for very steep S/D gradient ( $d \leq 2$  nm/dec) in GOI devices whereas a slightly higher value of  $d = 3$  nm/dec can still achieve the same *DIBL* for SOI DG MOSFETs. A wider spacer of  $0.5L_g$  relaxes the constraint on S/D doping gradient for SOI and GOI devices. DG SOI devices should be designed with  $d < 4$  nm/dec and 5 nm/dec for GOI and SOI devices respectively with  $s/L_g = 0.5$  to achieve *DIBL* of 100 mV/V. Underlap S/D design can be utilized to limit short channel effects in SOI/GOI devices and achieve reasonable values of *S*-slope and *DIBL*.

### III. CONCLUSIONS

A comprehensive analysis to limit short channel effects in single and double gate SOI/GOI MOSFETs, based on the ratio of effective channel length to natural length, has been presented. Results suggest that GOI based devices exhibit higher degree of short channel effects as compared to SOI based MOSFETs. Underlap channel design defined by spacer width, S/D doping gradient and lateral straggle offer additional degree of freedom apart from transistor structural parameters to design devices with immunity to short channel effects. Underlap channel design is particularly useful in suppressing short channel effects in GOI based devices with silicon films  $> 8$  nm. DG SOI MOSFETs offer maximum flexibility in selecting silicon film thickness and lowest spacer width at a given S/D doping gradient when compared to single gate SOI MOSFETs and GOI based single/double gate MOSFETs. Reasonable values of *S*-slope and *DIBL* can be achieved in underlap channel GOI DG devices. Results presented in this work will be useful in design and optimization of nanoscale single and double gate SOI/GOI MOSFETs for low voltage applications.

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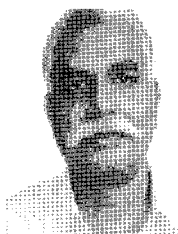
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