Inductorless 8.9 mW 25 Gb/s 1:4 DEMUX and 4 mW 13 Gb/s 4:1 MUX in 90 nm CMOS

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Abstract— **A low-power inductorless 1:4 DEMUX and a 4:1 MUX for a 90 nm CMOS are presented. The DEMUX can be operated at a speed of 25 Gb/s with the power supply voltage of 1.05 V, and the power consumption is 8.9 mW. The area of the DEMUX core is 29 × 40 μm^2. The operation speed of the 4:1 MUX is 13 Gb/s at a power supply voltage of 1.2 V, and the power consumption is 4 mW. The area of the MUX core is 30 × 18 μm^2. The MUX/DEMUX mainly consists of differential pseudo-NMOS. In these MUX/DEMUX circuits, logic swing is nearly rail-to-rail, and a low V_{dd}. The component circuit is more scalable than a CML circuit, which is commonly used in a high-performance MUX/DEMUX. These MUX/DEMUX circuits are compatible with conventional CMOS logic circuit, and it can be directly connected to CMOS logic gates without logic level conversion. Furthermore, the circuits are useful for core-to-core interconnection in the system LSI or chip-to-chip communication within a multi-chip module, because of its low power, small footprint, and reasonable operation speed.**

Index Terms—**MUX, DEMUX, low-power, high-speed, CMOS logic circuit, pseudo-NMOS**

I. INTRODUCTION

Currently used processors are required to handle ever-increasing amounts of data. Until recently, performance en hancement of processors was achieved by increasing the clock frequency. Presently, performance enhancement is achieved by integrating multiple cores on a chip and/or by stacking multiple chips in a package. Therefore, it is important to ensure efficient communication between cores and chips.

Owing to the recent advancement in packaging technology, various options for chip-to-chip communication in multi-chip modules have become available. However, it is not always practical or desirable to have parallel interconnects between chips except between a processor chip and memory chips. This is because upper level interconnects involving pads or through-substrate vias (TSVs) impose significant area penalty (e.g. [1]). For this reason, interconnects that are at a higher level up in the interconnect hierarchy, must be used sparingly. By using a serializer/deserializer (SerDes), high-bandwidth chip-to-chip communication can be effected even with limited interconnect resources. For this purpose, a low-power and high-speed SerDes is required.

The abovementioned requirement is very different from that for high-speed optical communication systems. Scalability is another important parameter that must be considered when a SerDes is designed with the aforementioned features. Ideally, the circuit design adopted should be suitable for a large number of technology generations; however, this is not always possible. Most CMOS implementations of high-speed SerDes are based on MOS current-mode logic (CML) [3, 4]. A schematic of a CML latch is shown in Fig. 1. Since CML is based on a differential amplifier, it has a constant current source, typically realized by a MOS transistor operating in the saturation region. In a 90-nm CMOS process, the voltage drop across the tail current source transistor can easily reach or beyond Vdd/2, while the voltage drop across the source-coupled pair may not be sufficient for proper operation.

To enhance the speed performance especially for optical communication systems, passive on-chip

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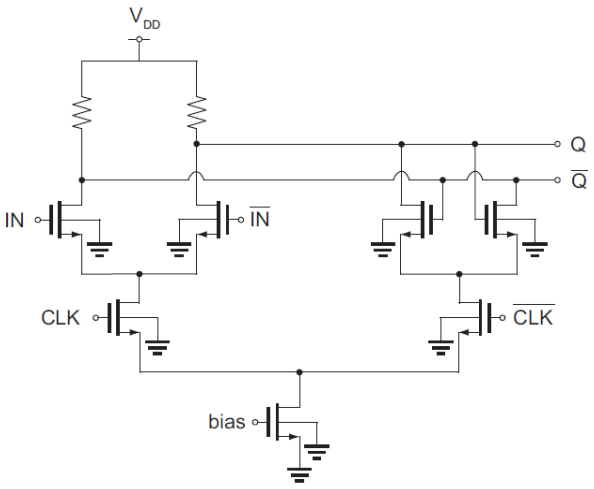

Fig. 1. Schematic of a Current-mode-logic-type D-latch.

inductors are recently used to cancel the capacitive components in the circuit and then extend the bandwidth [6, 14, 15]. However, the inductors occupy large chip areas that are not scalable along the CMOS process advancement. Therefore, inductorless SerDes is essential and desired especially in communication between cores and chips.

In this paper, we present differential-pseudo-NMOS logic type multiplexing (MUX) circuit as the serializer and demultiplexing (DEMUX) circuit as the deserializer which we believe are nearly as fast as circuits using a inductorless CML topology and more scalable than the latter. The differential pseudo-NMOS logic has a near rail-to-rail logic swing, as opposed to the low voltage swing in a typical CML circuit.

The rest of the paper is organized as follows. Section II presents the design of the basic circuit blocks used in the SerDes circuit, Section III describes the architecture of the proposed DEMUX and MUX. Section IV presents the measurement results as well as a comparison of the obtained results and the results of other studies. Section V includes concluding remarks.

II. Circuit Design

The components of the SerDes circuit, such as, the D flip-flop and frequency divider, consist of a combination of D-latches. In addition, the selector circuit which is the main circuit in the MUX comprises same logic style of D-latches. The performance of the D-latch circuit has a strong influence on the SerDes performance. In this study, we make use of the differential pseudo-NMOS logic style, which was proposed in [5], for the D-latches.

1. Differential-pseudo-NMOS-type D-latch

Fig. 2 shows the schematic of a differential-pseudo-NMOS-type D-latch. In a differential pseudo-NMOS-type D-latch, the tail current source transistor is eliminated as in [6, 7], and thus, voltage headroom becomes high. In addition, the load resistors are replaced with PMOS transistors operating in the triode region, as in the case of ordinary single-ended pseudo-NMOS logic circuit [8] as shown in Fig. 4. We refer to this type of load as a PMOS triode [9]. The area occupied by the loads is significantly reduced when PMOS triodes are used [5]. Furthermore, differential pseudo-NMOS-type D-latches operate with a near-rail-to-rail logic swing. The transistors that receive the clock signal are wide gate width, and the voltage drop across them is small. In the same manner, the selector circuit (Fig. 3) receives these favors.

Generally, logic circuits with a small logic swing operate faster than the circuit with a large logic swing. Hence, the main concern here is that our circuit with near-rail-to-rail logic swing might be rather slow. This is the case in a differential NMOS logic circuit with ordinary load resistors. Fig. 5 shows that the speed of a latch decreases with an increase in the logic swing. In contrast, the differential pseudo-NMOS logic circuit with the PMOS triode loads shows a very different behavior,

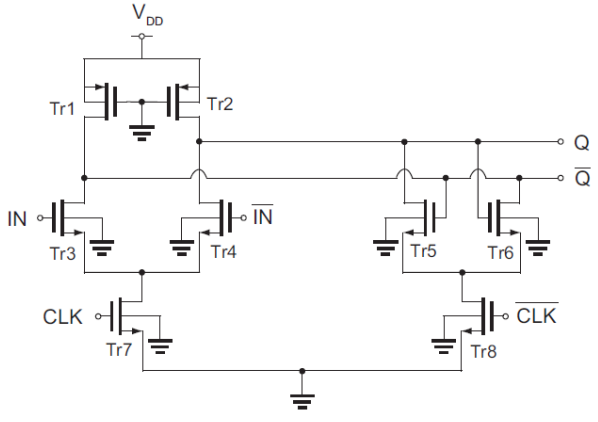

Fig. 2. Schematic of a differential pseudo-NMOS-logic-type D-latch.

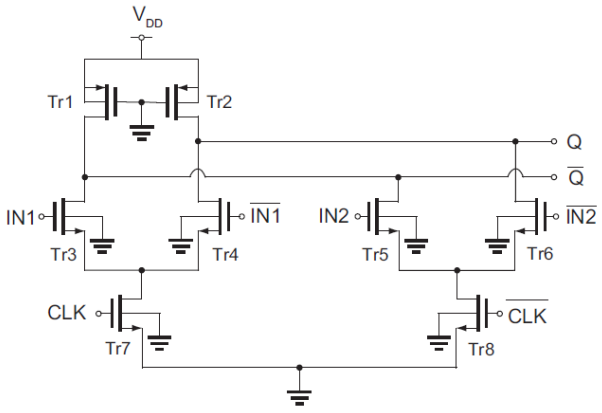

Fig. 3. Schematic of a Differential pseudo-NMOS logic style selector.

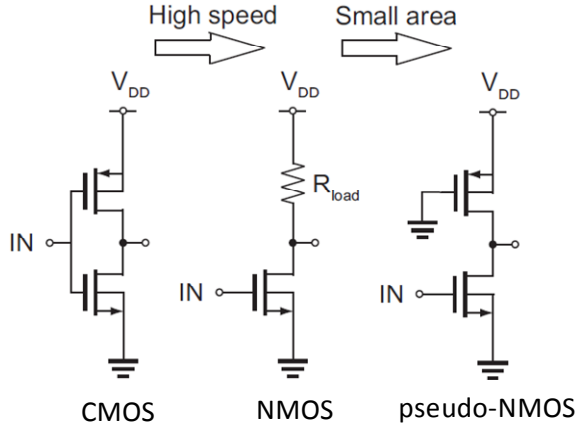

Fig. 4. Characteristics of pseudo-NMOS logic.

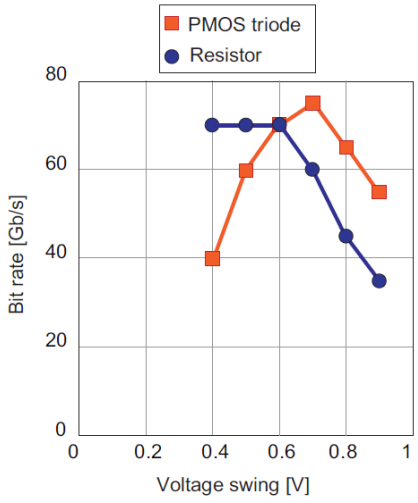

Fig. 5. Operation speed: PMOS triode vs. resistor.

as shown in red line in Fig. 5. When the voltage swing is small, the PMOS triode resistance is low. In this case, the PMOS size and the gate capacitance are large. Therefore, the operation speed of the differential pseudo-NMOS circuit is low when the voltage swing is small. However, when the voltage swing is almost rail-to-rail, the PMOS triode resistance is high, implying that the PMOS size and the gate capacitance are small. Therefore, the operation speed of the differential pseudo-NMOS is high. When the voltage swing exceeds 0.7 V, the large swing outweighs the advantages of the small PMOS size. In any case, when the voltage swing is near-rail-to-rail, the differential pseudo-NMOS latch with PMOS triode loads outperforms the differential NMOS latch with resistor loads.

2. Frequency Divider

Frequency divider is a component circuit of the SerDes. The SerDes has multi-phase clock architecture [5], and it is driven by 90-degree phase-shifted clock signals generated by the frequency divider from a half-rate clock. Hence, a high speed frequency divider is required for the SerDes. In this study, a master-slave type divider [10] consisting of two D-latches is used.

Fig. 6 shows the schematic of this divider. In the SerDes, a half-rate clock signal CLK is fed to the divider, and 90-degree phase-shifted outputs CLK1 and CLK2 are obtained.

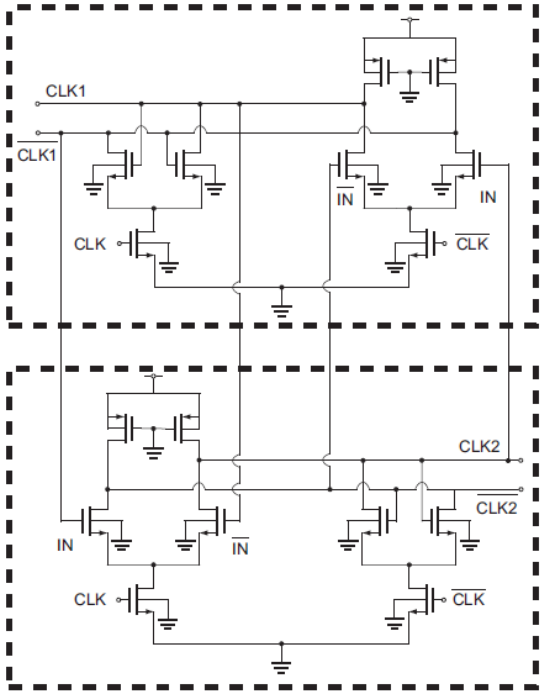

Fig. 6. Schematic of a divider.

III. ARCHITECTURE DESIGN

1. DEMUX Architecture

Fig. 7 shows the 1:4 DEMUX, which is based on a multiphase clock architecture [5], and Fig. 8 is showing a DEMUX timing chart. This architecture splits the input bit-stream into four output bit-streams by using the 90° phase-shifted clock signals generated by the frequency divider. High-speed serial input data is deserialized into four quarter-rate parallel output data streams.

Fig. 9 shows a chip micrograph of the 1:4 DEMUX fabricated by 90-nm CMOS process technology. The DEMUX comprises a clock divider, a clock buffer and the main DEMUX circuit consisting of D-latches. One of the four output bit-streams is chosen by the selector circuit, and the selected differential output signal is transformed into a single-ended signal before the output buffer. The area of the DEMUX circuit including the divider and clock buffer is as small as 29 × 40 μm^2.

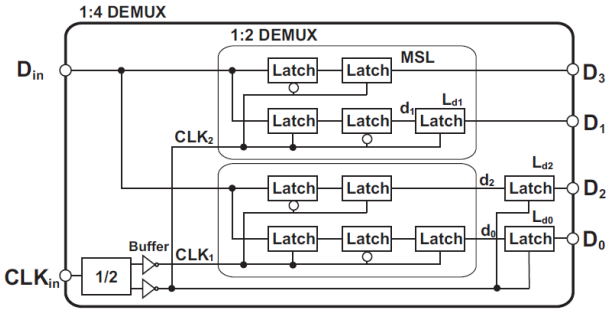

Fig. 7. DEMUX architecture.

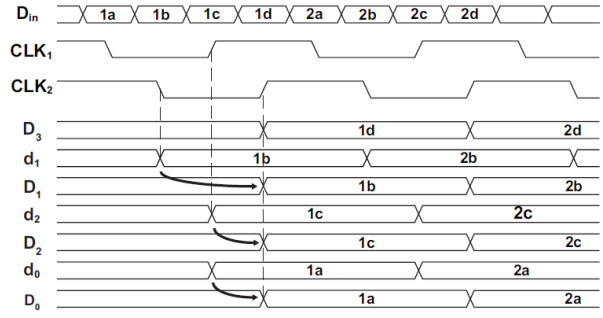

Fig. 8. DEMUX timing chart.

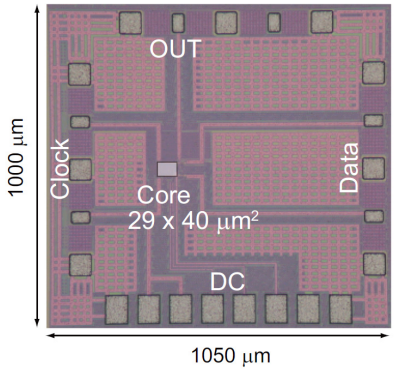

Fig. 9. Chip micrograph of 1:4 DEMUX.

2. MUX Architecture

The 4:1 MUX architecture is shown in Fig. 10. The clock style in this architecture is the same as that in the DEMUX. Fig. 11 shows a timing chart. This MUX architecture serializes four signals from the DEMUX to one high-speed signal.

Fig. 13 shows a chip micrograph of the 4:1 MUX that is also fabricated by 90-nm CMOS process technology. For the measurement convenience, the DEMUX is integrated with the MUX, as shown in Fig.12, because four parallel input signal preparations are unnecessary. Measurement can be done by inputting a high speed serial data to the DEMUX input terminal.

The area of the MUX circuit including the divider and clock buffer is as small as 30 × 18 μm^2.

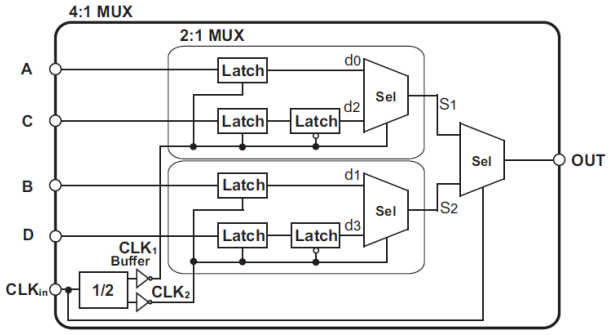

Fig. 10. MUX architecture.

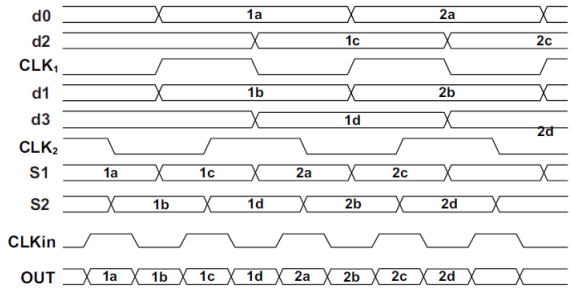

Fig. 11. MUX timing chart.

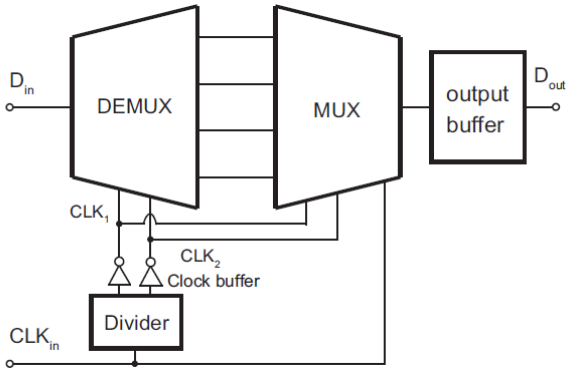

Fig. 12. Measurement circuit architecture of MUX.

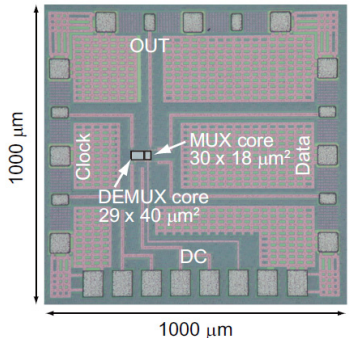

Fig. 13. Chip micrograph of 4:1 MUX (with DEMUX).

IV. Measurement Results

A pulse pattern generator (PPG) was used to generate an input pseudo-random binary sequence (PRBS) data. The output error was measured by using an error detector. The output was considered error-free if the error rate was less than 10^{-10}. The eye diagrams were observed with the help of a sampling oscilloscope.

Measurements were done by using RF probes that contact to the chip directly.

1. 1:4 DEMUX

Fig. 14 shows an output eye diagram of the 1:4 DEMUX for an input of 10 Gb/s $2^{31}-1$ PRBS data. The data rate at the DEMUX output, therefore, was 2.5 Gb/s. Clear eye opening with peak to peak jitter less than 32 ps was obtained. An input phase margin was 874 mUI (peak-to-peak), and the threshold margin was 317 mV (peak-to-peak).

The maximum operation speed was 25 Gb/s when 2^7-1

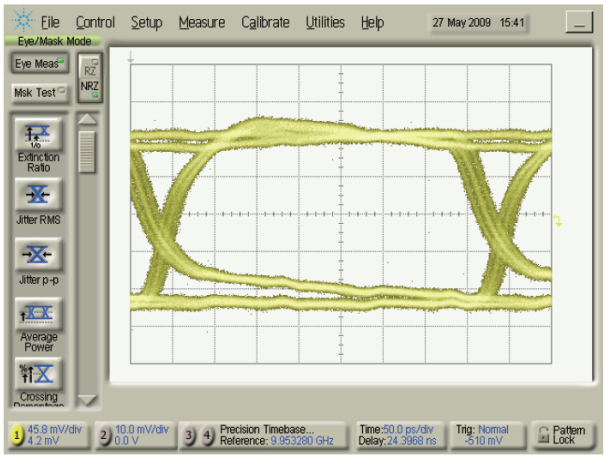

Fig. 14. Measured DEMUX output eye diagram at 2.5 Gb/s (10 Gb/s input).

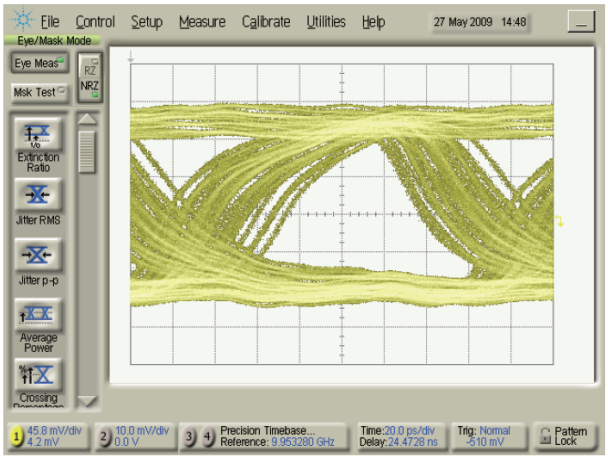

Fig. 15. Measured DEMUX output eye diagram at 6.25 Gb/s output (25 Gb/s input).

PRBS data was input. As shown in Fig. 15, the maximum speed was limited by the data pattern dependent jitter not by the thermal noise base random jitter. The jitter became large as operation speed is increased. We think the frequency dependence of the group delay especially in the output buffer is limiting the maximum operation speed. If more wideband frequency range of the constant group delay is achieved by optimizing the circuit parameters, higher speed operation thought to be observed. The power dissipation in the DEMUX core (DEMUX + divider + clock buffer) was 8.9 mW with 1.05-V power supply. The power dissipation including the output buffer was 20.2 mW. The input phase margin (peak-to-peak) and threshold margin (peak-to-peak) were 345 mUI and 146 mV respectively.

To pursuit low voltage and low power operation, the DEMUX was also evaluated with a lower power supply voltage of 0.9 V. In this case, the maximum data rate was 15 Gb/s. The power dissipation in the DEMUX core was 4.8 mW, and the power dissipation including the output buffer was 13.5 mW. We think this low voltage operation could be obtained by using the proposed pseudo-NMOS logic circuits to the DEMUX.

2. 4:1 MUX

Fig. 16 shows an output eye diagram of the 4:1 MUX for an output of 13-Gb/s $2^7 - 1$ PRBS data. The output jitter of 32 ps (peak to peak) was limiting the maximum operation speed. As same as the DEMUX, we think the maximum speed is limited by the data pattern dependent jitter especially in the output buffer. Therefore, we think there is a possibility that the MUX core could be operated at more than 13 Gb/s, if the output buffer performance is improved. The power supply voltage could be reduced to 1 V. In this case, The speed was 10 Gb/s with 2.3-mW power dissipation.

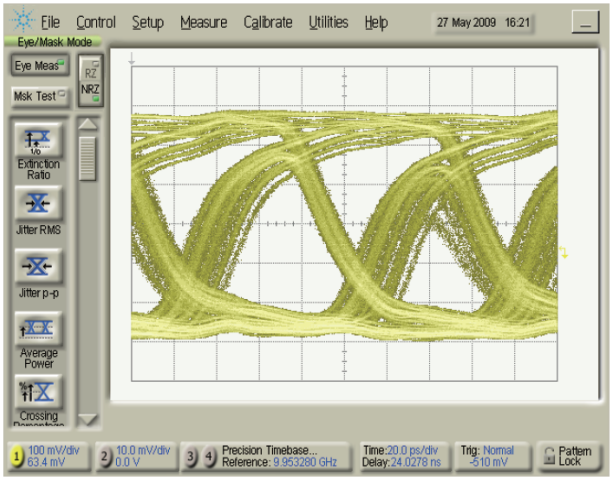

Fig. 16. Measured MUX output eye diagram at 13 Gb/s.

3. Potential of Proposed DEMUX and MUX

Table 1 and 2 shows performance of high-speed CMOS DEMUXes [5, 6, 11-13] and MUXes [6, 14-16]. Since DEMUX outputs are usually fed to other circuit blocks on the same chip, power consumption without the output buffer is assumed to be more important than that with the output buffer. In the present study, the power consumption with the output buffer is quite low. However, the jitter is large in our study. We think this is caused mainly by the output buffer bandwidth. If the output buffer bandwidth can be improved, higher speed performances are thought to be observed in the proposed DEMUX and MUX.

The power efficiency of SerDes circuits operating at different data rates can be compared by using unit of the power per data rate in mW/Gb/s [17]. Figure 17 and 18 show comparisons of the performance of our DEMUX/MUX with that of the DEMUXes/MUXes reported in previous studies. These plots compare mW/Gb/s and area.

It is clear that our DEMUX/MUX are achieving the lowest-power operation with the smallest chip areas.

Table 1. Performance of high-speed CMOS DEMUXes

Reference	[11]	[12]	[13]	[6]	[5]	This work	
DEMUX	1:8	1:4	1:2	1:4	1:4	1:4	
Circuit type	Feedback MOS CML	Coupled latch CML	CML	Current-sourceless CML	Differential Pseudo-NMOS	Differential Pseudo-NMOS	
Load	PMOS triode	R	R	R+L	PMOS triode	PMOS triode	
Input data rate /Gb/s	10	19	40	40	20	25	15
Output jitter* /ps (p-p)	37	63	21	14	20	68	32
Power consumption (with output buffer)	48	(210)	(108)	(62)	9.5	8.9 (20.2)	4.8 (13.5)
Power supply voltage /V	2.0	1.2	1.5	1.2	1.2	1.05	0.9
Core circuit area /μm²	300 × 420	280 × 410	60 × 70	1400 × 1800	40 × 70	29 × 40	
CMOS technology	0.18 μm	0.13 μm	0.12 μm	90 nm	90 nm	90 nm	

*) estimated from each eye pattern data at cross point of rise and fall wave

Table 2. Performance of high-speed CMOS MUXes

Reference	[6]	[14]	[15]	[16]	This work	
MUX	4:1	4:1	2:1	2:1	4:1	
Circuit type	Current-sourceless CML	One-stage CML	Current-sourceless	Transformer-coupled CML	Differential pseudo-NMOS	
Load	R+L	R+L	R+L	R	PMOS triode	
Output data rate /Gb/s	40	10	20	30	13	10
Output jitter* /ps (p-p)	12	8	14	14	34	42
Power consumption (with output buffer)	(132)	75	22	28	4 (19)	2.3 (12)
Power supply voltage /V	1.2	1.5	1.8	1	1.2	1
Core circuit area /μm²	2400 × 1900	930 × 710	700 × 700	630 × 470	30 × 18	
CMOS technology	90 nm	0.13 μm	0.18 μm	0.12 μm	90 nm	

*) estimated from each eye pattern data at cross point of rise and fall wave

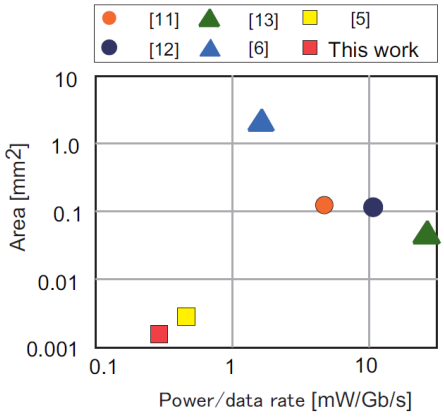

Fig. 17. Comparison of CMOS DEMUXes.

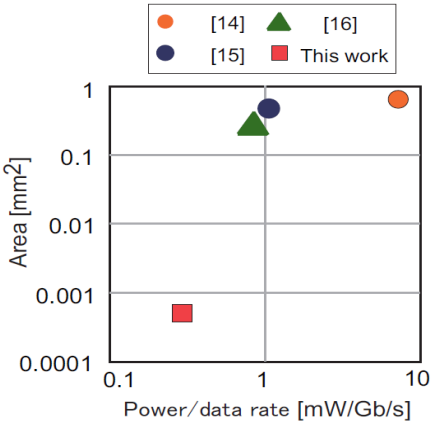

Fig. 18. Comparison of CMOS MUXes.

V. Conclusions

An 8.9 mW 25 Gb/s 1:4 DEMUX and a 4 mW 13 Gb/s 4:1 MUX were implemented in a 90 nm CMOS process. When the power supply voltage was reduced to 0.9 V, operation speed and power dissipation of the DEMUX were 15 Gb/s and 4.8 mW. The DEMUX core circuit area was 29 × 40 μm^2. The MUX core circuit area was 30 × 18 μm^2. By using a differential- pseudo-NMOS logic style and a multi-phase clock architecture, we could realize those high-speed, low-power, small footprint SerDes circuit. Because of these advantages and the near-rail-to-rail logic swing operation, the proposed DEMUX and MUX are suitable for core-to-core interconnection in the system LSI or chip-to-chip communication within a multi-chip module.

Acknowledgments

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