Optically Controlled Silicon MESFET Fabrication and Characterizations for Optical Modulator/Demodulator

S.N. Chattopadhyay, C. B. Overton, S. Vetter, M. Azadeh, B. H. Olson, and N. El Naga

Abstract— **An optically controlled silicon MESFET (OPFET) was fabricated by diffusion process to enhance the quantum efficiency, which is the most important optoelectronic device performance usually affected by ion implantation process due to large number of process induced defects. The desired impurity distribution profile and the junction depth were obtained solely with diffusion, and etching processes monitored by atomic force microscope, spreading resistance profiling and C-V measurements. With this approach fabrication induced defects are reduced, leading to significantly improved performance. The fabricated OPFET devices showed proper I-V characteristics with desired pinch-off voltage and threshold voltage for normally-on devices. The peak photoresponsivity was obtained at 620 nm wavelength and the extracted external quantum efficiency from the photoresponse plot was found to be approximately 87.9%. This result is evidence of enhancement of device quantum efficiency fabricated by the diffusion process. It also supports the fact that the diffusion process is an extremely suitable process for fabrication of high performance optoelectronic devices. The maximum gain of OPFET at optical modulated signal was obtained at the frequency of 1 MHz with rise time and fall time approximately of 480 nS. The extracted transconductance shows the possible potential of device speed performance improvements for shorter gate length. The results support the use of a diffusion process for fabrication of high performance optoelectronic devices.**

Index Terms— **OPFET, MESFET, etching, metallization, diffusion process, quantum efficiency, spectral responsivity, gain-bandwidth, device fabrication, characterization**

I. INTRODUCTION

Optically controlled MESFETs (OPFETs) have drawn considerable attention in recent years due to their potential application as optically controlled microwave devices [1] and optical modulator/demodulators [2]. A number of theoretical and experimental works have been reported on optically controlled MESFETs [3-6]. The potential of MESFETs as high-speed photodetectors was first demonstrated by Baack et al [7]. Various control functions such as amplifier gain, phase shifting, oscillator tuning and injection locking can be achieved by using OPFET devices. Experimental findings show that the microwave characteristics of a GaAs MESFET can be controlled by incident light radiation having photon energy greater than or equal to the bandgap energy of GaAs in the same manner as varying the gate bias [8-12]. In comparison with avalanche photo diodes (APDs), OPFET devices show superior performance for dispersion measurement on optical fibers with low dispersion and very high speed [13]. For frequencies higher than a few GHz, the best photodetector devices are p-i-n or Schottky diodes or ITO photodiodes combined with MESFET devices used as a preamplifier in built-in monolithic optoelectronics integrated circuit (OEIC). The gain and noise performance of single-gate GaAs MESFET's have been extensively characterized and the MESFET potential in low noise amplifiers has been clearly demonstrated [14]. The advantage of MESFET using a preamplifier is low noise performance and extremely low gate-to-source capacitance. This low capacitance allows for high sensitivity. In recent years, there

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has been considerable attention given to the development of silicon based OEICs [15, 16], which is the integration of a photodetector (p-i-n or APD or MSM) with a transistor (MESFET or HBT). The fabricated OPFET device shows similar function of OEICs for photo detection and amplification with reduced signal delay, noise and enhancement of QE and responsivity, etc. Successful implementation of OPFET in MMIC applications, however, largely depends on the noise performance of the device in the illuminated condition. The semi-insulated substrate of GaAs MESFET technology greatly reduces parasitic capacitances and thus, is an excellent choice for low noise and high speed applications [17]. For a given gate length technology, increasing gate width of MESFET device has been found effective at improving the noise figure [18].

To date, desired impurity distribution profiles have been achieved with ion implantation followed by annealing to minimize defects. Experiments measuring the bulk generation lifetime of MOS capacitors have shown residual ion implantation defects in the substrates remain in spite of annealing [19]. Phosphorus ion implantation not only results in the transition of the crystalline fullerenes to an amorphous material phase, but also produces a significant defect level, which is evident from solar cell efficiency ranges of only 10-20% [20]. An effective loss of photo-generated carriers due to the ion implantation process induced defects in the active channel region of OPFET is a major issue of degradation of quantum efficiency and sensitivity [21]. A dc analytical model of an ion implanted GaAs based OPFET has been proposed by many researchers [22-24]. Unfortunately, none of these models incorporate a number of important parameters required to account for physical fabrication problems such as out-diffusion of carriers during annealing and ion implanted process induced defects. These additional parameters are necessary to properly estimate quantum efficiency performance in practical devices. Process induced defects due to diffusion process are obviously far less compared to ion implantation, as has been verified by our previous articles [25, 26]. This work focuses on investigating of the impact of diffusion process induced defects verifying their minimal effect on quantum efficiency. Various parameters were optimized for our fabricated device to maximize speed and reduce power consumption. The gate length of the MESFET was shortened and parasitics reduced to increase f_T, and the load resistance was selected to minimize the output-circuit time constant without reducing the logic swing. This research paper presents the characterization results of our fabricated OPFET in our microelectronics laboratory.

II. THEORY

A schematic diagram of OPFET with MESFET structure is shown in Fig. 1. The transparent gate is made of indium tin oxide (ITO) forming a Schottky rectifying contact with proper antireflection properties. OPFET device structure was optimized by analytical modeling

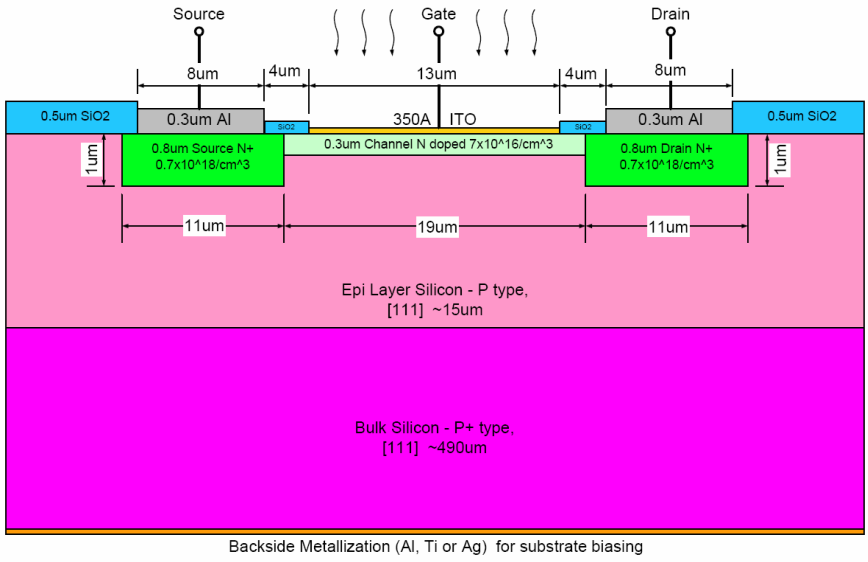

Fig. 1. Device structure of OPFET.

and TCAD simulations for gate lengths varying from 1 μm to 13 μm. Fig. 1 shows a cross-sectional schematic diagram for 13 μm gate length. The theory for OPFET considering non-uniform doping has been described with the physics based analytical modeling [21]. When the device is illuminated by photons with energy $E_{ph} = h\nu$ (h = Planck's constant and ν = frequency of the light) greater than the energy bandgap of silicon (1.12 eV) but smaller than the energy bandgap of indium tin oxide (~3.5 eV), electron and hole pairs are generated.

Depending on device structure and the wavelength of the incident light, several different photo-induced processes may occur. The primary photo effect along the Schottky junction (low injection case of incident photon flux) is photovoltaic. In this case, the photo-generated electron-hole pairs are separated by the Schottky junction built-in electric field and move in different directions due to the space charge effect [27]. The electrons move towards the channel and holes toward the surface. The holes recombine with traps or recombination centers, giving rise to a gate leakage current [13, 24]. Thus a photovoltage is developed across the junction, effectively reducing the depletion width in the channel. This reduction of the gate depletion region causes an increase in drain current for a given source-drain bias. Thus a photovoltage is developed across the junction, effectively reducing the depletion width in the channel. This reduction of the gate depletion causes an increase in drain current. Thus variation of depletion width directly affects the drain current. This optical modulation of drain current gives higher optical responsivity in a FET compared to a simple Schottky diode, which normally achieves an optical responsivity of less than unity. Additional lesser photo-induced effects may be present as well. For large gate resistances a noticeable photovoltage is generated, supplementing the dark gate-source bias voltage. A similar photovoltaic effect can also occur at the channel substrate junction which can act as a photodiode but this effect can usually be ignored by assuming low injection conditions.

Moreover, the photo-generated carriers in the depletion layer from the gate to the drain are swept out by the electric field and contribute to the primary photocurrent between the drain and gate. This gate current causes a change in the gate voltage due to the potential drop on the gate resistance, which in turn causes a change in the drain current via the transconductance of MESFET [28].

Optical radiation is absorbed by the gate depletion region through the transparent ITO gate. As a result, electron-hole pairs (EHPs) are generated and carrier transport occurs due to drift and surface recombination. Due to gate-biasing, the generated electrons move towards the n-channel, whereas the holes move towards the surface to recombine the surface traps. Carrier transport is considered to be due to diffusion, and both bulk and surface recombination, therefore reasonable channel thickness is optimized to absorb maximum optical radiation as well as to prevent the loss of photo-generated carriers. Space charge in the gate and substrate depletion region changes due to the excess generated carriers, which in turn controls the channel opening leading to incremental changes in current. Changes in the space charge region modulate the barrier potential in the junction and as a result, photovoltage will be generated affecting the electrical parameters in the dark to illumination transitions.

III. DEVICE FABRICATION

The active area was formed by diffusion process, which is preferred over ion implantation due to diffusion having little or no process induced defects [21]. Ion implantation induced defects in silicon substrates have been characterized to study the dependence of substrate dopant species (phosphorous and boron) on defect formations [29]. I-V characteristics of ion implanted solar cell devices at optical illumination have shown efficiencies as low as 0.01%. Phosphorous ion implantation not only results in the transition of the crystalline fullerenes to amorphous material phase, but also produces a significant defect level [30]. An effective loss of photo-generated carriers due to ion implantation process induced defects in the active channel region of OPFET is a major issue of degradation of quantum efficiency, sensitivity, etc.

OPFET fabrication was performed using silicon wafers with <100> orientation with a 10-12 μm thick p-epitaxy with a resistivity of 10 Ohm-cm and p+ substrate with thickness of about 490 to 500 μm and resistivity of 0.02 Ohm-cm boron doped. The wafer was cleaned by SC-1 and SC-2 processes followed by phosphorus impurity doping by diffusion process using Saint Gobain (Carborundum) planar diffusion sources (PDS) PH 900

to form the active channel. The resultant diffusion process shows an impurity distribution with the surface impurity concentration of approximately $3x10^{18}$ cm^{-3} and junction depth of approximately 0.375 µm measured by Solecon Laboratories shown in Fig. 2.

The high surface impurity concentration and large junction depth resulting from this type of doping process are not reasonable for optoelectronic device for high QE and speed performance. Hence, the doped silicon wafers were further etched by 45% KOH at 50 ^oC for 3.5 minutes at N_2 ambient based on the optimization of etching time and temperature calculated using the KOH etching model [31], thus a shallower junction with lower surface doping concentration was achieved compared to the conventional diffusion process using PH900.

KOH etching process was preferred for anisotropic etching and uniform bright surface [32]. One of the crucial issues during etching process is its effect on the surface roughness of the resulting silicon film surface. The roughness of silicon <100> surfaces caused by etching can affect their nanotribological (friction and wear) behavior [33, 34] as well as mechanical properties of the microscale structures [35-37]. Experimental studies on the measurement of the roughness of the etched surfaces [38, 39] have shown that the roughness of the etched surface depends upon the temperature and concentration of KOH etchant [40-42]. Higher micro-roughness will result in voids that can not be cured during annealing processes [43] and cause higher stress in the bonding interface [44]. Once the surface micro-roughness exceeds a critical value, the wafer will no longer be bondable. However, anisotropic etchant solutions such as KOH or NaOH generally form random distributed pyramids as a micro-roughness, which can improve light trapping properties [45, 46]. These pyramidal textures have geometries, which allow as much light as possible to be absorbed and converted to electrical current in the solar cell or optoelectronic devices. Fig. 3 shows KOH etching analysis of a doped sample inspected by Atomic Force Microscopic (AFM). Considering above effects, some test wafers were etched and finally the etch process was optimized to an etching solution of 45% KOH at 50 ^oC for 3.5 minutes at N_2 ambient. This technique has been applied to OPFET forming a channel with appropriate impurity distribution and junction depth. The etched and non-etched areas can be clearly seen in Fig. 3. Fig. 4 shows the impurity distribution of KOH etched sample extracted from C-V measurement, where the KOH etching brings the surface concentration down from about $2x10^{19}$ cm^{-3} to the range of $6x10^{16}$ - $7x10^{16}$ cm^{-3} and the junction depth in the range of about 0.1 µm.

The source and drain doping was formed by diffusion process using PH900 and the drain/source doping con-

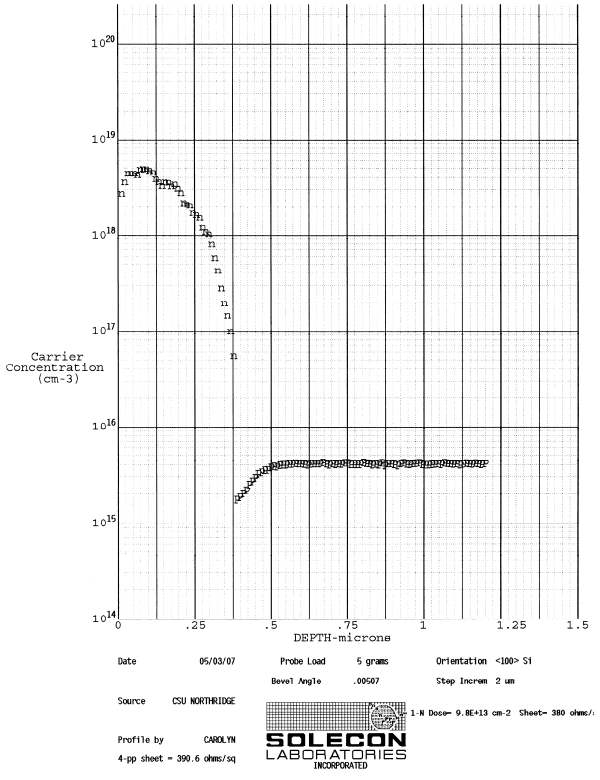

Fig. 2. Doped Phosphorous Impurity distribution measured by Solecon Laboratories.

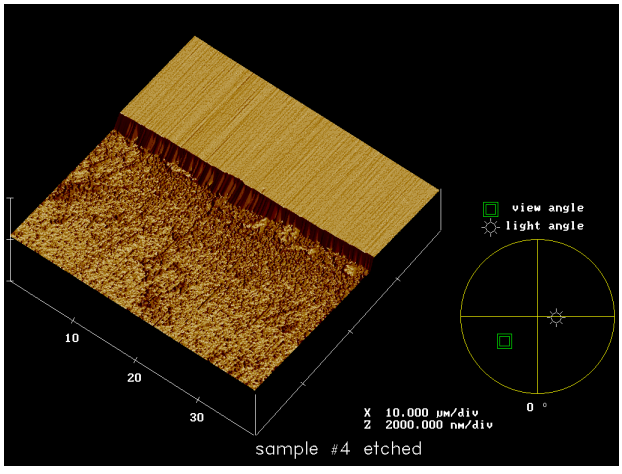

Fig. 3. AFM image of silicon wafer sample etched by KOH at 50 ^oC for 3.5 min in N_2 ambient.

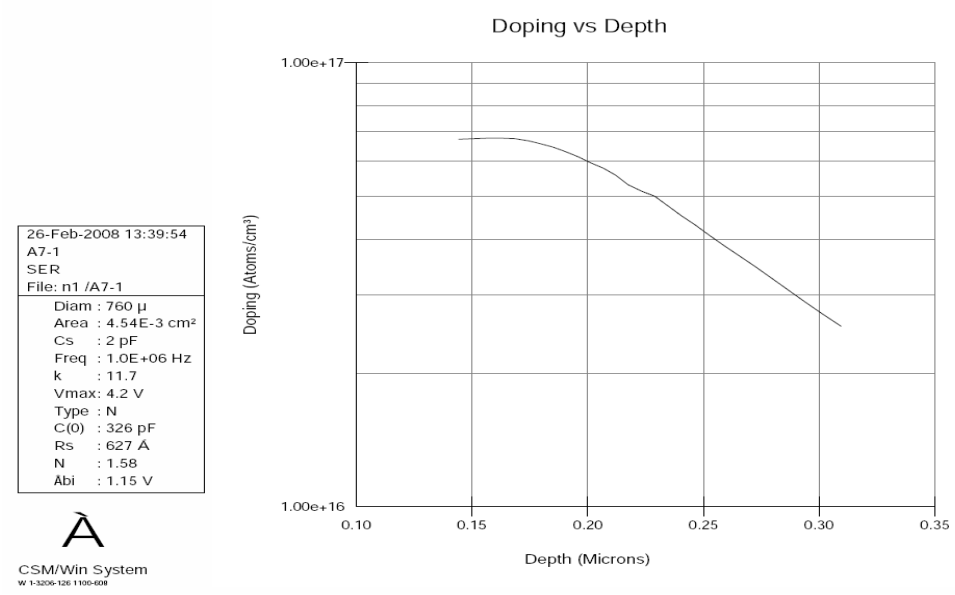

Fig. 4. Impurity distributions from C-V measurement after KOH etching.

centration and junction depth were kept in the range of $5x10^{19}$ - $8x10^{19}$ cm^{-3} and 0.5 to 0.75 μm. Aluminum film deposition for source/drain was performed by a sputtering system with power set to 100 Watt and 10SCCM argon flow resulting in the chamber pressure of approximately $4.3x10^{-3}$ Torr for 30 minutes. The deposited aluminum film thickness measured by Veeco A-Scope was found to be 3000 Å with a thickness tolerance of 5%.

The indium tin oxide (ITO) Schottky gate was formed by using a bi-layer photoresist metal lift-off process. ITO deposition was performed by sputtering with initial vacuum in the range of $5x10^{-8}$ to $7x10^{-8}$ Torr. The ITO film was deposited at power setting of 100 Watt for 4 minutes in argon and oxygen flowing at 12 SCCM and 0.2 SCCM respectively, resulting in a chamber pressure of approximately $8.5x10^{-3}$ Torr. An ITO film thickness of 600 - 700 Å was typically used for defining the gate during OPFET fabrication. The entire process cycle was optimized for process integration and resulted in approximately 90% yield for nine various OPFET devices with gate lengths ranging from 1 μm to 13 μm.

IV. Results and Discussion

The electrical and optical characteristics of the fabricated OPFET were extracted from different experiments to evaluate the device performance, which is described below. The I-V characteristics of the 13 μm OPFET device were obtained by probing the source, drain and gate contact pads with floating ground as measured by a Tektronix 370B curve tracer as shown in Fig. 5(a) and 5(b). As indicated, curves were captured at gate-source voltages (V_{GS}) of 2 V to 12 V in 2 V steps. The obtained plots are shown under dark and illuminated conditions. The OPFETs with 13 μm gate length and gate width of 200 μm had maximum saturation currents of 39 mA and 27 mA for gate-to-source voltages V_{GS} = 12 V and 2 V respectively. Comparison of Fig. 5(a) and 5(b) shows the experimental drain current (y-axis) versus drain-source voltage (x-axis) under dark and illumination conditions, indicating the devices have typical FET characteristics. Due to scaling, where the photo-generated current is very small relative to the bias current, the photocurrent measurement was performed using the two diodes configuration (Schottky/n/p) between the gate and substrate shown in Fig. 6(a) and 6(b). The measured I-V characteristics between the gate and substrate under forward and reverse bias in dark and illumination conditions exhibit the typical photo current similar to that of an ideal photodiode in transition from dark to illumination. The measured reverse saturation current under illumination was approximately 80 - 90 μA due to the photo generated carriers resulting from white light.

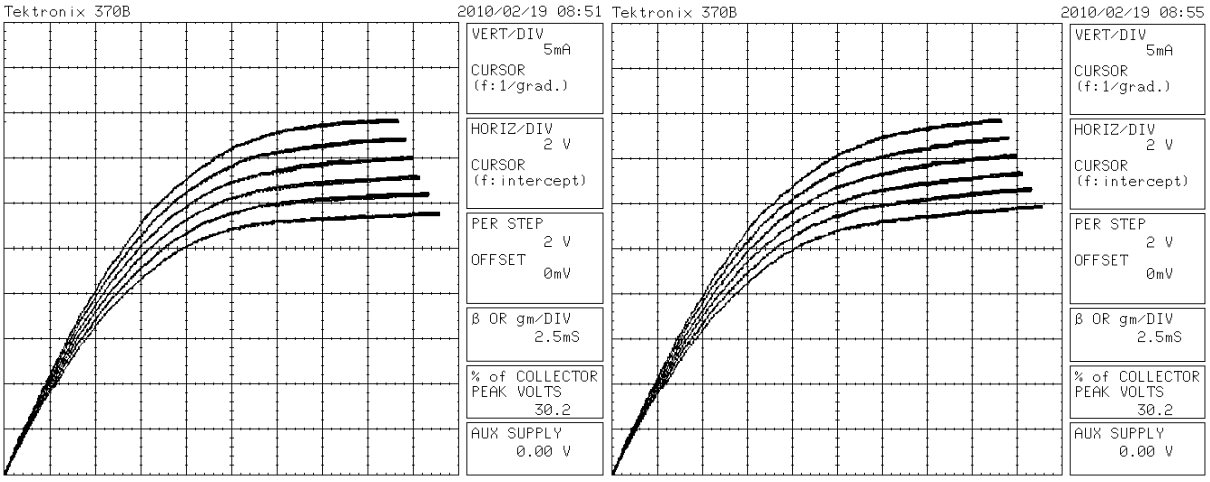

Fig. 5(a) and 5(b). 13 μm OPFET - IV curves taken from first complete OPFET wafer. From Left to right: 13 μm gate OPFET IV curves without illumination, and IV curves with illumination. X axis: Drain to Source Voltage (V_{DS}) and Y axis: Drain Current (I_D).

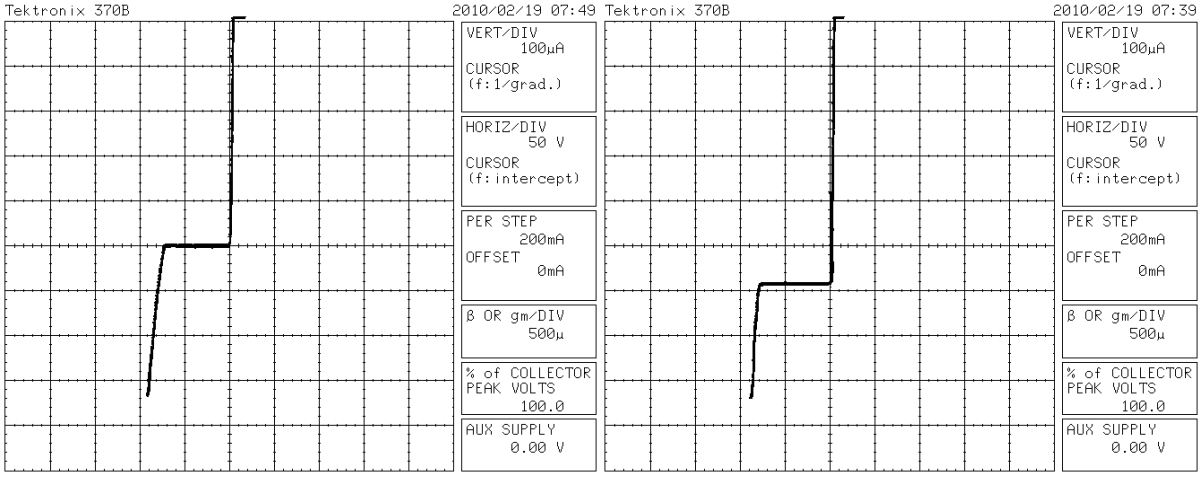

Fig. 6(a) and 6(b). Schottky Photo Diode effect - Schottky diode IV curve is shown using the 13 μm OPFET gate and the substrate. As can be clearly seen, the reverse bias current changes significantly between darkened condition (left) and illuminated (right). X axis: Gate to Substrate Voltage and Y axis: Gate Current.

The pinch-off voltage is found to be approximately 6.06 V extracted from the I-V characteristics. The resulting pinch-off voltage justifies the channel depth as optimized by process simulation and the diffusion process. The active channel depth is an important parameter, which is key in determining the pinch-off voltage of the physical device. The active channel depth and the junction depth of the doped layers are co-related to estimate the pinch-off voltage. Therefore, the pinch-off voltage is not only one of the electrical parameters of the OPFET, but also is key to assist in the optimizing of the fabrication parameters such as the channel depth and junction depth. Diffusion process parameters such as the diffusion time of 20 minutes, diffusion coefficient of approximately $5x10^{-15}$ cm^2/sec for 840 ^oC [47] and measured impurity flux of $5.5x10^{13}$ cm^{-2} from the spreading resistance profiling (SRP) for impurity distribution profile were taken into consideration to calculate the pinch-off voltage from our previous paper [21].

Fig. 7 shows the plot of OPFET device's responsivity, factoring out the Air-ITO boundary reflectance and ITO absorption (approximately only 14% combined loss at 620 nm due to ITO thickness of only 60 to 70 nm and index of refraction of 1.95), where the peak responsivity was found at 620 nm and the spectral response was observed in the range of 500 – 910 nm. The spectral response was measured under reverse bias of 10 V with optical flux from 350 nm to 1100 nm. The resulting spectral responsivity profile is somewhat typical for silicon material, given the small effect of ITO spectral absorp-

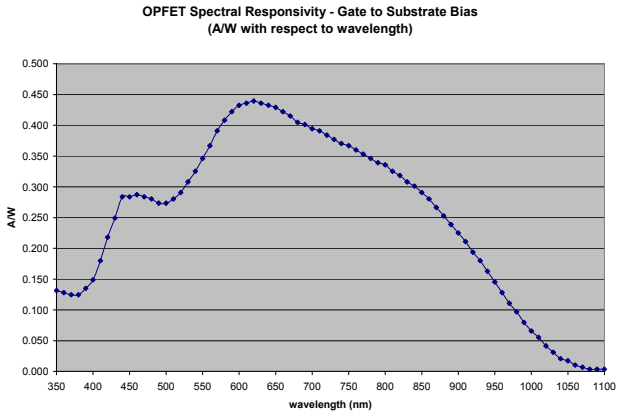

Fig. 7. OPFET optical response (measured by the reverse biased current/watt) versus optical wavelength.

tion and effect of the doping on absorption profile. The optical transmissivity of doped silicon is a function of the sheet resistance and incident wavelengths [48]. Hence, the peak responsivity of the OPFET device can be controlled by adjustment of doping in the absorption layer.

Using this data, quantum efficiency at peak responsivity can be calculated using following equation:

$$QE_\lambda = \frac{R_\lambda}{\lambda} \times \frac{hc}{e} \approx \frac{R_\lambda}{\lambda} \times (1240 W \cdot nm / A)$$

where, $\frac{R_\lambda}{\lambda} = \frac{0.439 W/A}{620 nm}$ which yields a quantum efficiency of about 0.879 or 87.9%.

The spectral responsivity results show that the OPFET has an external quantum efficiency (excluding the Air-ITO boundary reflectance and ITO absorption) of approximately 87.9%, which is much higher than other optoelectronic devices. Factoring in the losses at the Air-ITO boundary and ITO absorption, total external quantum efficiency is calculated as being about 75.6%. This result indicates an improvement due to fewer process induced defects in the active channel region of OPFET compared to optoelectronic devices fabricated by other more complex and expensive doping process technologies, such as ion implantation.

Fig. 8 shows the experimental set-up to measure the modulated output voltage of the device with 13 μm gate versus frequency. Fig. 9(a) shows the OPFET device was packaged in a TO-5 header with Fig. 9(b) showing a close-up of the 13 μm device. Connections were made by gold wire bonding using cold welding process at OSI Ins., USA. EPO-TEK-H20E silver epoxy was used to bond to the gate pad, due to the inability of gold wire to adhere to the ITO coated gate pads. The transistor was mounted in a TO-5 to SMA test fixture specially designed for high frequency compatibility and high precision cables were used to minimize any high frequency effects due to interconnects.

The drain/source and gate terminals of the OPFET device were biased through DC power supplies. The modulated laser signal impinged on the gate and resulted in common source output signal modulation. Fig. 10 shows the output voltage with the drain-to-load resistor of 1.5 kΩ as measured by a 500 MHz (5 GS/s) bandwidth oscilloscope, with a modulated light signal swept from 100 kHz to 2.5 MHz, produced by the direct modulation of a 650 nm, 5 mW laser diode illuminating the ITO transparent gate.

The OPFET device was biased with V_{DS} = 24 V and V_{GS}= -1.35 V. The measured voltage gain was A_V = 2.2 as obtained in the dark condition. The laser was biased at

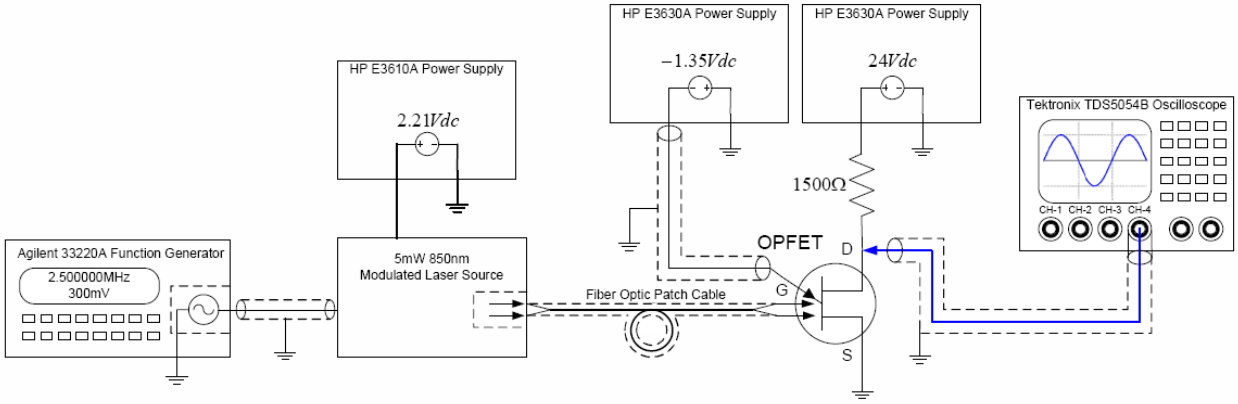

Fig. 8. Experimental setup for optical characterization of the OPFET.

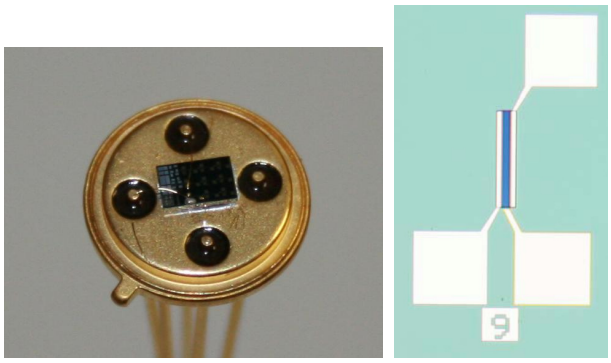

Fig. 9(a) and 9(b). OPFET die in TO-5 package, and close up of 13 µm device.

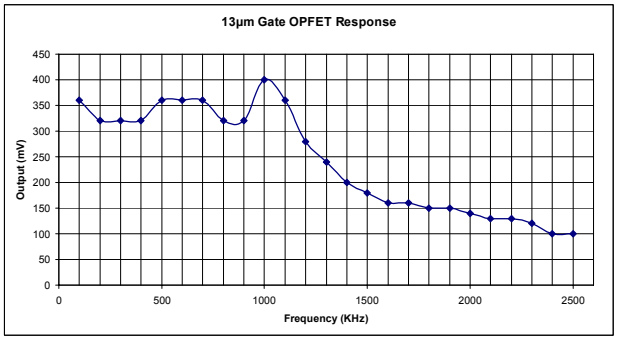

Fig. 10. OPFET output voltage versus modulated signal frequency with a laser biasing of 20 mA and 2.21 V, laser signal amplitude 300 mV, V_{DD} = 24 V DC, V_{GS} = -1.35 V, A_V = 2.2 (electrical gain at 1 MHz at dark condition).

2.21 V with a bias current of 20 mA. The amplitude of the signal generator output was 300 mV for the various frequencies modulating the laser illumination. The voltage gain of the device under illumination is found to be 1.33 at approximately 1.0 MHz and starts falling above 1.1 MHz. The voltage gain and current gain variations in the dark and illumination conditions shows a practical evidence of the OPFET as an optical modulator. The 3 dB bandwidth of the OPFET device was determined to be approximately 1.5 MHz, which is limited by the cut-off frequency of the 13 µm Si MESFET, which should be in the GHz range for similar sub-micron devices.

Fig. 11 shows a plot of drain-source current versus gate-source voltage for 1 µm and 13 µm gate length OPFET devices estimated from the I-V characteristics measured from the Tektronix 370B curve tracer. The intersecting point of the plot at V_{GS} axis with I_{DS} = 0 in Fig. 11 indicates the threshold voltages of -4.0 volts for 13 µm and -2.0 volts for 1 µm gate length under gate illumination condition. The maximum drain current for 13 µm gate OPFET device becomes almost twice as small

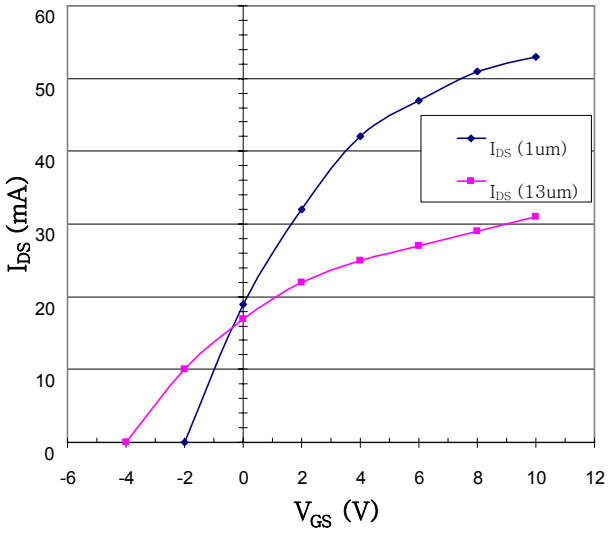

Fig. 11. Drain-source current versus gate-source voltage for 1 µm and 13 µm gate length.

i.e. approximately 32 mA compared to that of 1 µm gate OPFET i.e. approximately 54 mA due to the gate length reduction. As a result, the transconductance is higher and the gate capacitance should be lower, compared to those of the 13 µm gate OPFET. Therefore, higher gate length and gate-source capacitance will limit the device response to a range in the lower MHz scale because of the influence of gate capacitance and long transit time on the frequency response.

V. Conclusions

In contrast to optoelectronic devices fabrication by ion implantation and their inherent device performance issues, OPFET fabrication was pursued using diffusion process. Due to low process induced defects and low gate-to-source (Schottky gate) capacitance, high quantum efficiency has been achieved by obtaining high photocurrent with excellent responsivity at wavelengths ranging from 550 nm to 850 nm. The enhancement of quantum efficiency (87.9%) allows for the sensitive control of the channel opening by significant photovoltaic effect in the gate. The peak responsivity and maximum output voltage of the 13 µm gate OPFET were found to be at 620 nm and 1.0 MHz respectively. Modeling and simulation shows that the responsivity and output voltage can be further enhanced by optimizing the gate length

and channel doping concentration. Comparative study of transconductance of OPFET devices with 1 μm and 13 μm gate lengths shows that the transconductance of 1 μm gate length is much higher compared to that of the 13 μm gate length. Moreover, the gate-source capacitance for the 1 μm gate length is much smaller than that of the 13 μm gate. It can be anticipated that the combination effect of transconductance and gate-source capacitance of the 1 μm gate OPFET would show significantly improved frequency performance useful for high speed switching applications. The scope of research for measuring the responsivity and frequency response characteristics of OPFETs with 1 μm gate length (or smaller) would be extremely valuable to completely understand the full potential of silicon OPFET devices in optical switching, optical routing, optical modulation and high sensitivity photo-detection applications.

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