Investigation of Thermal Noise Factor in Nanoscale MOSFETs

Jongwook Jeon*, Byung-Gook Park, and Hyungcheol Shin****

Abstract— **In this paper, we investigate the channel thermal noise in nanoscale MOSFETs. Simple analytical model of thermal noise factor in nanoscale MOSFETs is presented and it is verified with accurately measured noise data. The noise factor is expressed in terms of the channel conductance and the electric field in the gradual channel region. The proposed noise model can predict the channel thermal noise behavior in all operating bias regions from the long-channel to nanoscale MOSFETs. From the measurement results, we observed that the thermal noise model for the long-channel MOSFETs does not always underestimate the short-channel thermal noise.**

Index Terms—**Channel thermal noise, nanoscale MOSFETs, noise modeling, short channel effects, thermal noise factor**

I. INTRODUCTION

Since low noise design is one of the key issues in the overall analog and RF CMOS circuits, modeling of the noise characteristics of the nanoscale MOSFETs is important [1–3]. The channel thermal noise is the most dominant noise source of the MOSFETs at high-frequency [4–7]. As the gate length scales down to nanoscale era the channel thermal noise becomes larger [4–10].

A. van der Ziel modeled the power spectral density (PSD) of the long-channel thermal noise (S_{id_long}) as given in (1). It is most commonly used channel thermal noise model [11].

$$S_{id\_long} = 4k_B T_o \gamma_{long} G_{DO} \tag{1}$$

where G_{DO} is the channel conductance at $V_{DS} = 0$ V. γ_{long} is the noise factor of the long-channel MOSFET. It is 1 at $V_{DS} = 0$ V and it converges into 2/3 at the saturation bias region. It has been widely known that the long-channel thermal noise model severely underestimates the short-channel thermal noise due to short channel effects such as channel length modulation (CLM), velocity saturation effect (VSE), and carrier heating effect (CHE) [3–10, 12]. As the channel length shrinks down to the nanoscale, these short-channel effects become more prominent in noise behaviors [13]. Especially, the decrease in the linear channel region due to the high-field effect increases the channel thermal noise in the nanoscale device.

The noise factor, γ, is the most common parameter describing the bias dependence of the channel thermal noise. It is also very important parameter used mostly by circuit designers. However, no simple analytical model of γ for short channel MOSFETs has been presented. It will be helpful if such an analytical model is provided to the circuit designers as well as device engineers. In this paper, we propose the noise factor as a compact form which is expressed in terms of the channel conductance and the electric field in the gradual channel region. By using the proposed noise model, the channel thermal noise is investigated in all operating bias regions from long-channel to nanoscale MOSFETs. In section II, we show the derivation procedure of the thermal noise factor as a compact form based on our previous works. In section III, the thermal noise is characterized from long-

Manuscript received May. 24, 2010; revised Sep. 8, 2010
* Semiconductor Research Center, Samsung Electronics, Korea
** ISRC and School of Electrical Engineering, Seoul National University, Korea
E-mail : voix0707@naver.com

channel to nanoscale devices by using the derived thermal noise factor. In addition, the proposed noise is compared and verified with the noise measured data in this section. Finally, conclusions are presented in section IV.

II. Analytical Channel Thermal Noise Modeling

In our previous work, we derived S_{id} equation as an integral form including the short-channel effects; CLM, VSE, and CHE [13, eq. (10)]. It is repeated here for convenience. The noise characterization involves derivation of the local voltage noise source and propagation from local fluctuations to the output port. The local voltage noise source is given by

$$\overline{(\Delta v_n)^2} = 4k_B T_c \cdot \frac{\Delta x}{(-Q_I^{'}) \cdot W \cdot \mu_n^{'}} \cdot B \tag{2}$$

where T_c is carrier temperature and is ac mobility around the bias point. The propagation from local voltage noise source to drain output port can be derived with taking into account velocity saturation effect as

$$\Delta i_{dn} = \frac{1}{L_c + V_{DSat}/E_c} \cdot \frac{W\mu_{eff} Q_I^{'}(x)}{1+E(x)/E_c} \cdot \Delta v_n \tag{3}$$

where Δv_n is the local voltage noise in the channel region and Δi_{dn} is the channel thermal noise current at the drain output port. By using (2) and (3), the total power spectral density (PSD) of the channel thermal noise can be expressed as

$$S_{id} = \frac{-4k_B T_o}{L_c^2 \left(1+V_{DSat}/L_c E_c\right)^2} \int_0^{L_c} W\mu_{eff} Q_I^{'}(x) \times \left(1+E(x)/E_c\right)^2 dx \tag{4}$$

The analytical channel thermal noise from (4) is derived without any approximation.

In this paper, for further simplification, we assume that $E(x) \approx \bar{E}$ $(= V_{DS}/L_c)$ in the gradual channel region, then S_{id} becomes

$$S_{id} = 4k_B T_o \frac{\mu_{eff} |Q_{inv}|}{L_c^2} \tag{5}$$

where L_c is the length of the gradual channel region. By using the short-channel current equation, $\mu_{eff}|Q_{inv}|$ can be expressed as $I_{DS}L_c[(L_c/V_{DS})+(1/E_c)]$, and then (5) is changed into the form of (1) using the noise factor, γ, as

$$S_{id} = 4k_B T_o \gamma G_{DO} \tag{6}$$

$$\gamma = \frac{G_{DS}}{G_{DO}} \left(1 + \frac{\overline{E}}{E_c}\right) \tag{7}$$

where G_{DS} is the intrinsic conductance of the channel and E_c is the critical electric field which is equal to $2v_{sat}/\mu_{eff}$ [14]. (7) is valid at both the linear and the saturation bias regions. Derived noise factor model deviates from the conventional long-channel model due to both the different channel conductance behavior and the enhanced electric field in a short-channel device. Therefore, the noise factor can be predicted if the channel conductance and the average electric field are known. A similar result to (7) was presented in [15, eq. (13)]. However, many previous works including [15] used an incorrect definition of the channel conductance for the short-channel MOSFETs as mentioned in [13].

III. Experimental and Discussion

The test devices were fabricated using 65 nm RF CMOS technology. The unit finger width and the number of fingers are 2.5 μm and 40, respectively. The shortest device has an effective channel length of 36 nm at $V_{GS} = 1$ *V*. Intrinsic and extrinsic voltages have to be distinguished to exclude the effects of extrinsic resistances. To do this, the accurate source/drain resistances were extracted by using the modified channel resistance method [16]. The noise measurement setup and the extraction procedure for the intrinsic S_{id} in [13] were used. The measurement frequency was 10 GHz where the low frequency noises such as flicker and RTS noise are negligible. By using the correlation matrix method [17], we eliminate the noise contribution of the

PAD/inter-connection line through the three step de-embedding technique (pad-open, open, and short dummy patterns) as well as the thermal noise from extrinsic resistances (R_{SD}, R_{poly}, and R_{sub}). The accuracy of the measured noise data was verified using the procedure in [6]. The short-channel thermal noise was compared with the long-channel thermal noise by extracting the thermal noise factor, γ. To make a thorough investigation on the short- channel thermal noise we extracted two parts of γ independently; G_{DS}/G_{DO} and $1+\bar{E}/E_c$. Fig. 1 shows G_{DS}/G_{DO} as a function of the drain bias for different channel lengths. G_{DS} was obtained from DC I-V measurement. G_{DS}/G_{DO} decreases as the drain bias increases in the linear bias region and then it starts to increase in the saturation bias region. Larger increment of G_{DS}/G_{DO} in the saturation bias region is observed in the short-channel devices than in the long-channel devices due to larger channel length modulation effect.

Fig. 2 presents the gate and drain bias dependencies of G_{DS}/G_{DO} for the nanoscale device. In this figure, we observe that in the saturation bias region the slope of G_{DS}/G_{DO} becomes smaller as the gate bias increases. Fig. 3 illustrates $1+\bar{E}/E_c$ as a function of the drain bias for different channel lengths. L_c was obtained by using the result of [18, eq. (8)] and E_c was extracted from the measured effective mobility (μ_{eff}). $1+\bar{E}/E_c$ becomes large as the channel length shrinks down. The gate and drain bias dependencies of $1+\bar{E}/E_c$ for the nanoscale device are depicted at Fig. 4. Fig. 5 compares modeled γ (solid lines) using (6) with measured data (symbols) for different channel lengths in all bias regions. The modeled

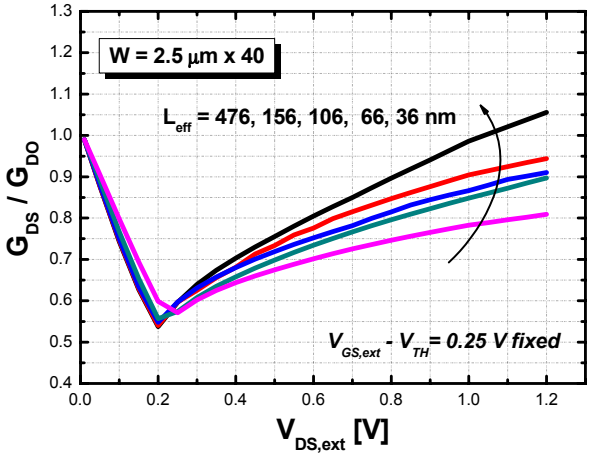


Fig. 1. Extracted G_{DS}/G_{DO} from measurements as a function of the drain bias from long-channel to nanoscale MOSFET.

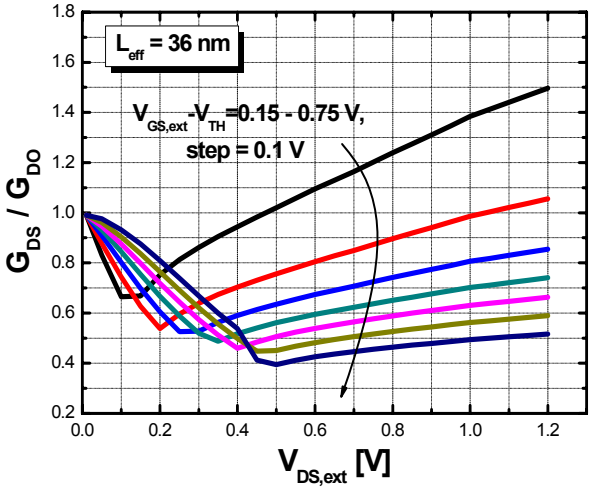


Fig. 2. The gate and drain bias dependencies of G_{DS}/G_{DO} for L_{eff}= 36 nm device.

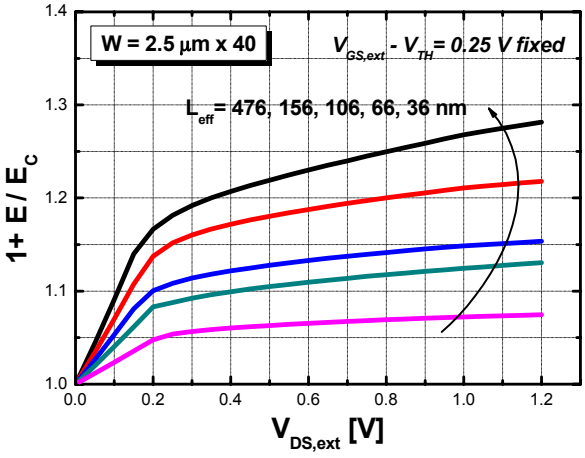


Fig. 3. Extracted $1+\overline{E}/E_c$ from measurements as a function of the drain bias from long-channel to nanoscale MOSFET.

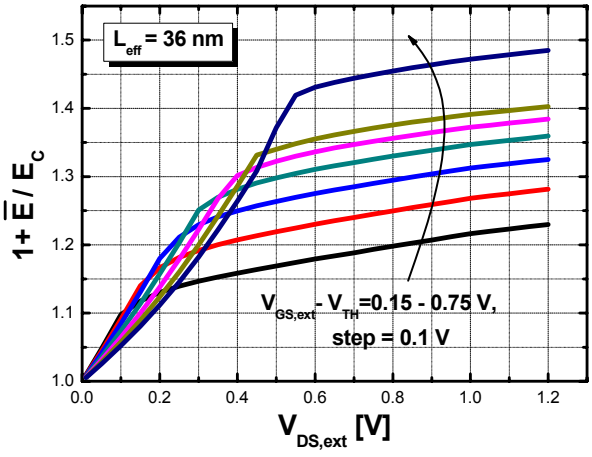


Fig. 4. The gate and drain bias dependencies of $1+\overline{E}/E_c$ for L_{eff}= 36 nm device.

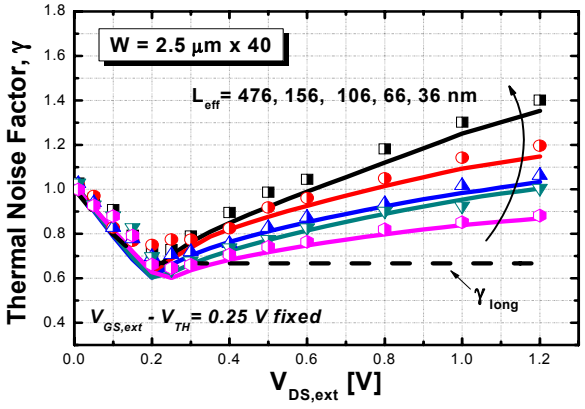


Fig. 5. Thermal noise factor versus the drain bias for different channel lengths; measurements(symbols), γ(solid lines), and γ_{long}(dash line).

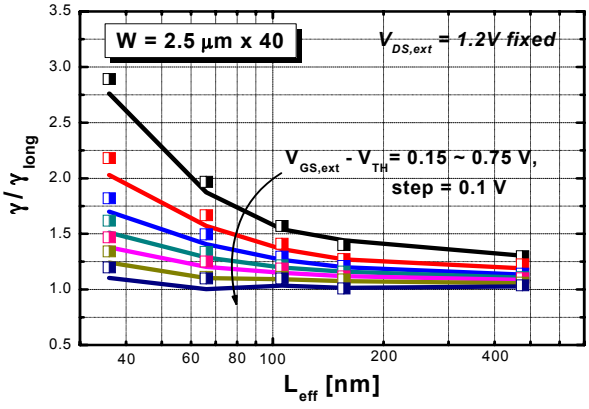


Fig. 7. γ/γ_{long} versus the gate bias for different channel lengths. Lines represent the modeled γ/γ_{long} and symbols are for the measured γ/γ_{long}.

γ_{long} (dash line) using the long-channel model, (1), is presented as well. A good agreement between the modeled γ and the measured data was obtained for both long-channel and short-channel devices. As the drain bias increases in the linear bias region, γ decreases in accordance with the decrement of G_{DS} and in the saturation bias region, γ increases with the increment of G_{DS} due to the short-channel effects such as VSE and CLM. Fig. 6 displays the gate and drain bias dependencies of the thermal noise factor for the nanoscale device. The modeled γ/γ_{long} and the measured data as a function of the gate lengths are given in Fig. 7. γ/γ_{long} increases as the gate voltage decreases. This increment becomes more outstanding at smaller gate overdrive. Fig. 8a and Fig. 8b exhibit γ/γ_{long} for L_{eff} = 36 nm and 476 nm, respectively. For the nanoscale device (Fig. 8a), γ/γ_{long} spreads over a wide range, 0.7 – 2.9. On the contrary, for the long-channel device (Fig. 8b), $\gamma/$

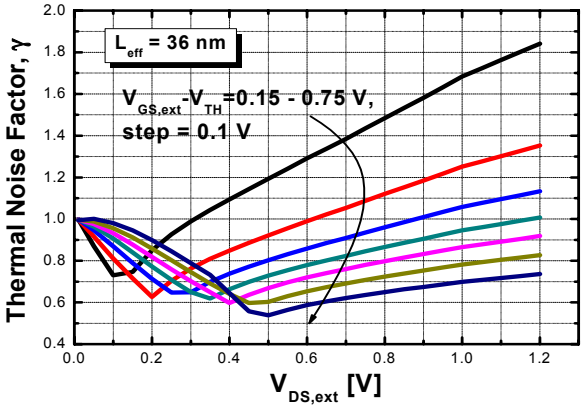
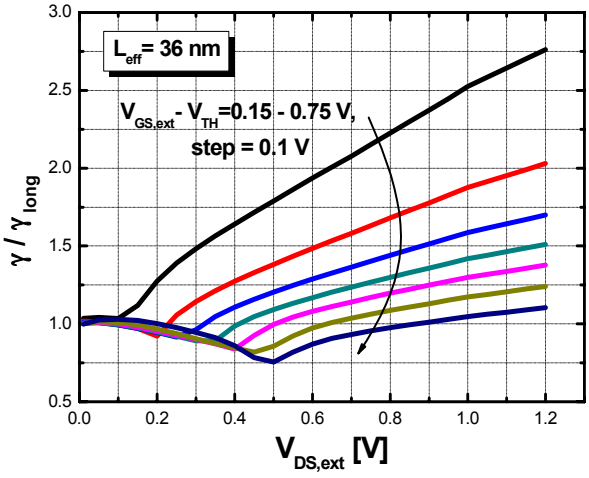
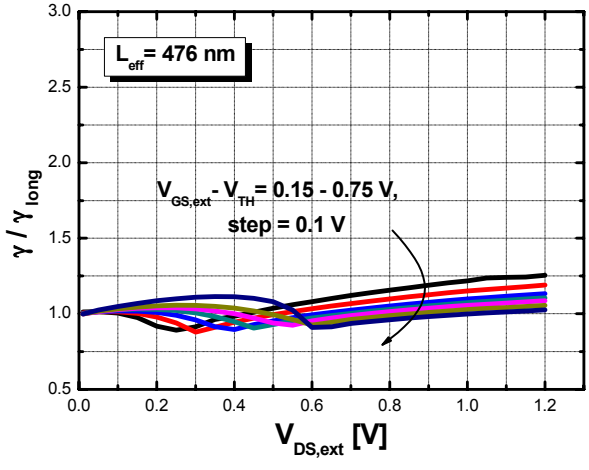


Fig. 6. The gate and drain bias dependencies of the thermal noise factor for L_{eff}= 36 nm device.



(8a)



(8b)

Fig. 8. The gate and drain bias dependencies of the modeled γ/γ_{long} for (8a) L_{eff}= 36 nm and (8b) 476 nm devices, respectively.

γ_{long} has a narrow range, 0.8 – 1.25. In the light of these results, when the model for the long-channel thermal noise is applied to the nanoscale devices, modeling error will be larger. Interestingly, as shown in Fig. 8a and Fig. 8b, the long-channel model does not always undervalue the short-channel thermal noise since γ / γ_{long} are smaller than one in some parts of operating biases. This strange phenomenon comes from the difference between long-channel and short-channel current equations. γ_{long} is calculated by using long-channel current equation according to [19]. However, γ is extracted from (7) by using short-channel current equation which includes mobility degradation and velocity saturation effects. The long-channel current equation commonly used in γ_{long} calculates higher $\mu_{eff}Q_{inv}$ than short-channel current equation in the linear region. Therefore, γ / γ_{long} is less than 1. These phenomena are apparent at high gate voltage as shown in Fig. 8a since the difference of $\mu_{eff}Q_{inv}$ from the long- and short-channel current equations becomes larger at higher gate bias.

IV. CONCLUSIONS

In this paper, the simple analytical model of the channel thermal noise of nanoscale MOSFETs in all operating bias regions is presented. The proposed thermal noise factor model is expressed as a compact form considering short-channel effects. It helps the characterization of the channel thermal noise for both long-channel and short-channel devices. It also allows the circuit designer to predict the short-channel thermal noise from DC measurements without complex noise measurements. It was found that the long-channel thermal noise is not always smaller than the short-channel thermal noise.

ACKNOWLEDGMENTS

This work was supported by Inter-university Semiconductor Research Center (ISRC) and Samsung Electronics Ltd.

REFERENCES

[1] D. K. Shaeffer and T. H. Lee, "A 1.5-V 1.5-GHz CMOS low-noise amplifier," *IEEE J. Solid-State Circuits*, Vol.23, pp.745-759, May 1997.

[2] G. Knoblinger, "RF noise of deep-submicron MOSFETs: extraction and modeling," in *Proc. 28th Eur. Solid-State Device Research Conf. (ESSDERC)*, 1998, pp.460-462.

[3] A. J. Scholten, L. F. Tiemeier, R. Van Langevelde, R. J. Havens, A. T. A Zegers-van Duijnhoven, R. de Kort and D. B. M Klassen, "Compact modeling of noise for RF CMOS circuit design," *IEE Proc.-Circuit Device Syst.*, Vol.151, No.2, pp.167-174, Apr. 2004.

[4] C. H. Chen and M. J. Deen, "Channel Noise Modeling of Deep Submicron MOSFETs," *IEEE Trans. Electron Devices*, Vol.49, No.8, pp.1484-1487, August 2002.

[5] A. J. Scholten, H. J. Tromp, L. F. Tiemeijer, R. van Langevelde, R. J. Havens, P.W. H. de Vreede, R. F. M. Roes, P. H.Woerlee, A. H. Montree, and D. B. M. Klaassen, "Accurate thermal noise model for deep–submicron CMOS," *IEDM Tech. Dig.*, Dec. 1999, pp.155-158.

[6] K. Han, H. Shin, and K. Lee, "Analytical drain thermal noise current model valid for deep submicron MOSFETs," *IEEE Trans. Electron Devices*, Vol.51, No.2, pp.261-269, Feb. 2004.

[7] J. Jeon, I. Song, I. M. Kang, Y. Yun, B.-G. Park, J. D. Lee, and H. Shin, "A new noise parameter model of short-channel MOSFETs," in *Proc. IEEE Radio Frequency Integrated Circuits(RFIC) Symposium*, June 2007, pp.639-642.

[8] A. S. Roy and C. C. Enz, "Compact modeling of Thermal Noise in the MOS Transistor," *IEEE Trans. Electron Devices*, Vol.52, No.4, pp.611-614, Apr. 2005.

[9] C. Enz, "An MOS Transistor Model for RF IC Design Valid in All Regions of Operation," *IEEE Trans. Microwave Theory and Techniques*, Vol.50, No.1, pp.342-359, Jan. 2002.

[10] K. Han, G. Joon, S.-S. Song, J. Han, H. Shin, C.-K. Kim, and K. Lee, "Complete high-frequency thermal noise modeling of short-channel MOSFETs and design of 5.2-GHz low noise amplifier," *IEEE Jour. of Solid-State Circuits*, Vol.40, No.3, pp.726-735, Mar. 2005.

[11] A. van der Ziel, *Noise in Solid State Devices and Circuits,* New York : Wiley, 1986.

[12] W. Jin, P.C.H. Chan, J. Lau, "A physical thermal noise model for SOI MOSFET," *IEEE Trans. Electron Devices*, Vol.47, No.4, pp.768-773, Apr. 2000.

[13] J. Jeon, J. D. Lee, B.-G. Park, and H. Shin, "An analytical channel thermal noise model for deep-submicron MOSFETs with short channel effects," *Solid-State Electronics*, Vol.51, No.7, pp.1034-1038, July 2007.

[14] S. Wolf, *Silicon Processing for the VLSI Era Volume 3 – The Submicron MOSFET*, Lattice Press, 1995.

[15] M. J. Deen, C. H. Chen, S. Asgaran, G. A. Rezvani, J. Tao, and Y. Kiyota, "High -Frequency Noise of Modern MOSFETs : Compact Modeling and Measurement Issues," *IEEE Trans. Electron Devices*, Vol.53, pp.2062-2081, Sep. 2006.

[16] J. Kim, J. Lee, I. Song, Y. Yun, J. D. Lee, B.-G. Park, and H. Shin, "Accurate Extraction of Effective Channel Length and Source/Drain Series Resistance in Ultrashort-Channel MOSFETs by Iteration Method," *IEEE Trans. Electron Devices*, Vol.55, No.10, pp.2779-2784, Dec. 2008.

[17] H. Hillbrand and P. Russer, "An Efficient Method for Computer Aided Noise Analysis of Linear Amplifier Network," *IEEE Trans. Circuit Syst.*, Vol. CAS-23, pp.235-238, Apr. 1976.

[18] S. Asgaran, M. J. Deen, and C. H. Chen, "Analytical Modeling of MOSFETs Channel Noise and Noise Parameters," *IEEE Trans. Electron Devices*, Vol.51, No.12, pp.2109-2114, Dec. 2004.

[19] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*, New York : McGraw-Hill, 1987.

Jongwook Jeon was born in Korea, on 1981. He received the B.S. degree from School of Information and Communication Engineering from Sungkyunkwan University, Suwon, Korea, in 2004, and he was granted Ph.D. degree in Electrical Engineering at the Seoul National University, Korea in 2009. In 2009, he joined Samsung Electronics as a senior engineer. His current research interests are CMOS noise modeling and nano-scale CMOS characterization.

Byung-Gook Park (M'90) received the B.S. and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1982 and 1984, respectively, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, in 1990. From 1990 to 1993, he was with AT&T Bell Laboratories, Murray Hill, NJ, where he contributed to the development of 0.1-㎛ CMOS and its characterization. From 1993 to 1994, he was with Texas Instruments, Dallas, TX, developing 0.25-㎛ CMOS. In 1994, he joined the School of Electrical Engineering, Seoul National University, as an assistant professor. He is currently a full professor. He has been in charge of the research of Inter-university Semiconductor Research Center (ISRC) in Seoul National University since 2003 as the chief of the research department. His current research interests are nanoscale CMOS devices, Si single-electron devices, nonvolatile memory devices, and organic electroluminescent displays. Dr. Park was a member of the International Electron Devices Meeting Subcommittee on Solid State Devices from 2001 to 2002 and worked for Silicon Nanoelectronics Workshop 2005 as a program chair.

Hyungcheol Shin received the B.S. and M. S. degree in electronics engineering from Seoul National University, Seoul, Korea, in 1985 and 1987, respectively, and the Ph. D. degree in electrical engineering from the University of California, Berkeley, in 1993. From 1994 to 1996, he was with Motorola Advanced Custom Technologies, as a Senior Device Engineer. In 1996, he joined the Department of Electrical Engineering and Computer Sciences at the Korea Advanced Institute of Science and Technology (KAIST), Taejon, in 1996 as an Assistant Professor. During his sabbatical leave from 2001 to 2002, he was with Berkana Wireless, CA, as a Staff Scientist in charge of CMOS RF modeling. In 2003, he joined the Department of Electrical Engineering and Computer Science at the Seoul National University, Seoul, as an Associate Professor, where he is a Professor. His current research interests include RF and noise characteristics in nano-scale CMOS devices and circuits. He has published over 300 technical papers in international journals and conference proceedings and also wrote a chapter in a Japanese book on plasma charging damage and a Korean book on semiconductor devices.

He has served as a committee member of several international conferences, including International Electron Devices Meeting. He is a Lifetime Member of IEEK and received the Second Best Paper Award from the American Vacuum Society in 1991. He also received the Excellent Teaching Award from the Department of Electrical Engineering and Computer Sciences at KAIST in 1998 and Seoul National University in 2005. In 1999, he received The Haedong Paper Award from the Institute of Electronics Engineers of Korea (IEEK). He is listed in Who's Who in the World.