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고정 지연 조건에서 전력-지연 효율성의 최적화를 위한 논리 경로 설계

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요 약

Logical Effort의 기법은 회로의 지연 값을 간단한 필산으로 신속하게 측정할 수 있는 기술이다. 이 기법은 설계 공정 시간을 절약하는 장점도 있지만 고정 지연이라는 설계조건에서 회로의 면적이나 전력의 최소화를 도출할 수 있는 논리 경로를 설계하는데 약점도 있다. 이 논문에서는 균형 지연 모형을 제안하고 이 방법을 기반으로 논리경로에서 전력-지연 효율성을 최적화하는 기법을 제안하고자 한다. 본 논문의 기법을 사용하여 8-input AND 게이트의 3가지 서로 다른 설계 회로를 모의 시험한 결과 기존 Logical Effort의 기법보다 약 40%정도 전력 소비의 효율성이 향상되었다.

키워드 : Logical Effort, 균형 지연 모델, 트랜지스터 크기 결정, 전력 소비, 게이트 크기 결정

On a Logical Path Design for Optimizing Power-delay under a Fixed-delay Constraint

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ABSTRACT

Logical Effort is a simple hand-calculated method that measures quick delay estimation. It has the advantage of reducing the design cycle time. However, it has shortcomings in designing a path for minimum area or power under a fixed-delay constraint. In this paper, we propose an equal delay model and, based on this, a method of optimizing power-delay efficiency in a logical path. We simulate three designs of an eight-input AND gate using our technique. Our results show about 40% greater efficiency in power dissipation than those of Logical Effort method.

Keywords : Logical Effort, Equal Delay Model, Transistor Sizing, Power Dissipation, Gate Sizing

1. Introduction

Design constraints of performance and power dissipation determine the appropriate topology for the target digital circuits and transistor size of the critical paths in the circuits. The formula of driving large capacitive loads connected to the inverter chain is derived using the equation of $N \cdot f \cdot \Gamma = \ln(y) \cdot [f \cdot \ln(y)] \cdot \Gamma$ where N is the number of stages, f is the a factor of the size of the second inverter over that of the first inverter, Γ is the inherent inverter delay, Y is C_l/C_g [1]. In Logical Effort [2, 3], based on the concept above, the authors devised a formula having the quick delay estimation and transistor size ratios(P/N transistor) of the circuit paths to be designed. This simple hand-calculated method has the advantage of efficiently reducing the design cycle time.

Because of the simplicity and clarity of Logical Effort model, many studies have improved the accuracy of Logical Effort model to adapt to different design conditions. A simple model for calculating transistor sizes of an asynchronous control circuits with circular paths is shown in [4]. Reference [5] introduces an extension of the Logical Effort model that considers the I/O coupling capacitance and the input ramp effect. The Logical Effort extension model that considers temperature and voltage

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variation is introduced in [6] and its application to FPGA interconnect driver sizing is well discussed in [7].

Logical Effort Model has shortcomings in designing a path for minimum area or power under a fixed-delay constraint [8]. In this paper we propose the equal delay model on the basis of Logical Effort to compensate for the above shortcomings and a new method of optimizing energy-delay efficiency on the basis of this model.

This paper is organized as in the following. In section 2 Logical Effort is reviewed and an equal delay model is proposed. Section 3 describes a relationship between delay and energy consumption using our proposed equal delay model. We also propose a new method to determine the appropriate transistor sizing that leads to the minimum power dissipation in the circuit path under the fixed-delay, based on the equal delay model. In section 4 we compare the simulation results on the basis of our model. Our proposed technique is summarized in Section 5.

2. Equal Delay Model

We introduce a method of Logical Effort and also describe a technique that is used to determine the transistor size using equal delay model, which is developed based on Logical Effort.

2.1 Logical Effort

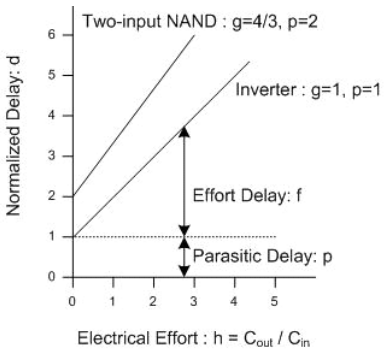
The method of Logical Effort was developed on the ground that circuit delay depends on load and circuit topology. The first step of the Logical Effort model is to describe circuit delay in terms of unit τ, which can exclude the process-dependent effects. More precisely, τ is the delay of an inverter driving an identical inverter with no parasitic. Thus, the absolute delay is expressed as the product of a unitless delay of the gate d and the delay unit that characterizes a given process.

$$d_{abs} = d\tau \tag{1}$$

The delay incurred by a logic gate is comprised of two components: a fixed part called the parasitic delay p and a part that is proportional to the load on the gate's output called the effort delay or stage effort f.

$$d = f + p \tag{2}$$

The effort delay depends on the load and on properties of the logic gate driving the load. The logical effort g captures properties of the logic gate while the electrical effort h characterizes the load. The effort delay of the logic gate is the product of the following two factors.



(Figure 1) Plots of the delay equation for an inverter and a two-input NAND gate

$$f = gh \tag{3}$$

The electrical effort is defined by:

$$h = \frac{C_{out}}{C_{\in}} \tag{4}$$

Where C_{out} is the capacitance that loads the output of the logic gate and C_{in} is the capacitance presented by the input terminal of the logic gate.

Combining (2) and (3), the following equation is derived that models the delay through a single logic gate.

$$d = gh + p \tag{5}$$

(Figure 1) shows this relationship graphically: delay appears as a function of electrical effort for an inverter and for a two-input NAND gate.

An important result of Logical Effort is that it provides a way of determining appropriate transistor size of the critical path to minimize delay.

The principle expressions of Logical Effort are summarized in <Table 1>.

〈Table 1〉 Summary of terms and equations for concepts in the method of Logical Effort

Term	Stage expression	Path Expression
Logical effort	g	$G=\Pi g_i$
Electrical effort	$h = C_{out}/C_{in}$	$H=C_{out-path}/C_{in-path}$
Branching effort	-	$B=\Pi b_i$
Effort	f=gh	$F=GBH=\Pi f_i$
Effort delay	f	$D_F=\sum f_i$ minimized when $f_i=F^{1/N}$
Number of stages	1	N
Parasitic delay	p	$P=\sum p_i$
Delay	d=f+p	$D=D_F+P$

2.2 Transistor Sizing Based On Equal Delay Model

Logical Effort assumes an equal effort delay per stage of the circuit while our equal delay model assumes an equal delay per stage.

(Figure 2) shows the circuit driving a load on the logical path, which is composed of 3 stages. Each gate is characterized by three parameters: delay(d), logical effort(g), and parasitic effort(p). We assume that there is no delay and load between signal lines connecting gates. D is defined as a delay needed for driving load(C_{load}) in the logical path where input capacitance is limited to a certain value.

In this paper we choose the minimum-sized inverter with a P-to-N ratio of 2 as the standard inverter. We also express the delay of each element in terms of τ and capacitance in units of *k*, the input capacitance of a standard inverter as shown in [4].

If the delay per stage in the logical path is the same, each stage's delay is given as $d_1=d_2=d_3=D/3$. Thus, we can establish the following equations on the basis of the overall delay, logical effort, and parasitic effort in the above three-stage logical path.

$$d_1 = \frac{D}{3} = f_1 + p_1 = g_1 h_1 + p_1 \tag{6}$$

$$d_2 = \frac{D}{3} = f_2 + p_2 = g_2 h_2 + p_2 \tag{7}$$

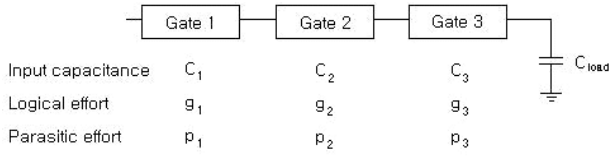
$$d_3 = \frac{D}{3} = f_3 + p_3 = g_3 h_3 + p_3 \tag{8}$$

In the case of no branch, the input capacitance of the next stage is the load of the currently processing stage. So, we can substitute h_1, h_2, and h_3 with C_2/C_1, C_3/C_2, and C_{load}/C_3, respectively. This delivers the following equations.

$$d_1 = \frac{D}{3} = \frac{g_1 * C_2}{C_1} + p_1 \tag{9}$$

$$d_2 = \frac{D}{3} = \frac{g_2 * C_3}{C_2} + p_2 \tag{10}$$

$$d_3 = \frac{D}{3} = \frac{g_3 * C_{load}}{C_3} + p_3 \tag{11}$$



(Figure 2) A three-stage logical path

With the above equations arranged with respect to the input capacitance, respectively, the following equations are derived.

$$C_1 = \frac{g_1 * C_2}{\left(\frac{D}{3} - p_1\right)} = \frac{g_1 * g_2 * g_3 * C_{load}}{\left(\frac{D}{3} - p_1\right)\left(\frac{D}{3} - p_2\right)\left(\frac{D}{3} - p_3\right)} \tag{12}$$

$$C_2 = \frac{g_2 * C_3}{\left(\frac{D}{3} - p_2\right)} = \frac{g_2 * g_3 * C_{load}}{\left(\frac{D}{3} - p_2\right)\left(\frac{D}{3} - p_3\right)} \tag{13}$$

$$C_3 = \frac{g_3 * C_{load}}{\left(\frac{D}{3} - p_3\right)} \tag{14}$$

With expansion of these equations for n-stage circuits, the input capacitance of i-th stage is described as in the following equation.

$$C_i = C_{load} \prod_{k=i}^{n} \frac{g_k}{\left(\frac{D}{n} - p_k\right)} \tag{15}$$

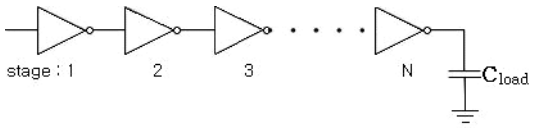
This equation is directly applied to compute input capacitance in a logical path with stage number and C_{load}, and is analogous to the capacitance transformation equation for Logical Effort Model [3], which is used to compute input capacitance backward starting at the end of the logical path.

Here, the value of (D/n) should be larger than the largest parasitic effort value. Because input capacitance of the first stage C_1 is the input capacitance in the logical path, it must satisfy the constraint condition of input capacitance in the logical path.

3. The method of determining gate sizing under the fixed-delay constraint

3.1 Relation between power and delay in the inverter chain

Power dissipation in CMOS circuits consists of dynamic and static dissipation. Static CMOS gates are highly power-efficient because they dissipate to nearly zero power when unused. In this paper, we only consider dynamic power dissipation. Suppose a load C is switched between GND and V_{DD} at an average frequency of f_{SW}, The average dynamic power dissipation is $P_{dynamic}= CV_{DD}^2 f_{SW}$ [9, 10]. The dynamic power dissipation is proportional to the value of C as indicated in the above formula. In other words, the total power dissipation in a path is proportional to the sum of capacitances in the path.



(Figure 3) Inverter Chain

(Figure 3) shows an example of the inverter chain driving the output load(C_{load}). With this structure, we attempt to estimate the gate sizing which drives the fixed load in the mode of optimizing the power dissipation under a constraint delay.

For example, we assume that the inverter chain has the value of 64[k] as output load(C_{load}) and the value of 15[τ] as required delay of the circuit. The above inverter chain consists of the same type of gate and has no branch with it. Therefore, under the equal delay model, input capacitance in the i-th stage can be expressed as in the following formula derived from (15).

$$C_i = \frac{g_i^{(n+1-i)} * C_{load}}{\left(\frac{D}{n} - p_i\right)^{n+1-i}} \tag{16}$$

Here, logical effort and parasitic effort of an inverter is, respectively, equal to 1. Therefore, the above equation can be reduced in the following formula.

$$C_i = \frac{C_{load}}{\left(\frac{D}{n} - 1\right)^{n+1-i}} \tag{17}$$

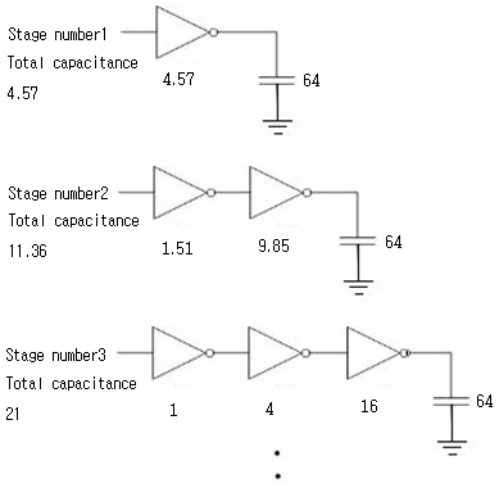
In the worst case, the total power dissipation in the path is proportional to the sum of input capacitances in each stage. The sum is referred to as the total capacitance(ΣC_i) in the path. Power consumption in the inverter chain becomes more efficient as the value of total capacitance(ΣC_i) becomes smaller.

<Table 2> shows the variations of input capacitance(C_{in}) and total capacitance(ΣC_i) as stage number(n) increases in inverter chain, which drive output load(C_{load}) under the constraint delay(D). Here, we assume that the value of output load is 64[k] and the value of constraint delay is 15[τ]. The C_{in} and ΣC_i of <Table 2> are calculated according to (17), respectively.

At first, we can see that total capacitance(ΣC_i) increases significantly as stage number(n) increase as in <Table 2>. Thus, if there are no constraints of input capacitance(C_{in}), the efficiency of power dissipation in a logical path is inversely proportional to the number of stage. However, we have to consider the constraint condition. So, according to the constraint of input capacitance, we will decide the number of stage for optimizing power dissipation. For instance, under the constraint of input capacitance(C_{in})<5[k], as indicated in <Table 2>, power dissipation is the most efficient at stage number(n)=1 where the total capacitance is the smallest. However, under the constraint of input capacitance(C_{in}) <4[k], the value of C_{in} at stage number(n)=1 exceeds the upper bound of the constraint. Therefore, in this case, it is the most efficient at stage number (n)=2.

〈Table 2〉 Cin and ΣCi in each stage number of the inverter chain
(*unit [k] is the input capacitance of a standard inverter [4])

Stage number(n)	Input capacitance(C_{in}) [k]	Total capacitance(ΣC_i) [k]
1	4.57	4.57
2	1.51	11.36
3	1.00	21.00
4	1.12	35.93
5	2.00	62.00
6	5.62	116.76
7	25.13	272.08



(Figure 4) Inverter sizes according to 〈Table 2〉

With an inverter chain driving a load of 64[k], (Figure 4) shows the inverter sizes according to <Table 2> for stage number 1, 2, and 3, respectively.

3.2 Determination of transistor sizing and stage number for optimal power dissipation

Taking into consideration the example of inverter chain, we will show how to determine the appropriate transistor sizing for optimal power dissipation under the constraints of delay and input capacitance in a logical path.

The detailed procedures are shown below.

1. We determine the upper bound of stage number(n)

so that D/n is greater than the parasitic delay value of any logic gates in the logical path.

2. Under the constraint of required delay, the input capacitance(C_1) of the first gate in the various types of topologies for the given logic function is obtained, as stage number(n) increases, using equation (15).
3. Among the topologies which have the input capacitance(C_1: determined at the above procedure) meeting the input constraint(design specs), we look for the minimum stage number(n).
4. Equation (15) is applied to the topology with the minimum number of n and thus to determine the transistor sizing of each gate in the logical path.

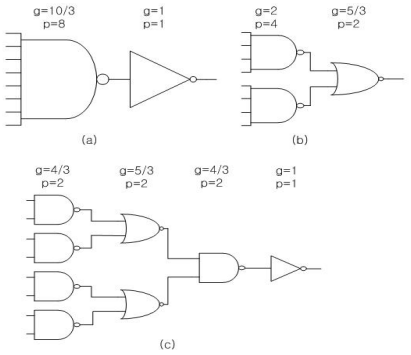
4. Example of an 8-input AND Gate for Our Model

(Figure 5) shows an eight-input AND gate in three different topologies. Under the constraints of Max delay=20[τ], C_{load}=48[k], Max C_{in}=4[k], we will determine topology and gate size for the minimum energy consumption.

<Table 3> shows transistor sizes of i-th stage(C_1, C_2, C_3, C_4) in each AND gate topology((a), (b), (c)) using equation (15). We can observe that topology (a) exceeds the requirement value of Max C_{in} and topology(c) is larger than topology (b) in terms of total capacitance(ΣC_i). Therefore, topology (b) is the best one and the value of C_{in} is 3.33[k]. Topology (LE) indicates the result (of the transistor sizing for the minimum delay) obtained by applying the method of Logical Effort to topology (c), in case of C_{in}=4[k] and C_{load}=48[k].

<Table 4> shows the simulation results for power dissipation and delay in the process of 1.8[v] and 0.18[μm]. Note that topology (a), (b), (c), (LE) use C_i value computed in each topology of <Table 3>. In the result of the Hspice simulation, we note that topology (b) delivers the most efficient power dissipation. In comparison with topology (LE) showing the shortest delay, topology (b) shows about 40% efficiency in power dissipation but is slower approximately by 7%.

<Table 5> shows transistor sizes of each topology based on equation (15) under the constraints of Max delay=20[τ], C_{load}=96[k], and Max C_{in}=4[k]. With this new constraints of the above, topology (c) shows the best result in terms of total capacitances. <Table 6> shows the simulation results for power dissipation and delay using



(Figure 5) The AND function of eight-input : (a) 8-NAND (b) 4-NAND, 2-NOR (c) 2-NAND, 2-NOR, 2-NAND, INVERTER

〈Table 4〉 Simulation result using 〈Table 3〉

Topology	Power dissipation[μ watts]	Delay[τ]
(a)	41.96	22.17
(b)	32.46	16.53
(c)	36.97	17.72
(LE)	54.93	15.35

〈Table 3〉 The capacitance of 8-input AND gate in each topology

(the constraints of Max delay=20[τ], C_{load}=48[k], Max C_{in}=4[k])

Topology	Input capacitanceof stage1(C_1)[k]	Input capacitanceof stage2(C_2) [k]	Input capacitanceof stage3(C_3) [k]	Input capacitance of stage4(C_4) [k]	Total capacitance(ΣC_i) [k]
(a)	8.89	5.33	NA	NA	14.22
(b)	3.33	10.00	NA	NA	13.33
(c)	1.32	2.96	5.33	12.00	21.61
(LE)	4.00	7.33	10.73	19.66	41.72

〈Table 5〉 The capacitance of 8-input AND gate in each topology

(the constraints of Max delay=20[τ], C_{load}=96[k], Max C_{in}=4[k])

Topology	Input capacitanceof stage1(C_1) [k]	Input capacitanceof stage2(C_2) [k]	Input capacitanceof stage3(C_3) [k]	Input capacitance of stage4(C_4) [k]	Total capacitance(ΣC_i) [k]
(a)	17.78	10.67	NA	NA	28.45
(b)	6.67	20.00	NA	NA	26.67
(c)	2.63	5.93	10.67	24.00	43.23
(LE)	4.00	8.71	15.18	33.06	60.95

〈Table 6〉 Simulation result using 〈Table 5〉

Topology	Power dissipation [μ watts]	Delay[τ]
(a)	83.94	22.17
(b)	64.93	16.52
(c)	73.97	17.72
(LE)	89.49	16.78

the transistor sizes of each topology in <Table 5>. In comparison with topology (LE) showing the shortest delay, topology (c) shows about 18% efficiency in power dissipation but is slower approximately by 5%.

5. Conclusions

We introduced an enhanced equal delay model and showed how to determine appropriate transistor sizing using our proposed delay model. For instance, for topology used in Logical Effort, we attempted to figure out the transistor sizing which leads to optimizing power dissipation under the given constraint. On the basis of this value, we compared the simulation results using Hspice with those in Logical Effort.

Our technique makes up for the shortcomings of the existing Logical Effort that cannot easily show how to design a path for minimum area or power. Our proposed technique, however, shows a difference between real delay and model delay in case of a big parasitic effort value.

This method can be expanded to multiple paths of a fanout, on the condition of knowing the sum of capacitances in the branch. However, the capacitance value of each branch should be given in the design specifications. Therefore, further research must be carried out to determine the appropriate input capacitance of the individual branch of a fanout to optimize the energy-delay efficiency on the multiple paths.

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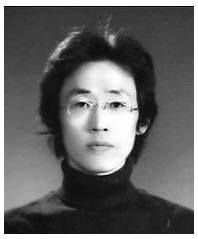

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