Design of an EEPROM for a MCU with the Wide Voltage Range

Du-Hwi Kim, Ji-Hye Jang, Liyan Jin, Pan-Bong Ha, and Young-Hee Kim

***Abstract*—In this paper, we design a 256 kbits EEPROM for a MCU (Microcontroller unit) with the wide voltage range of 1.8 V to 5.5 V. The memory space of the EEPROM is separated into a program and data region. An option memory region is added for storing user IDs, serial numbers and so forth. By making HPWs (High-voltage P-wells) of EEPROM cell arrays with the same bias voltages in accordance with the operation modes shared in a double word unit, we can reduce the HPW-to-HPW space by a half and hence the area of the EEPROM cell arrays by 9.1 percent. Also, we propose a page buffer circuit reducing a test time, and a write-verify-read mode securing a reliability of the EEPROM. Furthermore, we propose a DC-DC converter that can be applied to a MCU with the wide voltage range. Finally, we come up with a method of obtaining the oscillation period of a charge pump. The layout size of the designed 256 kbits EEPROM IP with MagnaChip's 0.18 μm EEPROM process is 1581.55 μm × 792.00 μm.**

***Index Terms*—Wide voltage range, MCU, DC-DC converter, reliability**

I. INTRODUCTION

As a market for MCU (Microcontroller unit) applied products such as mobile devices, household appliances, and so on grows continuously, the need of embedded non-volatile memories for storing updated real-time information, security data, instruction codes, etc. is also stressed recently. As shown in Fig. 1, we have used a mask ROM as an embedded non-volatile memory of instruction codes and a separate EEPROM as a user-supplied data memory at the early stage. Currently, the conventional mask ROM is replaced with a OTP (One-time programmable) memory which can be programmed by users and the separate EEPROM is implemented with an embedded memory to reduce the cost [1]. For applied products requiring non-volatile memory capacity of 1 Mbits or below, EEPROMs are widely used [2, 3]. Recently, the memory space of the EEPROM used in a MCU is separated into a program and data region. An option memory region is added for storing user IDs, serial numbers and so on for the convenience of users. MCUs used for mobile devices require a voltage supply of 1.8 V and those of household appliances a range of 2.7 V to 5.5 V. Thus, a design of EEPROM with the wide voltage range of 1.8 V to 5.5 V is needed to meet these requirements.

Studies on the EEPROM design have been focused on techniques such as small area, low power, and high speed.

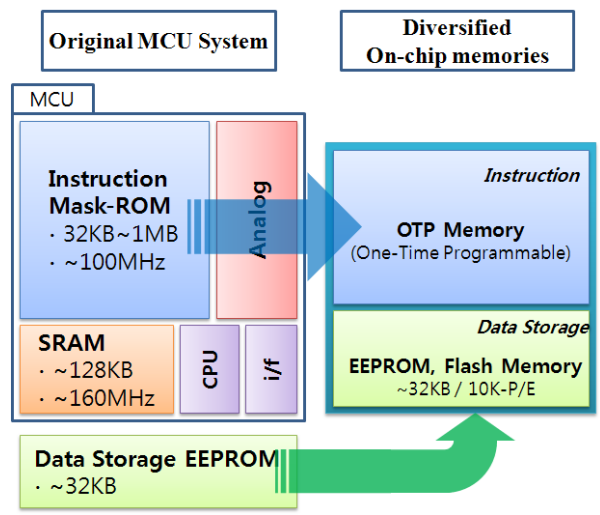

Fig. 1. Trend of non-volatile memories used for MCU applications [1].

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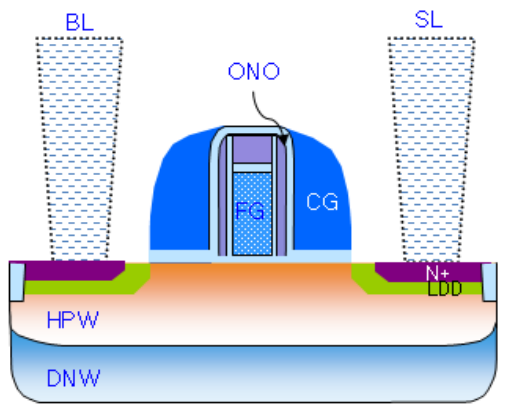
As a small-area solution, we proposed a SSTC (Side-wall selective transistor cell) EEPROM cell [3]. Also, we proposed a DB (Data bus) sensing circuit of the digital sensing scheme which does not require its reference voltage generator to reduce the stand-by current, and a low-power DC-DC converter [4]. Furthermore, we proposed a circuit design technique of distributed DB scheme to obtain a high-speed operation [3].

In this paper, the memory space of the EEPROM is separated into a program region of 256 kbits and a data region of 4 kbits. An option memory region of 2 kbits is added for storing user IDs, serial numbers, security codes and so on. As a small-area technique, by making HPWs (High-voltage P-wells) of the EEPROM cell arrays with the same bias voltages in accordance with the operation modes shared in a double word unit, we can reduce the HPW-to-HPW space and hence the area of the EEPROM cell arrays. Since there is a problem of taking a long time testing the EEPROM if writing (erasing or programming) is done word by word, we reduce the test time using a page buffer circuit of 32 words (=512 bits). In case of a 100,000 write endurance and a ten-year retention time of the EEPROM for a MCU, we should consider VT (threshold voltage) variations of EEPROM cells. In consideration of these VT variations, we propose a write-verify-read mode of reading the EEPROM cells with an external voltage VRD allowing for VT shifts in the wafer test. Also, we propose a DC-DC converter scheme operating with the wide voltage range of 1.8 V to 5.5 V. Furthermore, we present a method of obtaining the period of a ring oscillation using a NTC (Normalized transfer charge) curve in designing a ring oscillator of the DC-DC converter. A 256 kbits EEPROM IP is designed with MagnaChip's 0.18 μm EEPROM process and the layout size of the designed EEPROM IP is 1581.55 μm × 792.00 μm.

II. CIRCUIT DESIGN

A SSTC [3] shown in Fig. 2(a) is used as an EEPROM cell in this paper. The SSTC EEPROM cell has a structure that the CG (Control gate) surrounds the sides of the FG (Floating gate). An insulating material ONO (Oxide-nitride-oxide) is used between the CG and the FG to raise the coupling ratio. The oxide of the SSTC EEPROM cell consists of a thin tunnel oxide of 92 Å and a thick oxide of 300 Å. A DNW (Deep N-well) surrounding the HPW is needed for isolation of the SSTC EEPROM cell since the HPW is applied with a high voltage of 14 V in the erase mode as shown in Fig. 2(b). The thick gate oxide transistor is a HV select transistor. The operation that electrons are ejected from the FG is erasing and the operation that electrons are injected to it is the programming. Erasing and programming are done by the FN (Fowler-Nordheim) tunneling through the tunnel oxide under the FG of the EEPROM cell.

Table 1 shows major specifications of the designed 256 kbits EEPROM IP with 0.18 μm SSTC EEPROM cells. The SSTC EEPROM cell size is 0.99 μm^2. VDD is 1.8 V and the temperature range is between -40 ˚C and 85 ˚C. There are five operation modes: page erase, page buffer load, page program, normal read, and write-verify-read mode. Page erasing and page programming



(a)

Node \ Mode		Page Program			Page Erase		Normal Read		Stand-by
		Selected Column		Non-Selected Column	Selected Column	Non-Selected Column	Selected Column	Non-Selected Column	All
		DIN='0'	DIN='1'						
CG (WL)	Selected Row	16V	16V	16V	0V	0V	VRD	VRD	0V
	Non-Selected Row	0V	0V	0V	11V	11V	0V	0V	0V
Bit Line		10V	0V	10V	14V	11V	VDD	Floating	Floating
Source Line		Floating	Floating	Floating	Floating	Floating	0V	0V	0V
HPW		0V	0V	0V	14V	0V	0V	0V	0V
DNW		VRD	VRD	VRD	14V	14V	VRD	VRD	VRD

(b)

Fig. 2. SSTC EEPROM cell: (a) Cross-sectional view, (b) Bias voltage conditions in accordance to the operation modes.

Table 1. Major specifications of a 256 kbits EEPROM

Process		MagnaChip's 0.18 μm EEPROM
EEPROM Cell		SSTC
Cell Array	Program Memory	256 Rows × 1024 Columns
	Data Memory	4 Rows × 1024 Columns
	Option Memory	2 Rows × 1024 Columns
Supply Voltage (VDD)		1.8 V
Temperature Range		-40 ˚C ~ 85 ˚C
Operation Modes		Page Erase
		Page Buffer Load
		Page Program
		Normal Read
		Write-Verify-Read
		Power Down
Write Bits		512 bits
Read Bits		16 bits
Write Time		2.5 ms
Access Time		100 ns

are done in a unit of 32 words, and page buffer loading and reading in a unit of word.

As shown in the block diagram of the designed 256 kbits EEPROM IP in Fig. 3, the memory space is separated into a program, data, option region. Their respective capacities are 16 kwords, 256 words, and 128 words. The option memory region of 128 words is added for storing user IDs, serial numbers and so on for the convenience of users. We use a page buffer of 32 words to reduce a test time.

For page erasing, a datum of 32 words can be erased by decoding the page address A[15:5] as shown in a timing diagram of Fig. 4. The row decoder activates one of WLs (Word lines) among WL_PM[255:0], WL_DM [3:0], and WL_OM[1:0] which are respective WL signals for the program, data, and option memory region by decoding the row address A[15:6]. In the page buffer load mode, the column address A[4:0] is used to store an word datum DIN[15:0] into the page buffer.

In the read mode, the column address A[5:0] is used to output one of the 64 word data connected to a selected WL through the RD (Read data) switch. The DOUT buffer consists of a RD S/A (sense amplifier) and a tri-state buffer. The selected word datum is outputted to DOUT[15:0] through the tri-state buffer after the datum is sensed by the RD S/A.

The control logic in Fig. 3 generates internal control signals necessary for the operation of the EEPROM in

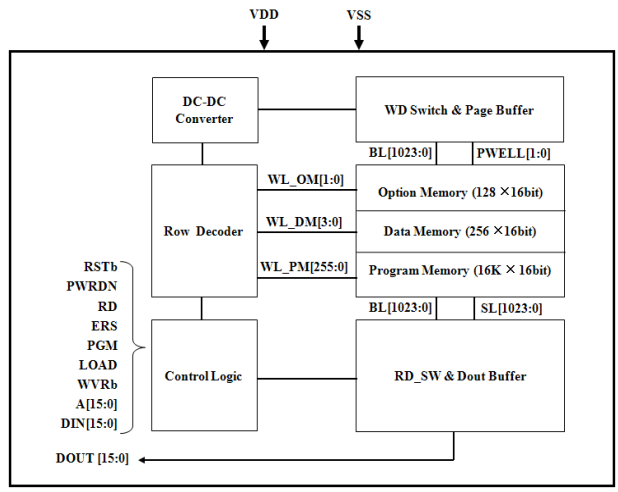


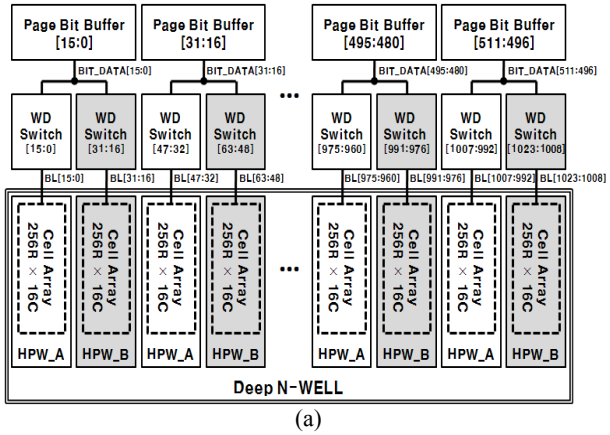
Fig. 3. Block diagram of 256 kbits EEPROM IP.

accordance to the operation modes. The DC-DC converter supplies VRD (Read voltage) in the read mode, and VPP and VPPL in the write mode. Table 2 shows VRD, VPP, and VPPL supply voltages used in the EEPROM IP in accordance to the operation modes. There are control signals (RSTb, PWRDN, RD, ERS, PGM, LOAD, and WVRb), address A[15:0], input data DIN[15:0], and output data DOUT[15:0] as interface signals on a large scale.

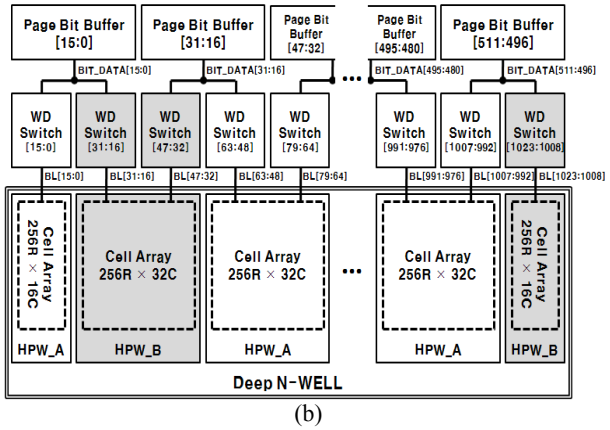
The HPW voltage of the EEPROM cell array should be biased to 14 V for the selected words and 0 V for non-selected words in the erase mode. The HPWs are separated in a unit of word to apply the different voltages in the erase mode. The page read and page program mode of the 256 kbits EEPROM select 32 words of 64 words. Fig. 4 shows EEPROM cell array arrangement schemes. Fig. 4(a) shows an arrangement of an isolated HPW in a word unit and the scheme has 64 isolated HPWs. The HPW-to-HPW space is 1 μm and hence the layout size of the cell array becomes bigger. In this paper, we use an arrangement of sharing HPWs which have the same applied bias voltage as shown in Fig. 4(b). As a result of this arrangement, the 256 kbits EEPROM cell array size is reduced from 0.357 mm^2 to 0.324 mm^2, smaller by about 9.1 percent.

Table 2. Supply voltages of DC-DC converters in accordance to the operation modes

	Erase	Program	Read	WVR
VRD	3.15 V	3.15 V	3.15 V	2.5 V
VPPL	11 V	10 V	VRD	VRD
VPP	14 V	16 V	VRD	VRD



(a)



(b)

Fig. 4. EEPROM cell array arrangement schemes: (a) arrangement of an isolated HPW in a word unit, (b) arrangement of sharing a HPW in a double word unit.

A page buffer circuit should be used to reduce a test time related to writing the EEPROM IP. A timing diagram is shown in Fig. 5 in the program mode using the page buffer. There are the page buffer mode of 32 words and the page program mode as program modes. If a page program signal PGM is applied after the page buffer is loaded, a page buffer output BIT_DATA[511:0] in Fig. 4(b) is transferred to 512 BLs of BL[1023:0] through selected WD (Write data) switches and programmed into the corresponding EEPROM cells of 512 bits (=32 words). Table 3 shows comparisons of calculated erase and program time per page between without a page buffer and with a page buffer. As shown in Table 3, the write time (erase and program time) per page is sufficient with the time of writing one word because of using the page buffer. Thus, the EEPROM test time can be reduced.

Fig. 6 shows a conventional page buffer circuit which consists of a byte flag latch and a data bit latch [5]. If LOAD is activated high in the page buffer load mode, the byte flag latch of the selected byte is set and the data bit latch is loaded with the input datum. When the page buffer is loaded in the conventional page buffer circuit, the input datum is overwritten in the inverter latch surrounded with a dotted line in Fig. 6 through NMOS pass transistors MN0 and MN1. The widths of the transistors MN0 and MN1 using HV devices to overwrite the inverter latch should be wider and hence the layout size becomes bigger. Also, a V_T loss can occur since VPP is transferred through the NMOS pass transistor MN1 in the page program mode.

Table 3. Comparisons of calculated erase and program time per page between without a page buffer and with a page buffer

	Without page buffer	With page buffer
Erase time/page	80 ms	2.5 ms
Program time/page	80 ms	2.5064 ms

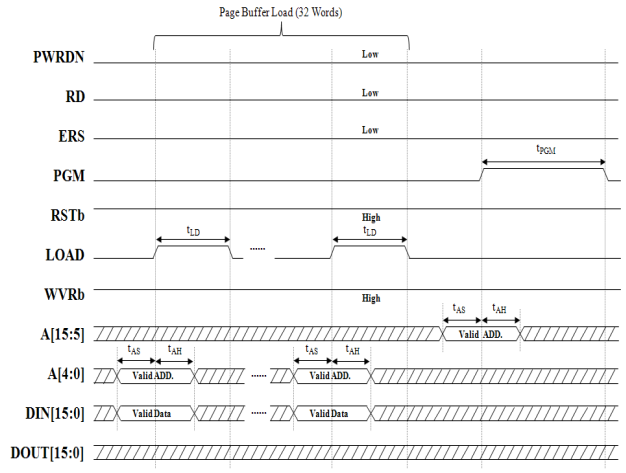


Fig. 5. Timing diagram of 256 kbits EEPROM in the program mode.

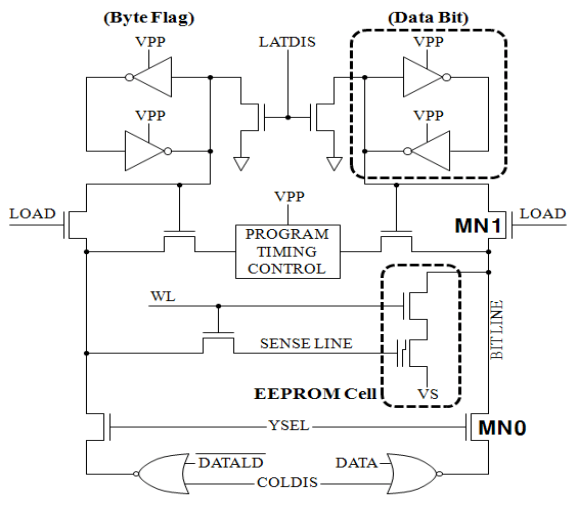


Fig. 6. Conventional page buffer circuit with an EEPROM cell.

A page buffer circuit proposed in this paper uses a VDD-to-VPP voltage level translator circuit instead of a NMOS pass transistor. Also, a V_T loss is eliminated since a CMOS transmission gate of HV devices is used in the page program mode. The page buffer circuit proposed in Fig. 7(a) consists of an input data latch and a voltage level translator. To write the EEPROM, we should write a page datum to be programmed after the page datum is erased in the page erase mode. In the page erase mode, PAGE_RST is activated high by an erase pulse and then the datum stored in the latch LAT_DATA is resetted to be 0 V. The resetted latch output LAT_DATA is outputted to BIT_DATA through the voltage level translator. The BIT_DATA outputs VPP in the page erase mode.

Each BL voltage, each column to be erased through the selected WD switch circuit in Fig. 7(b), is driven with VPP. In the page erase mode, selected BLs are driven with VPP and non-selected BLs with VPPL. The WD drive circuit can eliminate a V_T loss in transferring VPP since it uses a CMOS transmission gate. In the page buffer load, page buffer write signals PB_WRT and PB_WRTb are applied with VDD and 0 V and hence the CMOS transmission gate TG0 is turned on. The program input datum PGM_DATA is latched into the data latch through TG0 which is turned on. The latched datum LAT_DATA outputs VPPL when the input datum DIN is '0' and 0V when DIN is '1' through the voltage level translator. When the page buffer is loaded with 32 words to be programmed to perform a page program, the 32 words are programmed into selected EEPROM cells by the page program pulse PGM in Fig. 5. The HV NMOS transistor connected to BLC_EN in Fig. 7(b) preconditions BL to 0 V in exiting from the write mode.

In regard of a 100,000 write endurance and a ten-year retention time for MagnaChip's 0.18 μm EEPROM cell, VT of the erased cell can be about 0.5 V higher and that of the programmed cell can be about 0.5 V lower. Without any consideration of those endurance and retention time in the wafer test, problems can occur in the field. Thus, we design the cell to secure a reliability characteristic by applying a voltage lower than VRDmin in reading an erased cell and a voltage higher than VRDmax in reading a programmed cell to the VRD_EXT (External read voltage) pad in this paper. For the designed 256 kbits EEPROM, VRD (Internal read voltage)

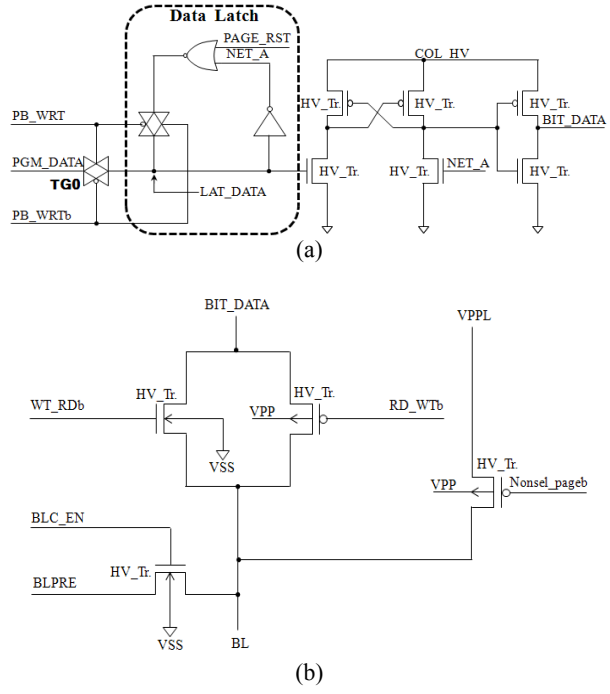


Fig. 7. (a) Proposed page buffer circuit, (b) WD switch circuit.

is in the range of 3.0 V to 3.3 V by a charge pumping. Fig. 8 shows a VRD switch circuit. VRD_CP is generated by a pumping of the internal charge pump and VRD_EXT is supplied by a wafer probing pad. In the normal read mode, the PMOS transistor MP0 in Fig. 8 turns on and hence VRD is supplied with VRD_CP. Also, VRD is supplied with VRD_EXT through the turned-on transistor MP1 since WVRb is applied with 0 V in the write-verify-read mode. Fig. 9 shows a timing diagram in the write-verify-read mode. It is possible to do a function test considering cell reliability characteristics since the EEPROM cell is read out with an external voltage VRD allowing for VT shifts in the wafer test.

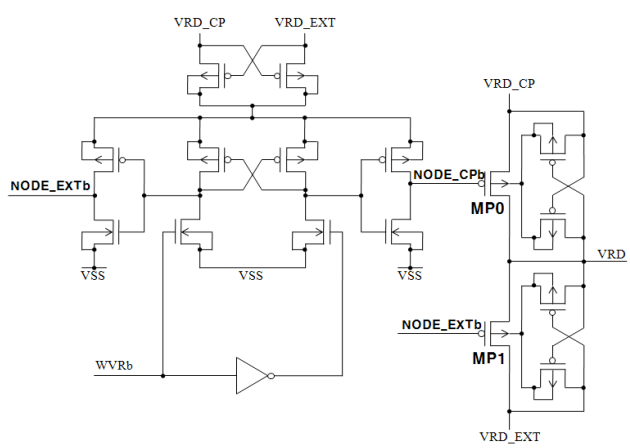


Fig. 8. VRD switch circuit.

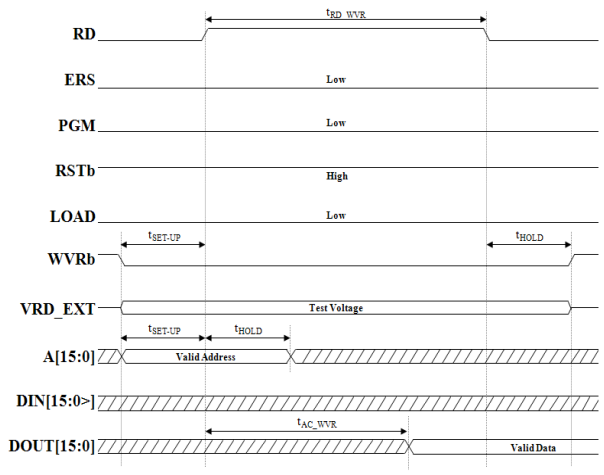


Fig. 9. Timing diagram of EEPROM in the write-verify-read mode.

VRD, VPP, and VPPL are required in the normal read and write mode of the EEPROM cell. An EEPROM design technique with the wide voltage range of 1.8 V to 5.5 V is also required for EEPROMs used in a MCU applied to both mobile devices and household appliances. On the other hand, it is difficult to obtain the VRD voltage of 3.15 V needed for the EEPROMs in the normal mode by linear-regulating of the VCC voltage with the wide voltage range of 1.8 V to 5.5 V. In this paper, we assume that the VDD voltage of the designed EEPROM IP will be supplied from a voltage regulator of an MCU chip. By applying the linear-regulated VDD (=1.8 V) voltage as an input voltage of a DC-DC converter, the boosted VRD voltage is generated. Also, the VDD voltage is designed based on a target specification of 1.8 V ± 10%. Any MCUs can supply this VDD voltage easily to meet the target specification of the VDD voltage by linear-regulating the VCC voltage with the wide voltage range of 1.8 V to 5.5 V. Thus, VRD can supply its target voltage of 3.15 V stably by the charge pumping method although the VCC voltage falls below the VRD voltage. Since the VDD voltage is used as the input voltages of charge pump circuits (VRD, VPP, and VPPL) like this, the supply voltages of DC-DC converters in Table 2 can be supplied stably with the VCC of 1.8 V or above. They can be operating normally for the VCC of 1.8 V to 5.5 V.

Fig. 10 shows a block diagram of the VRD_CP generation circuit by a charge pumping scheme with a voltage VDD. The VRD_CP generation circuit consists of a 2-stage cross-coupled charge pump, a control logic, a ring oscillator, a VRD_CP level detector, and a bandgap reference voltage generator. When VRD_CP is lower than the target voltage, VRD_EN, which is the output signal of the VRD_CP level detector, goes high. Then, VRD_CP goes high as well by a positive charge pumping. When VRD_CP is higher than the target voltage, VRD_EN becomes low. Then VRD_CP can be stable at the target voltage of 3.15 V by the negative feedback mechanism. The reference voltage VREF_VRD (=1.05 V) of the VRD_CP level detector is generated by the bandgap reference voltage generator. Fig. 11 shows a unit charge pump using a cross-coupled charge pump. We reduce the layout size by using a 5 V NMOS capacitor of 2.76 fF/μm^2 instead of a MIM (Metal-insulator-metal) capacitor of 1.1 fF/μm^2 as a pumping capacitor of the pumping circuit and a charge reservoir capacitor at the output of the VRD generation circuit.

Memory capacity of an EEPROM used in a RFID tag chip is mostly 4 kbits or below [6, 7]. A VPP and VPPL generation circuit designed for the RFID tag chip is as shown in Fig. 12 and the loading current of VPPL is small.

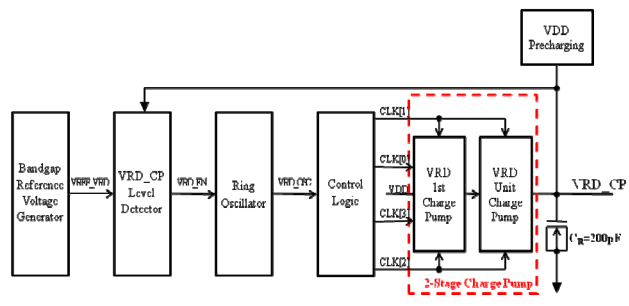


Fig. 10. Block diagram of VRD generation circuit.

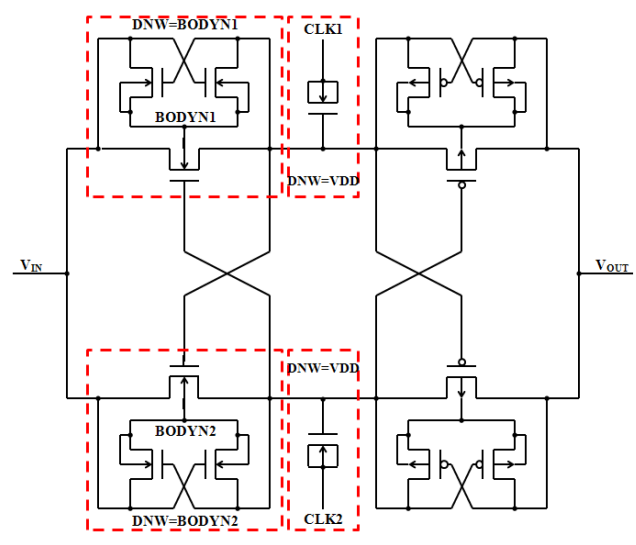


Fig. 11. Unit charge pump circuit of VRD.

Thus, we designed the VPP and VPPL generation circuit generating VPP with a Dickson charge pump and a VPPL switching circuit selecting needed VPPL_PGM and VPPL_ERS in accordance to the respective program and erase mode by using an arbitrary node of the Dickson charge pump [4]. On the other hand, it is necessary to design separate VPP and VPPL charge pumps since their loading currents are big for a 256 kbits EEPROM used in a MCU. Hence we design the separate VPP and VPPL charge pumps as shown in Fig. 13.

III. SIMULATION RESULTS

Fig. 14 shows function simulation results in the read mode under a condition of VDD = 1.62 V, temperature = 85 ˚C, and slow model parameters. Fig. 14(a) and (b) show voltage waveforms in the normal read and write-verify-read mode. When WL is activated after BL is precharged, a datum of cells transfers to DLINE through BL, and then the datum on the DLINE is sensed by RD S/A (Read data sense amplifier) and outputted to DOUT if SAENb signal is activated low after a sufficient transfer of the cells to the DLINE. Fig. 14(b) shows a simulation result in the write-verify-read mode with VRD_EXT (=2.5 V) applied. Since it take a longer time for the datum to develop on the DLINE since VRD lower than VRD_EXT in the normal read mode is applied. Thus, a S/A enable signal SAENb is delayed more by 35 ns or so.

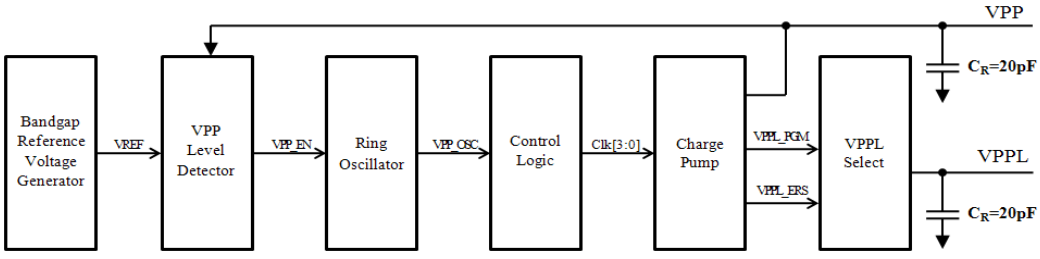


Fig. 12. Conventional VPP and VPPL generation circuit.

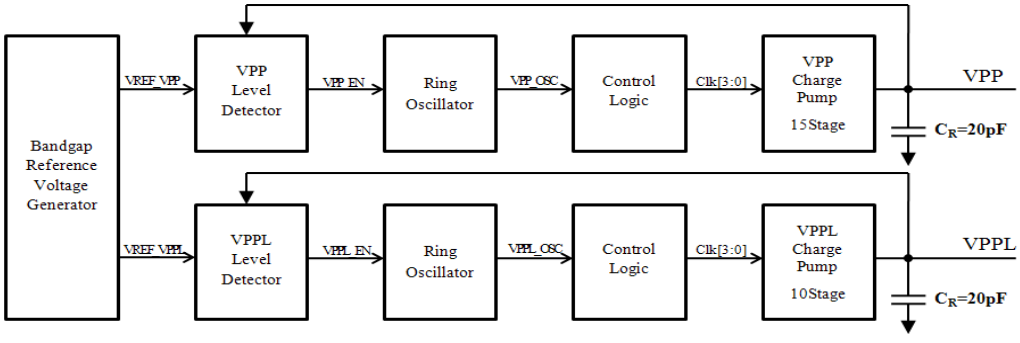


Fig. 13. Proposed VPP and VPPL generation circuit.

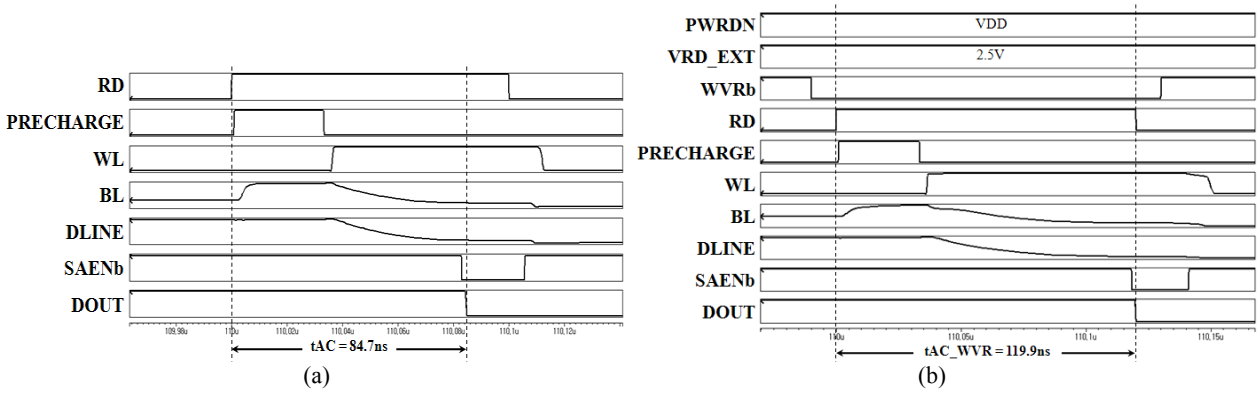
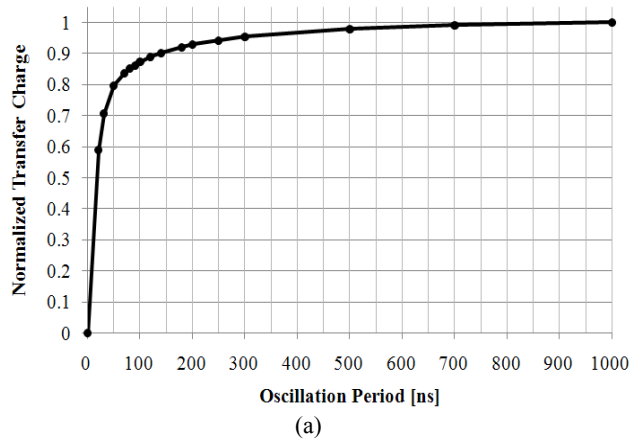


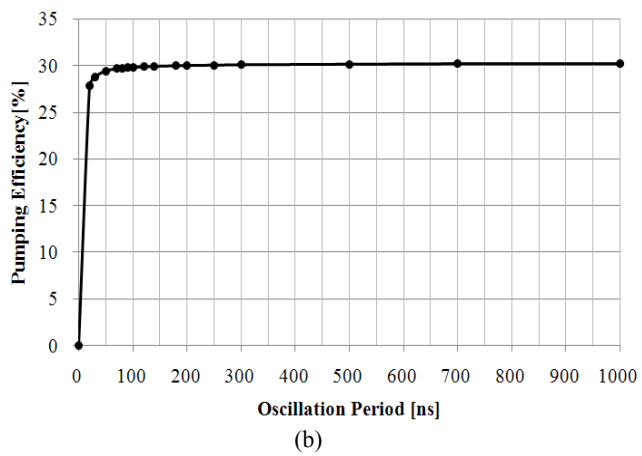
Fig. 14. Simulation results in the read mode : (a) normal read mode, (b) write-verify-read mode.

In this paper, we present a method of obtaining the period of a ring oscillation in a charge pump. Fig. 15(a) shows a NTC (Normalized transfer charge) curve with respect to ring oscillation periods of the designed VRD charge pump. A NTC means pumping charges transferred to the output node with a given oscillation period normalized by those with a sufficiently long oscillation period. As a ring oscillation period is short, its NTC value becomes short. In this paper, the VRD charge pump is designed with an oscillation period of which the NTC is 0.8. We can obtain an efficiency of about 30 percent, about 33.3 percent of the efficiency of an ideal charge pump, with an oscillation period of 50 ns as shown in Fig. 15(b) and the pumping current is 180 μA.

Fig. 16 shows a layout image of the designed 256 kbits EEPROM IP with MagnaChip's 0.18 μm EEPROM process and its size is 1581.55 μm × 792.00 μm.



(a)



(b)

Fig. 15. Simulation results of VRD charge pump circuit with respect to its ring oscillator periods: (a) NTC curve, (b) pumping efficiency curve.

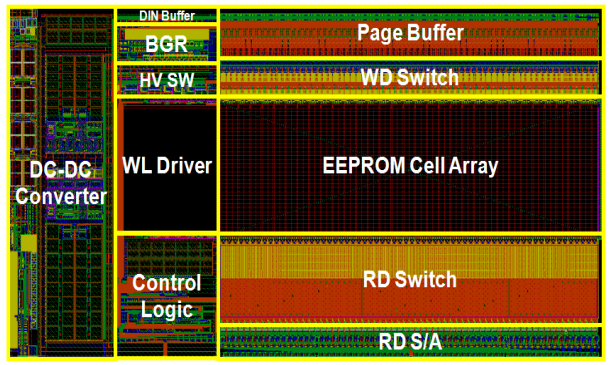


Fig. 16. Layout image of the designed EEPROM IP with Magnachip's 0.18 μm EEPROM process.

IV. CONCLUSIONS

The memory space of the EEPROM for a MCU in application fields of mobile devices and household appliances is required to be separated into a program, data, and option region. The option region is needed for storing user IDs, serial numbers and so on. Also, the EEPROM should be designed to be operated in the wide range of 1.8 V to 5.5 V, and in a small area. Furthermore, a 100,000 write endurance and a ten-year data retention time should be guaranteed.

In this paper, the memory space of the EEPROM was separated into a program, data, and option region. By making HPWs (High-voltage P-wells) of the EEPROM cell arrays with the same bias voltages in accordance with the operation modes shared in a double word unit, we could reduce the HPW-to-HPW space by a half and hence the area of the EEPROM cell arrays by 9.1 percent. Also, we proposed a page buffer circuit reducing a test time and a write-verify-read mode securing a reliability of the EEPROM. Furthermore, we proposed a DC-DC converter that could be applied to a MCU with the wide voltage range of 1.8 V to 5.5 V. Finally, we came up with a method of obtaining the oscillation period of a charge pump.

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