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간단한 위상 보간기 기반의 스프레드 스펙트럼 클락 발생 기술

(A Simple Phase Interpolator based Spread Spectrum Clock Generator Technique)

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(Kyoungrok Lee, Jaehee You, and Jongsun Kim)

요 약

본 논문에서는 전자기파 장애(EMI)의 감소를 위한 위상 보간기 기반의 새로운 스프레드 스펙트럼 클락 발생기(SSCG)를 제시한다. 제안하는 SSCG는 낮은 설계 복잡도와 저전력 및 작은 칩면적을 갖으며 삼각 주파수 변조를 이루기 위해 디지털적으로 조절 가능한 위상 보간 방식을 사용하였다. 이 새로운 SSCG는 듀티 싸이클 왜곡 없이 200MHz에서 ±2%의 센터-스프레드 스펙트럼 범위를 갖는 시스템 클락을 발생시킬 수 있다. 이 위상 보간기 기반의 SSCG 회로는 200MHz에서 약 5.0 mW의 전력을 소모하고, 0.18-um 1.8-V CMOS 공정을 사용하여 설계하여 검증하였으며 0.092mm^2 의 칩 면적을 차지한다.

Abstract

A compact phase interpolator (PI) based spread spectrum clock generator (SSCG) for electromagnetic interference (EMI) reduction is presented. The proposed SSCG utilizes a digitally controlled phase interpolation technique to achieve triangular frequency modulation with less design complexity and small power and area overhead. The novel SSCG can generate the system clock with a programmable center-spread spectrum range of up to +/- 2 % at 200 MHz, while maintaining the clock duty cycle ratio without distortions. The PI-based SSCG has been designed and evaluated in 0.18-um 1.8-V CMOS technology, which consumes about 5.0 mW at 200MHz and occupies a chip size of 0.092mm^2 including a DLL.

Keywords: Spread spectrum clock, SSCG, Frequency modulation, phase interpolator, EMI

I. Introduction

As the physical size and the resolution of liquid crystal display (LCD) TV panels increases, electromagnetic interference (EMI) is increasing as a result of higher clock speed and longer interconnect lines between chips on an LCD panel board. Conventional EMI reduction techniques, such as adding shielding of the box and using EMI filters, are useful but increase the cost of LCD products. One well-known and cost-effective method to reduce EMI is spread-spectrum clocking (SSC)[1] which modulates the system clock and spreads the clock signal energy over a much wider frequency bandwidth. Spread spectrum clock generator (SSCG) chips are widely used in LCD display to reduce EMI as an IC-level approach to meet regulations such as Federal Communications Commission (FCC) rules[2~3]. Traditional SSCGs are typically implemented based

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on phase-locked loops (PLLs)[4~6]. PLLs usually have higher jitter characteristics due to phase noise accumulation and have difficulties in designing due to stability issues. Therefore, PLL-based SSCGs are not readily adaptable to implementation in conjunction with digital circuits with high substrate noise. A delay cell array (DCA) based digital SSCG was proposed in [7] to overcome the random period jitter of PLLs. However, this DCA-based SSCG requires a significant number of cascaded inverter delay cells, increasing the power (120 mW at 100 MHz), propagation delay, and area overhead seriously. In this letter, a novel compact digital SSCG for LCD display EMI reduction is proposed. The proposed PI-based SSCG utilizes a digitally controlled phase interpolation technique to generate a center-spread clock signal without clock duty cycle distortions. The PI-based SSCG ,designed and evaluated in 0.18-um CMOS technology, consumes 5.0 mW at 200 MHz, which is only 4 % of the DCA-based SSCG[7] at 100 MHz. Since the architecture of the proposed SSCG is very simple and robust, it is easy to design and is easy to integrate on a single-chip with much smaller chip size.

II. Circuit Design

In the proposed design, the PI-based SSCG operates without a PLL. Fig. 1(a) shows the block diagram of the SSCG architecture. A typical DLL is just inserted to provide the reference clock (f_c) operating at 200 MHz. It consists of a typical voltage controlled delay line, a phase detector, and a charge pump. The proposed SSCG consists of a programmable delay buffer (DB), a DAC counter, a current-steering 8-bit digital-to-analog converter (DAC), a CML to CMOS buffer, and a digitally controlled phase interpolator (PI). The frequency of the output clock (SSCLK) is shifted by changing the interpolation delay of the PI for each cycle. The total amount of the frequency spreading range (from +/- 0.5 % to +/- 2 %) is controlled by the propagation

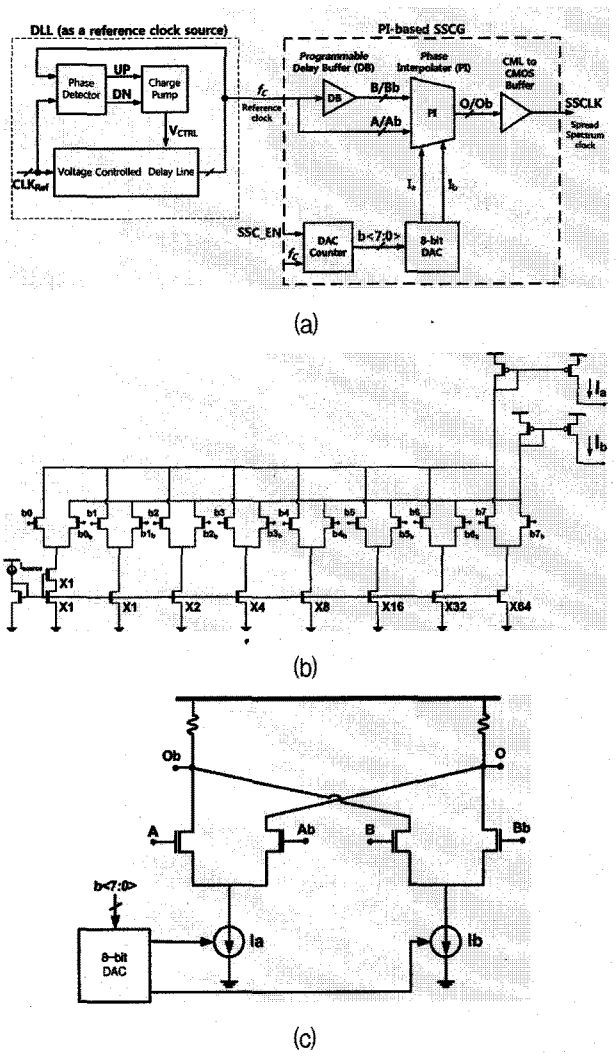


그림 1. (a) 제안된 기준 클락 소스로써 전형적인 DLL를 갖는 PI 기반의 SSCG, (b) 전류 조정형 8비트 DAC, 그리고 (c) 디지털적으로 조절 가능한 PI

Fig. 1. (a) Proposed PI-based SSCG with a typical DLL as a reference clock source, (b) current-steering 8-bit DAC, and (c) digitally controlled phase interpolator (PI).

delay amount of the programmable DB which consists of typical differential pairs and capacitive loads with digital control inputs. Unlike the conventional PLL-based SSCGs[4~6] and DCA-based SSCG[7] consuming large power consumption and occupying large chip area, this new SSCG provides slightly spread digital clock signal while minimizing the area and power overheads dramatically.

The binary-weighted current-steering 8-bit DAC, shown in Fig. 1(b), is controlled by the DAC counter and is used to provide programmable bias currents I_a

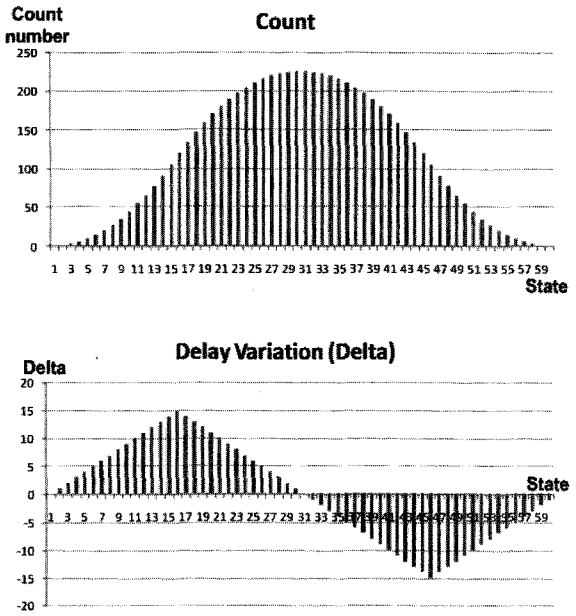
and I_b to the PI. The DAC settling time and the glitch level for one LSB change is important in order not to cause excessive phase jitter at the PI. The DAC counter has 8-bit output vectors (b<7:0>) for programmable interpolation delay control. The digitally controlled PI shown in Fig. 1(c) receives two differential small-swing signals (A/Ab and B/Bb) from the DB and interpolates between them to generate an intermediate phase signal (O/Ob) whose phase is dependent on the DAC current of I_a and I_b. Thus the phase of the PI is digitally controlled by the DAC counter sequence and the 8-bit DAC current variation. Interpolation between the two inputs is performed by changing the tail current of I_a and I_b in Fig.1(c) where I_a+I_b is aconstant. As I_b increases, I_a is decreased and the phase of the output signal (O/Ob) approaches that of the input signal B/Bb. This can be expressed as follows:

$$I_a + I_b = (1-x)*I_a + x*I_b = \text{constant} \quad (1)$$

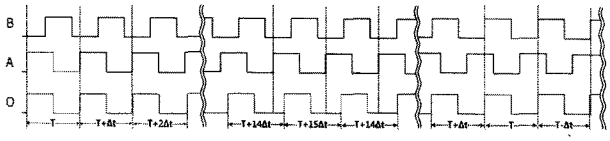
where $0 < x < 1$.

The digitally controlled phase modulation technique is described more in detail in Fig. 2. Fig. 2(a) shows the pattern generation of the DAC counter. The 8-bit DAC counter has 60 total states. When SSC_EN is off, the DAC counter resets to state 0 with output count b<7:0> =[00000000]=0. When SSC_EN is applied for spread spectrum turned on, the DAC counter changes the state from 0 to 59 sequentially at every input clock and then returns to state 0 again to repeat this sequence. The PI will delay the interpolated output signal (O/Ob in Fig. 1(c)) depending on the count value given in Fig. 2(a) for each state. Fig. 2(a) (lower) also shows the effective delay variation delta of the PI, which shows triangular delay variation for frequency modulation. Therefore, the linearly increased and decreased delay delta will produce a spread clock. When using an 8-bit DAC, the modulation frequency (f_m) and the delta (Δt) can be expressed as follows:

$$\text{Modulation frequency } (f_m) = 1/(T*60) \quad (2)$$



(a)



(b)

그림 2. (a) DAC 카운터 패턴(위) 그리고 삼각 주파수 변조를 위한 PI의 딜레이 변동(아래), (b) 시간축에서의 PI의 두 입력신호(A, B)와 변조된 출력신호(O) 사이의 주기 비교

Fig. 2. (a) DAC counter pattern (upper) and the delay variation of the PI for triangular frequency modulation (lower), (b) period comparison between the two input signals (A, B) and the modulated output signal (O) of the PI in time domain.

$$\text{Delta } (\Delta t) = t_{bdelay}/2^8 \quad (3)$$

where T is the input clock period ($=1/f_c$), t_{bdelay} is the delay amount of the programmable DB, and f_c is the original input clock frequency. The frequency range (Δf) can be determined as follows:

$$f_c + \Delta f = f_{max} = 1/(T - 15*\Delta t) \quad (4)$$

$$f_c - \Delta f = f_{min} = 1/(T + 15*\Delta t) \quad (5)$$

Fig. 2(b) shows the period comparison between the two input signals (A, B) and the modulated output signal (O) of the PI in time domain. As described in

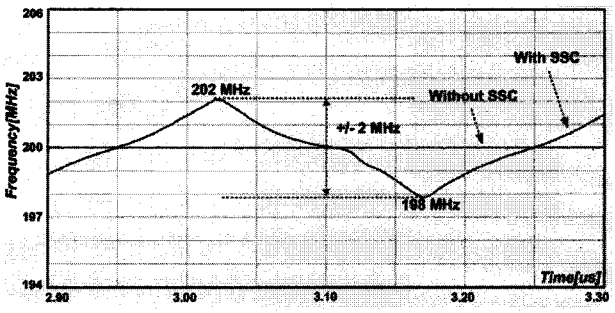
this figure, triangular frequency modulation can be achieved for every 60 cycles by changing the output clock (O) period sequentially as T, T + 1*Δt, T + 2*Δt, T + 3*Δt, ···, T + 15*Δt, T + 14*Δt, T + 13*Δt, ···, T + 1*Δt, T, T - 1*Δt, T - 2*Δt, ··· , T - 15*Δt, T - 14*Δt, ···, T - 1*Δt. The triangular wave was chosen because it has a reasonably flat power density in the frequency domain. One another important advantage of this SSCG is that the duty cycle ratio of the modulated clock remains unchanged without distortions. Thus, the proposed PI-based SSCG provides for center-spread spectrum clock generation with a simple digital interpolating structure that is readily integrated on a single chip and also adaptable to low-cost LCD panel EMI reduction applications. Also, this architecture is more suitable for use in Gbps LCD interface communication between a TV-controller SOC and an LCD-panel timing controller, since the required modulation frequency would be higher than 1 MHz.

III. Simulation Results

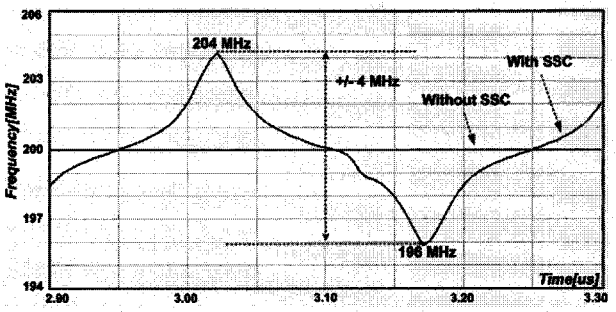
The proposed SSCG has been designed in 0.18-um CMOS technology. Fig. 3(a) shows the HSPICE simulated triangular frequency modulation profile for a center-spread of +/- 1 % (= +/- 2 MHz): Without SSC (SSC_EN = 0), the center clock frequency is 200 MHz. With SSC (SSC_EN = 1), the 200 MHz clock is modulated between 198 MHz and 202 MHz without duty cycle ratio distortions.

Fig. 3(b) shows the HSPICE simulated frequency modulation profile for a center-spread of +/- 2 % (= +/- 4 MHz) from 196 MHz to 204 MHz. Thanks to the increased nonlinearity characteristic of the PI, the modulation waveform of Fig. 3(b) looks like Hershey Kiss profile which can give the best performance in EMI reduction.

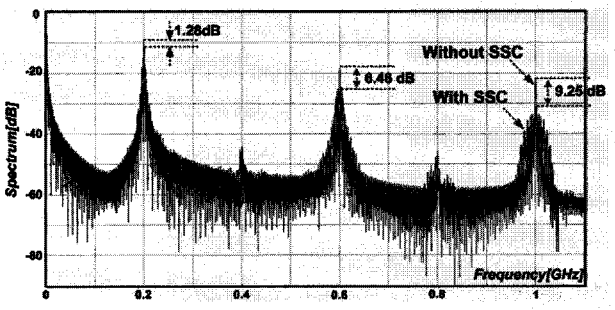
The power dissipation of the PI-based SSCG is about 5.0 mW from a supply voltage of 1.8 V at 200 MHz. The modulation frequency (f_m) was set at 1/(5ns * 60) = 3.333 MHz by using the 8-bit DAC



(a)



(b)



(c)

그림 3. (a) 200MHz에서 +/- 1.0 %의 중심 확산시킨 시뮬레이션 한 주파수 변조 프로파일, (b) 200MHz에서 +/- 2.0 %의 중심 확산시킨 시뮬레이션 한 주파수 변조 프로파일, (c) FFT 시뮬레이션 결과

Fig. 3. (a) Simulated frequency modulation profile with and without SSC at 200 MHz for center spread of +/- 1.0 % (b) for center spread of +/- 2.0 %, and (c) simulated FFT result.

counter. In [8] it is shown that the energy spreading can be optimized with a suitable selection of the f_m, which is usually close to the resolution bandwidth (RBW) of the EMC receiver. Generally, the EMI receivers used by EMC testing laboratories divide the electromagnetic spectrum into frequency bands approximately 120 KHz wide. For example, the RBW = 100 KHz in the frequency range of 30 MHz < f < 1 GHz and RBW = 1 MHz for f > 1 GHz. If the

표 1. DAC 해상도에 의존하는 변조 주파수
Table 1. Modulation frequencies depending on DAC resolutions.

n-bit DAC	# of states	modulation frequency
8-bit	60	3.33MHz
9-bit	88	2.27MHz
10-bit	124	1.61MHz
11-bit	176	1.14MHz
12-bit	252	793kHz
13-bit	360	555kHz
14-bit	508	394kHz
15-bit	704	284kHz
16-bit	956	210kHz
17-bit	1272	157kHz
18-bit	1660	120kHz
19-bit	2128	94kHz
20-bit	2684	75kHz

modulation frequency (f_m) is larger than the RBW of the EMC receiver, the EMI reduction to the peak-to-peak level of the spread spectrum can be estimated by using the following equation[7, 9].

$$\text{EMI reduction(dB)} = 10*\log(\delta * n * f_c / f_m) \quad (6)$$

where δ is the peak-to-peak spread percentage, f_c is the original input clock frequency, $n * f_c$ is the harmonic frequency, and f_m is the modulation frequency. For a center spread of +/- 2.0 % (δ = 0.04), the estimated EMI reduction values are around 3.8 dB at 200 MHz (n = 1) and 8.5 dB at 600 MHz (n = 3), respectively. Fig. 3(c) shows the simulated FFT result for the same spreading ratio of +/- 2.0 %, which shows a 1.28 dB reduction of the EMI at 200 MHz, 6.46 dB reduction at 600 MHz, and 9.25 dB reduction at 1 GHz, respectively. Note that the difference between the estimated result based on equation (6) and the simulated result is around 2 dB. Compared with the DCA-based SSCG[7] achieving 9 dB reduction at 390 MHz (n = 4) with 120 mW power consumption, the proposed PI-based SSCG achieves relatively good EMI reduction capability with much less power and area overhead. Further EMI reduction can be achieved by either increasing the delay amount of the DB or decreasing the modulation frequency f_m. For example, the modulation frequency can be controlled as small as 120 KHz by using an 18-bit DAC at the cost of some circuit overheads. EMI reduction of 7 dB (n = 1 at 200 MHz) is expected by using a 12-bit DAC, which can generate a modulation frequency of 793 KHz with reasonable circuit overhead. Table 1 illustrates the modulation frequencies depending on the n-bit DAC resolutions. Fig. 4 shows the chip layout of the proposed SSCG with a die area of 0.092mm^2 including a DLL. Table 2 compares the performance of this work with prior works. Compared with the VCO-based SSCG[5] and the digital SSCG[7], the proposed PI-based SSCG achieves traingular frequency modulation with much less power, area, and design complexity.

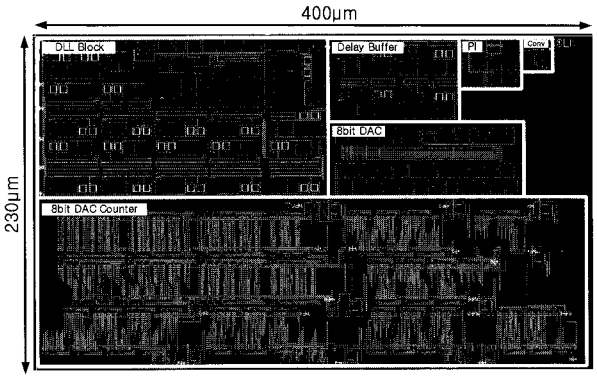


그림 4. 제안된 SSCG의 레이아웃 (DLL 포함)
Fig. 4. Layout of the proposed SSCG. (including a DLL)

표 2. 성능 비교
Table 2. Performance Comparison.

	Chang et al., JSSC 2003 [5]	Kim et al., TEC 2005 [7]	This paper
Modulation Method	VCO	DCA	PI
Modulation Profile	Triangular	Triangular	Triangular
Modulation Type	Center Spread	Center Spread	Center Spread
Target Frequency	266 MHz	100 MHz	200 MHz
Modulation Frequency	40 kHz	50 kHz	3.33 MHz
Spread ratio	0.5, 1, 1.5, 2, 2.5%	1%	2%
Technology	0.35 μm	0.35 μm	0.18 μm
Chip Area	2.013 mm^2	0.306 mm^2	0.092 mm^2
Power Dissipation	300 mW	120 mW	5.0 mW

Ⅳ. Conclusion

A cost-effective and compact technique to control and reduce EMI in LCD panels and high-speed digital applications has been proposed. Unlike the conventional SSCGs based on analog PLLs which usually requiring higher component count and design omplexity, the proposed PI-based SSCG offers programmable spread spectrum clock signal with much less size, power, and cost overhead. By utilizing the digitally controlled phase interpolation technique, the proposed circuit achieves a triangular frequency modulation with a center-spread range of up to +/- 2 % at 200 MHz, while maintaining the clock duty cycle ratio without distortions. The circuit is designed and evaluated in 0.18-um 1.8-V CMOS technology and consumes only 5.0 mW at 200 MHz with a die area of 0.092mm^2 including a DLL.

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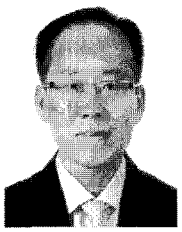

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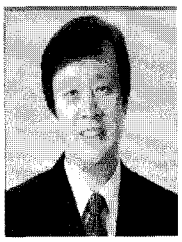

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