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수직형 4-비트 SONOS를 이용한 고집적화된 3차원 NOR 플래시 메모리

(Highly Integrated 3-dimensional NOR Flash Array with Vertical 4-bit SONOS (V4SONOS))

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요 약

수직형 채널을 가지는 4-비트 SONOS 플래시 메모리를 이용하여, 고집적화된 3차원 형태의 NOR 플래시 메모리 어레이를 제안하였다. 수직형 채널을 가지기 때문에, 집적도의 제한 없이 충분히 긴 채널을 가질 수 있다. 이로 인하여, 짧은 채널의 멀티 비트 메모리에서 발생할 수 있는 비트 간의 간섭효과, 짧은 채널 효과, 및 전하 재분포 현상을 해결 할 수 있다. 또한, 제시된 어레이는 3차원 형태를 기반으로 고집적화되어, 발표된 NOR 중에서 최소의 셀 크기 값인 $1.5F^2$/bit을 가진다.

Abstract

We proposed a highly integrated 3-dimensional NOR Flash memory array by using vertical 4-bit SONOS NOR flash memory. This structure has a vertical channel, so it is possible to have a long enough channel without extra cell area. Therefore, we can avoid second-bit effect, short channel effect, and redistribution of injected charges. And the proposed array structure is based on three-dimensional integration. Thus, we can obtain a NOR flash memory having $1.5F^2$/bit cell size.

Keywords: Charge Trap Flash, Multi-bit SONOS Flash Memory

I. Introduction

The floating gate device has been used for non-volatile memory, but the floating gate coupling cross talk issue will limit the scaling to ~40nm node [1]. Beyond that, nitride storage device such as SONOS which is immune to floating gate coupling must be used. Unlike the floating gate, the storage node of SONOS flash memory is the nonconductive nitride layer. So, we can realize 2-bit operation in one cell by charge trapping in the spatially different locations. The multi-bit operation is promising solution to overcome physical limits of device scaling.

Also, in order to overcome the problems of the scaling, 3-dimensional structures have been proposed beyond traditional planar structures[2~4].

In this report, we propose a vertical-type 4-bit SONOS flash memory and its 3-dimensional NOR flash array structure.

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II. Vertical 4-bit SONOS NOR flash memory

If SONOS devices adopt the double gate structure, 4-bit operation can be possible[3]. However, as the channel length is scaled down, several problems restrict reasonable memory device operation. The major limitation is the distribution of injected charges in the storage layer. The electrons injected by CHEI are distributed in the ~30 nm wide nitride layer[6], thus the trapped charges on the both multi-storage node cells would be mixed when the gate length is scaled down to 60 nm level. Moreover, considering the redistribution of injected charges in the retention mode, extra margin must be necessary to distinguish each bit.

Due to these inherent limitations, previous planar type 4-bit double SONOS flash memory (DSMs) has a long channel with 120 nm (2F size)[5].

To solve this limitation, we proposed a vertical 4-bit SONOS Flash Memory (V4SONOS).

Because it has vertical channel, we can obtain a long enough channel within 1F length. So, we can solve redistribution of injected charges without limitation of scaling.

The V4SONOS structure is shown in Fig. 1. Every storage node is formed at the same time, so that symmetric operation can be obtained easily unlike the previous double SONOS memories (DSMs)[5]. The V4SONOS is based on 3-dimensonal array structure. Top bit lines (TBLs) are formed on the active fin line,nal abottom bit lines (BBLs) are buried in the isolation region between word lines. Consequently, there is no extra region to contact bit line. So, we can efficiently organize array related with integration. Therefore physically separated TBL and BBL cross at right angles. And, word lines (WLs) are formed along the of the active fin lines.

Figure 2 shows plane view which corresponds with fig. 1. Owing to unique 3-dimensional composition, it

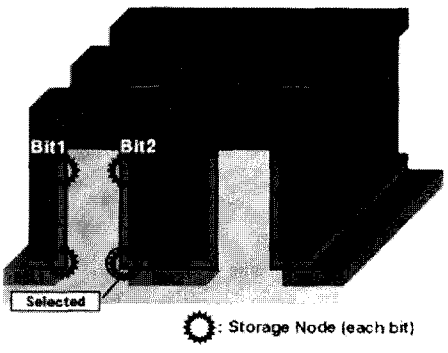


그림 1. 수직형 4-비트 SONOS NOR 구조
Fig. 1. Vertical 4-bit SONOS NOR structure.

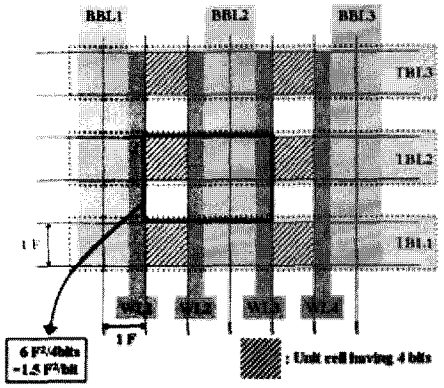


그림 2. V4SONOS 평면도
Fig. 2. Plan view of V4SONOS.

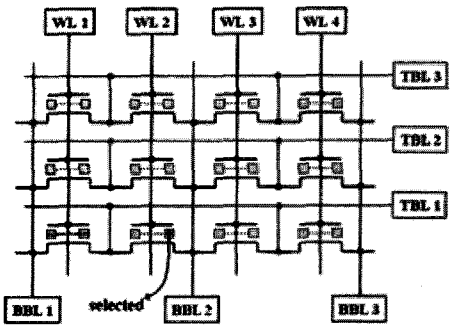


그림 3. V4SONOS NOR 플래시 회로도
Fig. 3. NOR flash circuit diagram of V4SONOS.

표 1. 동작 전압 인가 방식
Table 1. Operation Voltage Scheme.

	Program	Erase	Read
WL1	0V	0V	0V
WL2	6V	-8V	V_{READ}
WL3	0V	0V	0V
WL4	0V	0V	0V
TBL1	0V	0V	1.5V
TBL2	4V	Floating	0V
TBL3	4V	Floating	0V
BBL1	0V	0V	0V
BBL2	4V	4V	0V
BBL3	0V	0V	0V

has the smallest unit cell size (1.5F2/bit) compared with conventional NOR array. The V4SONOS can operate as a NOR type flash memory. Its circuit diagram is shown in Fig. 3. Additionally, Table 1 shows operation voltage scheme of V4SONOS. It uses channel hot electron injection(CHEI) / hot hole injection(HHI) as program / erase, and reverse reading method is used for read.

III. Fabrication Process of V4SONOS

The fabrication process of V4SONOS needs some unique methods. Figure 4 shows the critical fabrication steps of V4SONOS to obtain contact of buried bit lines and self-aligned formation of each cell.

The specific method of each step is as follows.

Fig. 4. (a) : First, Si active fin lines are formed.

The nitride layer on active fin line will be used for CMP stopper. And, the projection pillar of active fin line will make bottom bit line (BBL) contact easy. We will call the projection pillar as bottom bit line connection pillar.

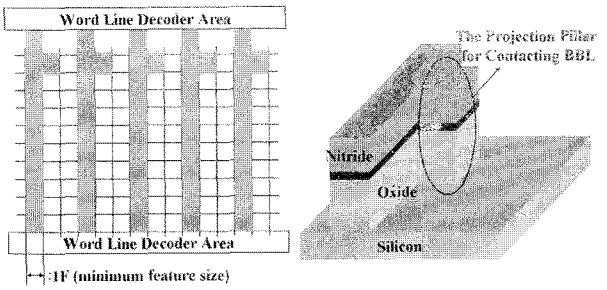
Fig. 4. (b) : Tunneling oxide/nitride/barrier oxide (O/N/O) layers are formed. Then, we make sidewall spacer gate along the active fin line.

Fig. 4. (c) : We isolate both word line sides of active fin line by photolithography. So, we can control right gate and left gate independently. Also, the bottom bit line connection pillar is exposed and the exposed region will be doped with n type in the next step, which is implantation for bottom bit line(BBL).

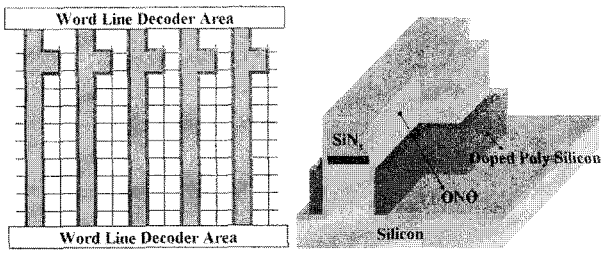
Fig. 4. (d) : The bottom bit line(BBL) is formed by implantation with arsenic. The wafer tilt direction during implantation is important because the bottom bit line connection pillar must connect with buried n-type region.

Fig. 4. (e) : We make ILD layer by deposition of TEOS and CMP. The end point of CMP is determined by nitride layer on the active fin line.

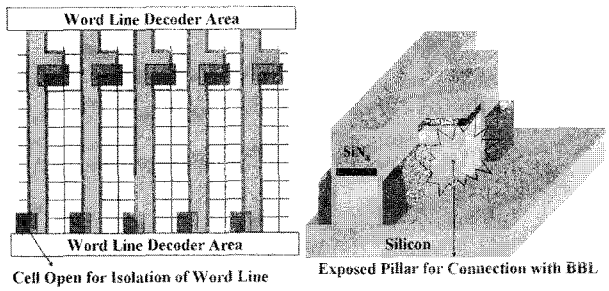
Fig. 4. (f) : The nitride CMP stopper is removed by selective H_3PO_4 et etch. Therefore, the upper surface of active fin line is exposed.



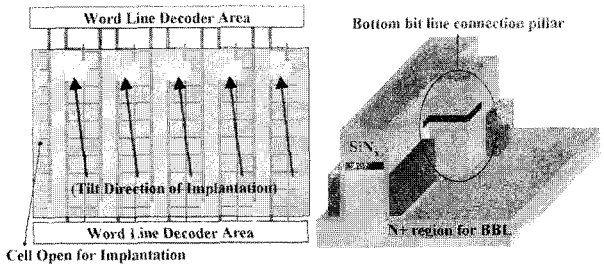
(a) Active formation



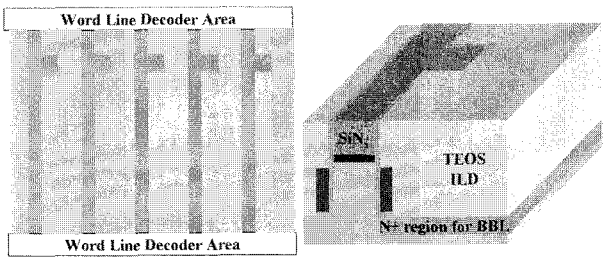
(b) ONO and sidewall gate formation



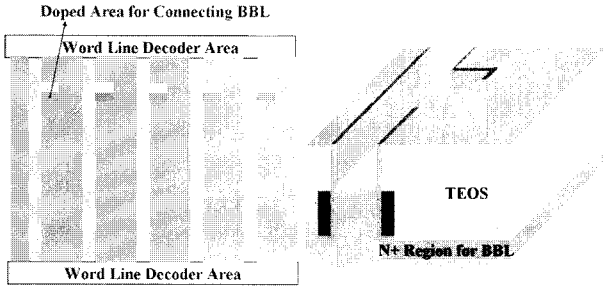
(c) Word line connection



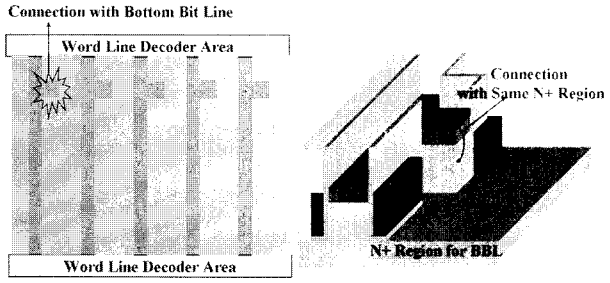
(d) BBL implantation



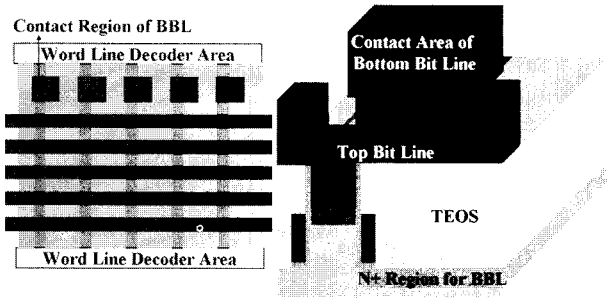
(e) ILD formation



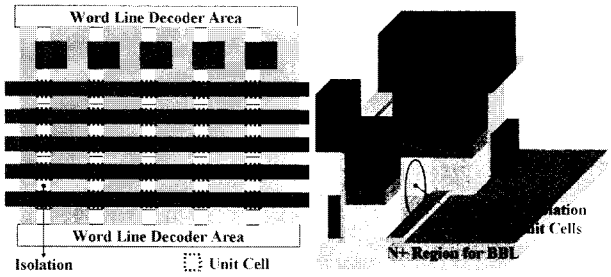
(f) Selective removal of nitride



(g) TBL implantation



(h) TBL, BBL patterning



(i) Isolation between unit cells

그림 4. V4SONOS의 주요 공정 과정
Fig. 4. Critical Fabrication Steps of V4SONOS.

Fig. 4. (g) : The top bit line(TBL) is formed by implantation with arsenic. In bottom bit line connection pillar, connection is achieved between buried n-type region and top bit line.

Fig. 4. (h) : The n+ doped poly-silicon is deposited and patterned to contact TBL and BBL. Because only active fin line is exposed and other region is shielded by TEOS, we can obtain a self-aligned contact.

Fig. 4. (i) : Using the same PR mask that is used for contact of TBL and BBL, we etch the silicon and form trenches. So, we can obtain self-aligned unit cells isolated by trenches.

IV. Memory Characteristic of V4SONOS

To evaluate the cell operation of the U3VNOR, 2D numerical simulation (ATLAS) from SILVACO was utilized. For convenience, the 2-dimensional cut plane of just one pillar is used. Figure 5 and table 2 shows structure and critical dimensions of the V4SONOS used in simulation.

Additionally, we note that because the ATLAS simulation cannot be used directly to simulate the charge trapping of the nitride, the poly-silicon dot (6×30 nm) is inserted in nitride layer for trapping transient simulation(Fig. 5).

Also, the impact ionization rate is a critical model parameter in a point view of the program and erase operation and its formula is given by

$$\alpha(x) = A_i \cdot \exp\left[-\frac{B_i}{E(x)}\right] \quad (1)$$

where A_i and B_i are impact ionization constants. For reliable impact ionization calculation, the impact ionization constants A_i=2.45×10^5/cm, and B_i=1.2×10^7 V/cm were used. These values are extracted by considering the nonlocal carrier heating effect[7].

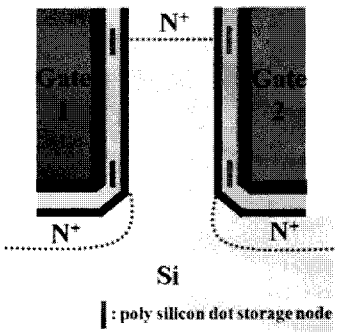


그림 5. 2D 시뮬레이션에서 사용된 구조
Fig. 5. Structure used in 2D simulation.

표 2. 시뮬레이션에 사용된 소자의 주요 변수
Table 2. Critical Dimensions for Simulation.

	Values
Fin width	30 nm
Channel length	200 nm
Storage length	30 nm
Tunneling oxide/nitride/barrier oxide (O/N/O)	4/8/8 nm
P type channel doping concentration	$1\times10^{18}/cm^3$
N^+dopingconcentration	$1\times10^{20}/cm^3$

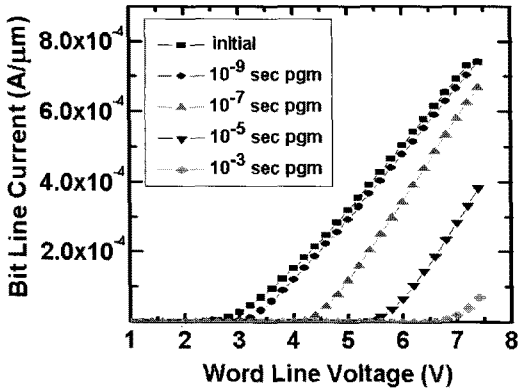


그림 6. V4SONOS의 전달 특성
Fig. 6. I-V characteristics of the V4SONOS. (simulation result)

Figure 6 shows I-V curves related with programming time. After 10^{-3} program time, we can obtain threshold voltage shift with 4V. This shows successful NOR memory characteristics.

V. Scaling Issue of V4SONOS

The key parameter of V4SONOS related with scaling is the fin width. In Fig. 1, Bit 1 and Bit 2 share the same fin line. So there is an interference due to electrical coupling. When we program in Bit 1 (selected bit), unwanted threshold voltage shift occur in Bit 2 (paired bit), also. We named this phenomenon as PCI(Paired Cell Interference). When silicon fin becomes thin, the PCI is more severe and exact read operation is impossible. This interference is the crucial scaling limitation of vertical-type flash memory.

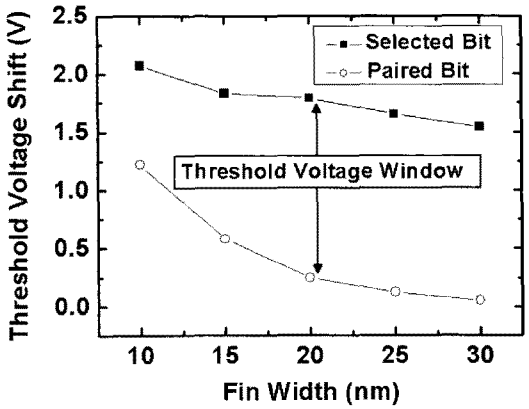


그림 7. 이웃 셀의 간섭효과(PCI)
Fig. 7. Paired Cell Interference (PCI) phenomenon. (simulation result)

Figure 7 show the PCI phenomenon versus a fin width when selected bit is programmed with -1.4×10^{-15}C/um. Through this result, the scaling limitation of a fin width can be expected. If a minimum read margin is 2V, the V4SONOS can be scaled down to 15nm.

VI. Conclusion

We proposed a 3-dimensional future NOR array structure by using vertical 4-bit SONOS (V4SONOS) and its unique fabrication method. Also, we verified memory characteristics and scaling limitation of V4SONOS by numerical simulation. This will be one of the promising structures for scaled multi-bit flash memory.

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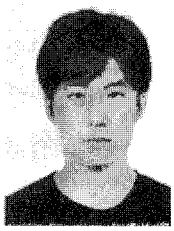
저 자 소 개



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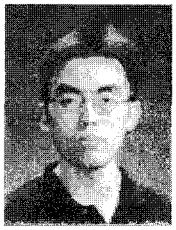

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