Threshold Voltage Dependence on Bias for FinFET using Analytical Potential Model

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Abstract— **This paper has presented the dependence of the threshold voltage on back gate bias and drain voltage for FinFET. The FinFET has three gates such as the front gate, side and back gate. Threshold voltage is defined as the front gate bias when drain current is 1 micro ampere as the onset of the turn-on condition. In this paper threshold voltage is investigated into the analytical potential model derived from three dimensional Poisson's equation with the variation of the back gate bias and drain voltage. The threshold voltage of a transistor is one of the key parameters in the design of CMOS circuits. The threshold voltage , which described the degree of short channel effects, has been extensively investigated. As known from the down scaling rules, the threshold voltage has been presented in the case that drain voltage is the 1.0V above, which is set as the maximum supply voltage, and the drain induced barrier lowing(DIBL), drain bias dependent threshold voltage, is obtained using this model.**

Index Terms— **FinFET(fin field effect transistor), threshold voltage, 3D Poisson's equation, short channel effect, DIBL**

I. INTRODUCTION

AS the size of MOSFET has been scaled down, the performance of MOSFET in high frequency has also been degraded due to SCEs(Short Channel Effects). The problems to occur according to decreasing the size of device, i.e. SCEs are the threshold voltage roll-off, increasing of subthreshold swings, DIBL(Drain Induced Barrier Lowing) and the likes. The FinFET is novel device to have the potential for the down sizing dimension below 45nm[1]. The scaled-down devices improves the performance in IC, and makes production cost go down even though SCEs occur. The performance of MOSFET has been influenced on scaling down of channel, and two-dimensional electrostatic effects become important factor in the mechanism of carrier transport. Thus the ability of electrostatic control by gate bias has decreased due to the increasing charge sharing from source/darin when the channel scaled down[2]. As the results of SCEs, the subthreshold current increases and device performance is degraded. Since the FinFETs have, however, three gates, ability of electrostatic control is improved nearly twice.

The threshold voltage is the most important factor to design the ICs since the threshold voltage determines ON/OFF of devices. Therefore we need the complete models of the threshold voltage to extend and facilitate the use of FinFET in IC. G. Katti et al. have presented an 2D(two dimensional) analytical model for the threshold voltage of mesa-isolated fully depleted ultrathin SOI MOSFET[3]. This model has analytically solved 2D Poisson's equation using quasi-2D method. It is not enough to take into account SCEs, but this model considers two dimensionally the narrow width effects. The charge sharing model to develop Yau's charge sharing model[4,5] for the analytical threshold voltage model does not include the solution of 3D Poisson's equation. The 3D analytical threshold voltage including NWEs(narrow width effects) has been presented in only bulk MOSFET [6]. Katti et al. have reported the 3D analytical model for SOI MOSFET to involve the SCEs and NWEs[7]. We use Katti's analytical potential model and current model for FinFET as solving 3D Poisson's equation. Using this analytical potential model, the transfer relationship of gate voltage and drain current is calculated, and the threshold voltage for different bias values is obtained. The FinFETs have two bias contact such as front and back bias, and source/drain bias. Even though many definitions for the threshold voltage have been reported the threshold voltage is defined as the front gate bias when drain current is $10^{-6}A$ as the onset of the turn-on condition in this paper [8].

The analytical potential model is mentioned from solving analytically 3D Poisson's equation in Sec. II. Comparing with 3D numerical results, the analytical model is verified and the threshold voltage and the drain induced barrier lowing are calculated using analytical potential model for different values of back gate bias and source/drain bias in Section III. Conclusions are provided in Section IV.

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II. THE ANALYTICAL MODEL OF POTENTIAL AND THRESHOLD VOLTAGE FOR FINFET

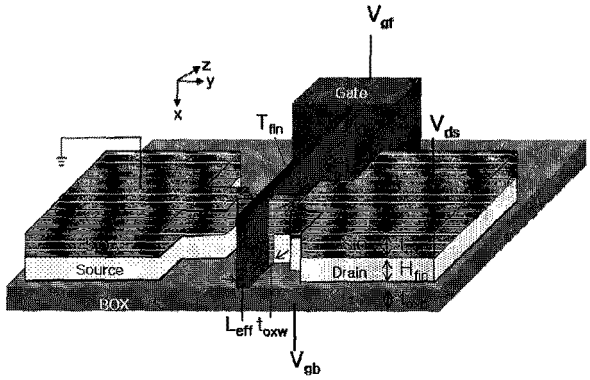

Fig. 1. Three dimensional view of FinFET with the notations described device parameters.

Fig. 1 is overview along the width, length and height direction of FinFET. The T_{fin} is width of channel and H_{fin} is height of channel, and t_{oxf}, t_{oxw} and t_{oxb} are oxide thickness of front, side and back gate respectively. The V_{gf} and V_{gb} are front and back gate bias. The L_{eff} is effective gate length and V_{ds} is source-drain voltage. Note the FinFETs have three gates of front, side and back direction even though front and side gate is equi-potential and the potential of width direction is symmetrical. Using the 3D Poisson's equation, the potential distributions in channel electrostatics are three dimensionally obtained under threshold and subthreshold bias condition with inversion charge term $n = n_i e^{q(\varphi-\varphi_F)/kT}$ where n_i is intrinsic electron density in silicon and φ_F is the nonequilibrium quasi-Fermi level as follows.

$$\nabla^2\varphi(x,y,z) = \frac{qn}{\varepsilon_{Si}} \tag{1}$$

Since the current is small in the subthreshold region, the Poisson's equation alone is sufficient. The boundary conditions referred to reference [3] are required to solve 3D Poisson's equation. In order to solve the Poisson's equation separation into 1D Poisson's equation and 2D and 3D is needed. The complete solution of Poisson's equation is the summation of 1D solution , φ_{1D}, 2D solution, φ_{2D} and 3D solution, φ_{3D}. The 1D solution is the potential distribution along the channel height, and the potential distribution φ_{1D} in the channel height can be expressed as

$$\varphi_{1D} = \varphi_{sb} + E_{sb}(H_{fin} - x) + \frac{q}{2\varepsilon_{Si}} N_A (H_{fin} - x)^2 \tag{2}$$

Since the 2D solutions is the potential distributions surrounded with the channel height and length, the potential distribution φ_{2D} is as follows.

$$\varphi_{2D} = \sum_{r=1}^{\infty} \frac{1}{\sinh(\gamma_r L_{eff})} [V'_r \sinh(\gamma_r y) + V_r \sinh(\gamma_r (L_{eff} - y))] \times [\sin(\gamma_r x) + \frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{oxf} \gamma_r \cos(\gamma_r x)] \tag{3}$$

Also the 3D solution is the potential distributions including channel width effects and can express such as the following equation.

$$\varphi_{3D} = \sum_{s=1}^{\infty}\sum_{r=1}^{\infty} P_{sr} [\sinh\{\chi_{sr}(T_{fin} - z)\} + \sinh(\chi_{sr} z)] \times \frac{\sin(\alpha_s (y - L_{eff}))}{\cos(\alpha_s L_{eff})} [\sin(\beta_r x) + \frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{oxf} \beta_r \cos(\beta_r x)] \tag{4}$$

To obtain the total potential distributions, summation of 1D solution , φ_{1D}, 2D solution, φ_{2D} and 3D solution, φ_{3D} is summed.

$$\varphi(x,y,z) = \varphi_{1D} + \varphi_{2D} + \varphi_{3D} \tag{5}$$

In the above equations, N_A is the doping concentration in the channel and the varibles related with dimension and material such as $\varphi_{sb}, E_{sb}, \gamma_r, P_{sr}, \chi_{sr}, \alpha_s, \beta_r$ refer to [3].

To calculate subthreshold current, we need to divide into two zone of front gate region and back gate region. The current for front gate and for back gate are able to be derived from $x_{\min}$ having the minimum potential along to height direction. The current for front gate is current of region from 0 to $x_{\min}$, and the current for back gate is current of region from $x_{\min}$ to H_{fin}. This model is verified, and the threshold voltage and DIBL are calculated using our potential model and current analytical model for different values of back gate bias and source/drain bias in Section III

III. RESULTS OF POTENTIAL AND THRESHOLD VOLTAGE

Fig. 2 shows the potential distributions calculated by this model. To verify this model, the results of this model are compared with those of 3D numerical simulation[9]. As well known in Fig. 2, these results agree with those of 3D numerical simulation. As above mentions, the potentials of z-direction is symmetrical due to structure of

FinFET. As shown in the potential along the channel length, the variations of potential in the drain region is higher than those in the source region. The variations of potential along the channel height is nearly constant since the backgate bias is zero.

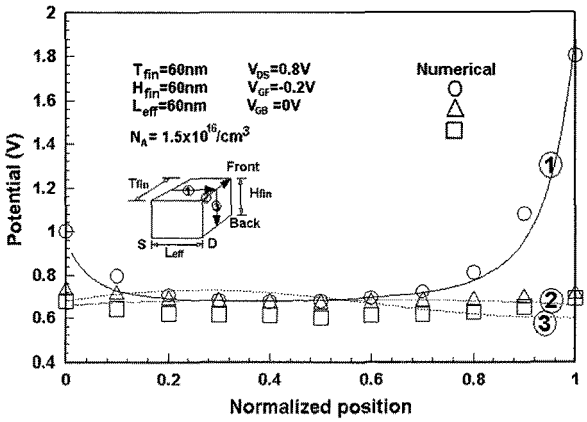

Fig. 2. Potential distribution of FinFET along the channel length ①, along the channel width ② and the channel height ③.

Fig. 3 shows the 3D potential distributions on the surface of the channel. As mentioned in Fig. 2, the potential distribution of z-direction is symmetrical regardless of channel height due to gate structure of FinFET. As known in the potential distribution of x-y surface, the influence on drain bias is bigger at the top gate than at the back gate. Also the potential is increased at the drain region of the x-z surface due to drain bias. Using 3D analytical potential model, subthreshold current is derived from the potential distributions according to the variation of back and source/drain bias.

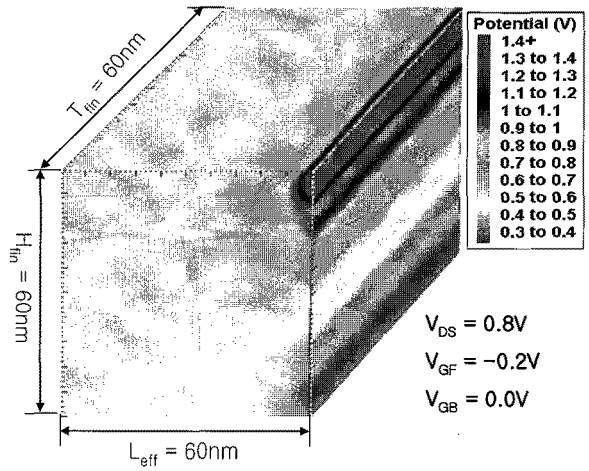

Fig. 3. Potential distribution of FinFET on the surface of the channel.

Fig. 4 shows the variations of the threshold voltage according to the change of back gate bias. The threshold voltages decrease with the increase of backgate bias due to the decrease of subthreshold current. The threshold voltages also decrease with the decrease of gate length due to the short channel effect. Note that the increase of the backgate bias decreases the subthreshold current. Therefore the backgate bias influences on the value of threshold voltage. To design the threshold voltage, we have to use the optimum back gate bias.

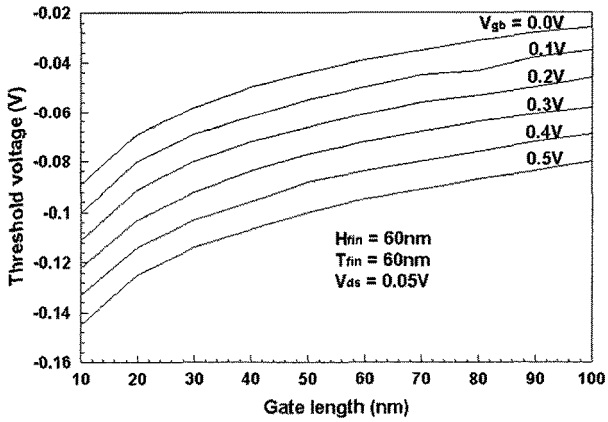

Fig. 4. The threshold voltage distribution of FinFET along the channel length according to the change of the backgate bias.

Fig. 5 shows the threshold voltage distribution of FinFET along the channel length according to the change of drain bias and H_{fin}. The threshold voltages decrease with the decrease of gate length due to the short channel effect. Since the increase of the drain bias exhibits pronounced short channel effects and very high off current, the absolute value of threshold voltage increase. We have, therefore, to use very thin gate oxide to solve this problem, but the ultra thin oxide leaks a very high input current.

Fig. 6 shows The threshold voltage distribution of FinFET along the channel width according to the change of drain. The threshold voltages increases with the decrease of channel height due to the short channel effect. Since the increase of the drain bias exhibits pronounced short channel effects and very high off current, the absolute value of threshold voltage increase as shown in Fig. 5 and Fig. 6. As mensioned before, the very thin gate oxide has to use in fabricating FinFET to solve this problem even though the ultra thin oxide leaks a very high input current.

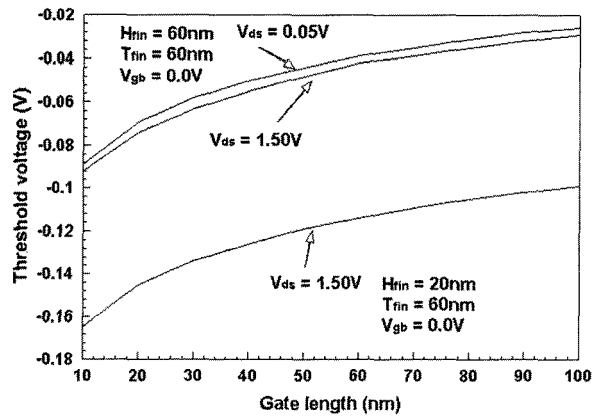

Fig. 5. The threshold voltage distribution of FinFET along the channel length according to the change of drain bias and the channel height.

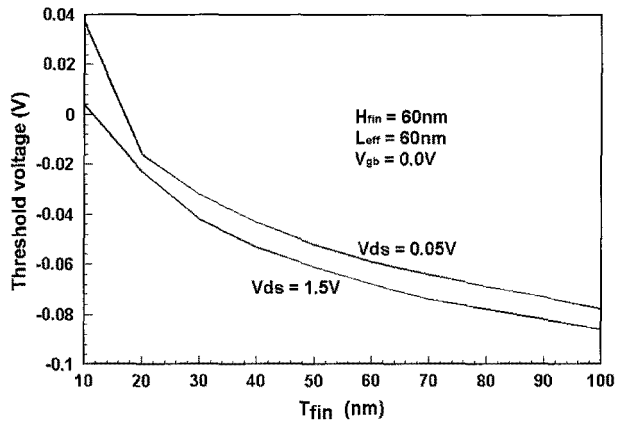

Fig. 6. The threshold voltage distribution of FinFET along the channel width according to the change of drain.

Fig. 7 shows the DIBL along the channel length according to the change of front gate oxide thickness. The DIBL is the threshold voltage dependence on drain bias. The variation of threshold voltage is investigated when the drain voltage is changed from 0V to 1V. As expected in the short channel effects, the DIBL is increased and the rate of increase is large in short channel. Since the most important oxide for device performance is the front gate oxide in the FinFET having three side oxide, the threshold voltage dependence on the front gate oxide thickness is investigated. The decrease of the front gate oxide thickness increases DIBL effects, and decrease in channel length also increases DIBL due to the short channel effects. The variation rate of DIBL according to gate length is large in the thin gate oxide, and the DIBL is above 100mV/V in the range of the channel length of 40nm below for $t_{oxf} = 20$ nm. Since the DIBL of above 100mV/V is generally inapplicable in digital application, the optimum front gate oxide thickness is needed for digital IC.

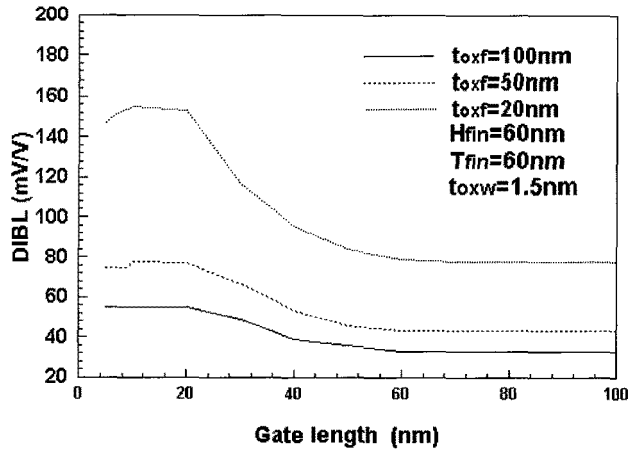

Fig. 7. The DIBL of FinFET along the channel length according to the change of front gate oxide thickness.

IV. CONCLUSIONS

This paper presents the dependence of the threshold voltage on back gate bias and drain voltage for FinFET which has three gates such as the front gate, side and back gate. In this paper the variations of threshold voltage have been investigated into the analytical potential model derived from 3D Poisson's equation with the variation of the back gate bias and drain voltage. As known from the down scaling rules, this paper have presented the threshold voltage in the case that drain voltage is the 1.0V above, which is set as the maximum supply voltage. To show the variation of the threshold voltage with drain voltage, this analytical potential model is used in this paper.

To verify this model, the results of this model are compared with those of 3D numerical simulation. These results agree well with those of 3D numerical simulation.

The potential distribution along to channel width is symmetrical regardless of channel height due to gate structure of FinFET. The influence on drain bias is bigger at the top gate than at the back gate. Also the potential is increased at the drain region due to drain bias.

The threshold voltages decrease with the increase of backgate bias due to the decrease of subthreshold current. Since the increase of the drain bias exhibits pronounced short channel effects and very high off current, the absolute value of threshold voltage increases. To investigate the threshold voltage dependence on drain bias, the DIBL is obtained from this model. The decrease of the front gate oxide thickness also increases DIBL effects, and decrease in channel length also increases DIBL due to the short channel effects.

This analysis for the threshold voltage of FinFET will be used in the design of IC based on FinFET.

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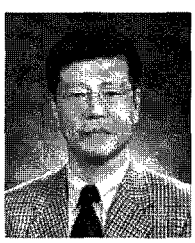

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Received the B.S. degree from Ajou University in 1983, the M.S. and Ph.D degrees from Yonsei University in 1985 and 1990, respectively, all in electronic engineering. In 1990, he joined Kunsan National University, Chonbuk, Korea, where he is current a Professor in the School of Electronic and Information Engineering. From 1994 to 1995, he held a research position with the Electronic Engineering Department, Osaka University, Osaka, Japan. From 2004 to 2005, he was with the School of Microelectronic Engineering, Griffith University, Nathan, QLD, Australia. His research interests include semiconductor device physics and device modeling with a strong emphasis on quantum transport and Monte Carlo simulation.