논문 2010-47SD-3-1

양자가둠 효과를 포함한 Saddle MOSFET에서의 모서리효과의 분석과 억제방법

(Analysis and Suppression of the Corner Effect in a Saddle MOSFET Including Quantum Confinements Effects)

셰 드*, 김 희 상*, 라 흐 만*, 이 종 호**, 박 병 국**, 신 형 철**

(Syed Atif Pervez, Heesang Kim, Atteq-Ur-Rehman, Jong-Ho Lee, Byung-Gook Park, and Hyungcheol Shin)

요 약

Saddle MOSFET의 모서리의 효과에 대한 고전역학과 양자역학적 시뮬레이션의 비교분석을 3차원 수치 시뮬레이터를 사용하여 수행하였다. 비교분석 결과 양자역학적 시뮬레이션에서는 실리콘 핀의 단면에서의 정확한 최대 전자 밀도의 위치와 크기를 제공함으로써 소자의 정확한 설명을 제공하는 것을 보여 주었고, 이를 이용하여 모서리 효과 및 그것이 소자의 문턱전압의 특성을 미치는 영향의 정확한 분석이 실행되었다. 또한, 모서리 효과를 억제하기 위해서 실리콘 핀의 모서리를 둥글게 하거나 구석의 바디도핑을 낮추는 두 가지 가능한 기법을 제시했다.

Abstract

A comparative analysis of quantum-mechanical and classical simulation regarding corner effect in a Saddle MOSFET has been carried out using a 3-D numerical simulator. The comparison has shown that quantum simulation gives correct description of device by providing accurate peak E-density position and magnitude at the Si-fin cross-section, hence accurate analysis of corner effect and its impact on device threshold voltage (Vth) characteristics is carried out. Moreover, rounding the Si-fin corners or lowering the body doping have been shown as two possible techniques to suppress the undesirable corner effect.

Keywords : Corner effect, Quantum-mechanical, Saddle MOSFET, Si-fin

I. Introduction

Saddle MOSFET (S-MOSFET), a device with a recess channel having tri-gate controllability over the channel, shows improved characteristics in controlling short channel effects and higher drive current compared with conventional recessed channel devices [1]. The S-MOSFET combines the merits of both a recess channel device and a multiple gate device in one structure. However, having a tri-gate at the bottom portion of the channel can give rise to the parasitic corner effect at the fin of the device. Due to the gate coupling at the top and side of the corners, carriers flow through the corners instead of the center resulting in the formation of independent channels located at different positions in Si-fin[2~3]. These channels are activated at different gate voltages. In other words, we can say that some part of the channel (corners) will turn on earlier than the rest of the channel and thus can result in unstable

* 학생회원, ** 평생회원, 서울대학교 전기컴퓨터공학부
(School of Electrical Engineering and Computer Science, Seoul National University)

※ 본 연구는 Inter-university Semiconductor Research Center (ISRC), Hynix Seimiconductor Inc.의 지원에 의하여 수행되었습니다.

접수일자: 2009년12월4일, 수정완료일: 2010년3월2일

V_{th} characteristics.

In this work, we have carried out an analysis of the corner effect at the tri-gated Si-fin of a S-MOSFET, through quantum and classical simulations. We have shown that as the device size is shrunk to below 50-nm range, quantum confinement effects become crucial for accurate results, and thus should be included in the simulations. We have also studied impact of the presence of sharp corners on the device V_{th} characteristics and based on the results possible solutions are proposed.

Ⅱ. Device Structure and Simulations

Both classical and quantum simulations have been performed on Sentaurus, a drift-diffusion based 3-D device simulator[4]. Device is designed using Sentaurus Process Emulator. For quantum simulations 2-D Poisson-Schrödinger have been solved using Modified Local Density Approximation (MLDA) model. MLDA model[5~6] calculates the confined electron-density (E-density) at some distance from the Si-SiO_2 interface, denoted by 'x' in equation 1. Under boltzmann statistics the equation for E-density is given as follows

$$n(x) = N_C \exp\left[(E_{fn} - E_C)/K_B T\right]\left[1 - \exp\left(-X^2/\lambda_{th}^2\right)\right] \quad (1)$$

Where, $\lambda_{th} = \left(\hbar^2/2mK_B T\right)^{1/2}$

N_C, E_{fn} and E_C are conduction band density of states, Fermi energy and conduction band edge respectively. λ_{th} is the electron thermal wavelength. m is effective mass, ħ is reduced Plank constant. K is Boltzmann constant and T is carrier temperature. Fig. 1(a) shows the 3-D schematic view of the S-MOSFET while Fig. 1(b) shows its cross sectional view across the silicon body. The tri-gated poly-Si gates covers only the bottom porion of the channel. Width of Si-fin and its portion overlapped by poly-gate is shown as W_{fin}=44 nm and H_{fin}=50 nm, respectively. The gate length (L_g) is 44 nm; gate

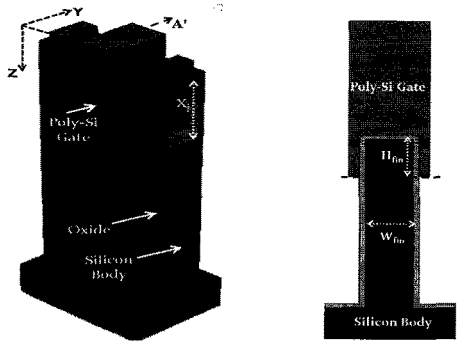

그림 1. S-MOSFET 소자의 개략도 (a) 조관도 (b) A-A' 방향 단면도

Fig. 1. Schematic view of the S-MOSFET device.
(a) bird's eye view
(b) cross sectional view along A-A'

oxide thickness (t_{ox}) is 5.7 nm; recess depth is 120 nm. Different values of uniform body doping (N_a) ranging from 4×1017cm-3 to 5×1018cm-3 are used, depending upon the requirement of the situation.

Ⅲ. Results and Discussion

1. Comparison of Quantum and Classical Simulation

Fig. 2. shows an analysis of corner effect in an S-MOSFET with varying gate bias. ncorner and ncenter represent E-density at corners and center of the channel, respectively, and their ratio indicates the intensity of the corner effect. From the figure it is

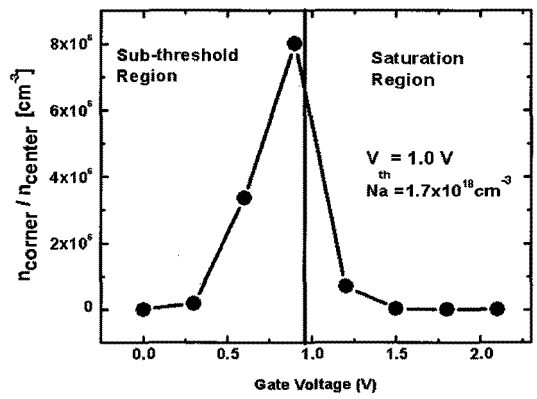

그림 2. 게이트 전압 변화에 따른 전자 농도에 대한 모서리 효과

Fig. 2. Corner effect regarding electron concentration with variation of the gate bias.

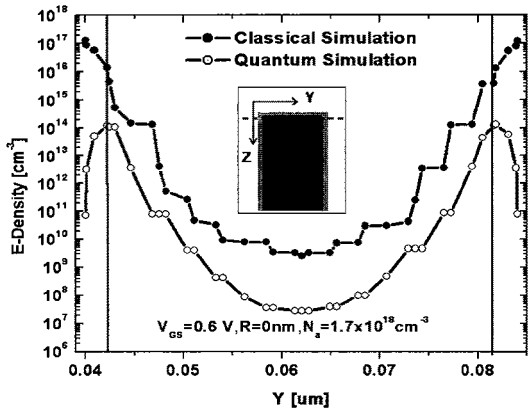

그림 3. S-fin 단면의 표면에서 고전적 그리고 양자적인 전자농도 분포

Fig. 3. Classical and quantum E-density distribution at top surface of the Si-fin cross-section.

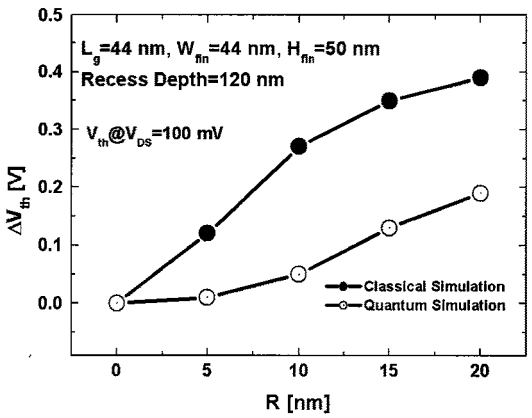

그림 4. 모서리 곡률(R) 변화에 따른 고전적 그리고 양자적 시뮬레이션에서의 문턱전압의 변화

Fig. 4. Change in threshold voltage (ΔV_{th}) with varying R for both classical and quantum simulation.

clear that corner effect is more prominent in sub-threshold region and corners have the highest E-density ratio just below V_{th}. Thus, on this stage, the device operation is fully dependent on the corners. However, at $V_{GS} \geq V_{th}$, there is a sharp decrease in the corner effect showing transitions from the corner-dominated to the sidewall-dominated regime of operation. With further increase of the gate bias, the device reaches homeogenous sidewall E-density and corner effect disappears, as shown in the figure.

Figure 3 shows a comparison of classical and quantum E-density distributions at top surface of Si-fin cross-section (inset of Fig. 3). From the figure it is clear that in case of quantum simulations, the maxima of E-density does not lie at the interface but

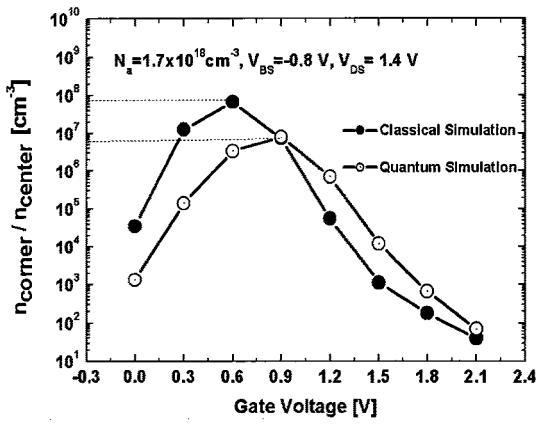

그림 5. 양자적 그리고 고전적 시뮬레이션에 대한 모서리 효과의 비교. 양자의 경의 모서리 효과가 경우 10배 정도 크다.

Fig. 5. A comparison of corner effect for quantum and classical simulation. Corner effect is one order of magnitude higher in quantum case.

at a certain distance (purple lines) and three order magnitude smaller than the classical simulations. Hence classical simulation not only overestimates E-density but also shows wrong position of its maxima and thus fails to provide accurate description of the device.

Figure 4 shows a comparative analysis of change in threshold voltage (ΔV_{th}) with variation in corner rounding (R). Classical simulation shows much higher ΔV_{th} than quantum simulation. This is due to the fact that E-density is largely concentrated in the corners in classical simulation. Thus change in R will largely affect the V_{th} . However, this is not the case in quantum simulation as shown in the figure.

As classical simulation overestimates E-density in the corners, corner effect can also be expected to be higher. This is shown in Figure 5, where corner effect in classical simulation is one order of magnitude higher than quantum simulation.

2. Suppression of Corner Effect

In section 3.1 we concluded that quantum simulation must be used for correct description of the device physics. Hence in this section, we include quantum confinement effects in the simulations and based on the results propose two different solutions for the suppression of corner effects.

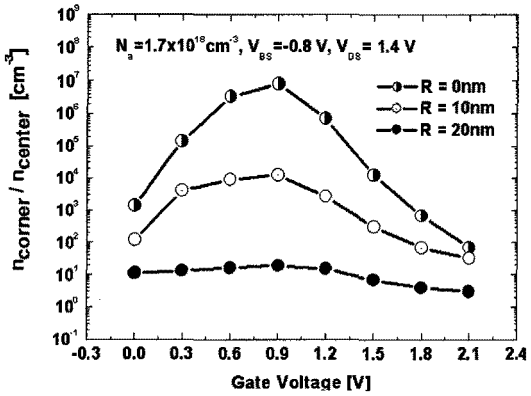

그림 6. 모서리 효과에 대한 Fin 곡률의 효과. 큰 모서리 곡률은 모서리 효과를 억제한다.

Fig. 6. Effect of fin rounding on the corner effect. Larger R suppresses the corner effect.

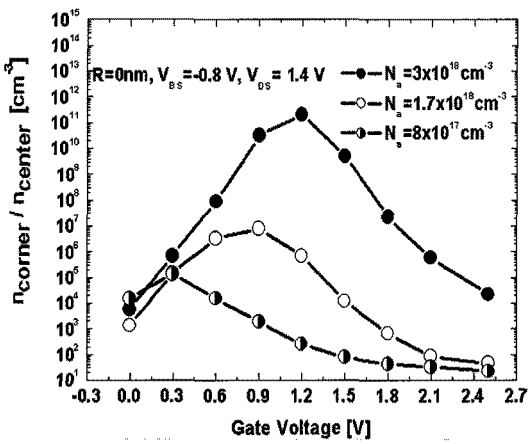

그림 7. 다른 바디도핑 조건을 가지는 소자에서의 모서리 효과. 바디도핑이 증가할수록 모서리 효과는 더 두드러진다.

Fig. 7. Corner effect at devices with different body doping conditions. The corner effect becomes more prominent as body doping increases.

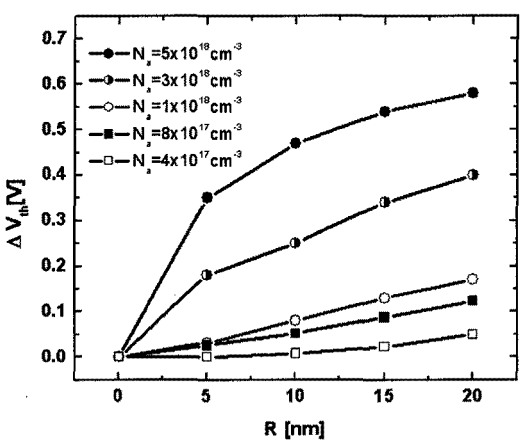

그림 8. 다른 N_a 값에 대한 R대 ΔV_{th}. N_a값이 노을수록 ΔV_{th}가 커진다.

Fig. 8. ΔV_{th} vs R for different values of N_a. At higher value of N_a, ΔV_{th} is larger and vice versa.

Figure 6 shows an approach by rounding the fin corners and consequently suppression of the corner effect. In rounded Si-fin corners, gate has more efficient control over the channel carriers, hence E-density along the Si-fin becomes uniform.

Another technique which can also suppress corner effect is to use lower body doping. This is shown in Fig. 7. At constant R=0 nm, higher N_a will bring higher corner effect and vice versa. Also, since at higher Na the electron concentration at the corners will be much higher, hence rounding the corner will bring larger change in V_{th}. This relationship between ΔV_{th} and R at increasing value of N_a is shown in figure 8. Three different body doping are considered and in each case R is increased from 0 to 20 nm and ΔV_{th} is observed. Analysis shows that at higher value of N_a, the change in threshold voltage of the device is much greater in comparison to the case when lower body doping is used. Hence we can conclude that using lower body doping will suppress corner effect and consequently smaller ΔV_{th}. Variation in N_a, however, will vary V_{th} of the device, and thus the V_{th} stability should be ensured through metal gate work-function engineering.

IV. Conclusion

An accurate analysis of the corner effect in a Saddle MOSFET has been carried out by considering quantum confinement effects in the device. In comparison to classical simulations, quantum simulations have been shown to give correct description of device by providing accurate peak E-density position and magnitude, thus accurate description of corner effect and its impact on device Vth characteristics. Effective techniques like rounding Si-fin corners or lowering the body doping, have also been shown to suppress the undesirable corner effect.

References (참 고 문 헌)

[1] S.W. Chung, S.D. Lee, S.A. Jang, M.S. Yoo, K.O. Kim, C. O. Chung, S. Y. Cho, H.J. Cho,

L.H. Lee, S.H. Hwang, J.S. Kim, B.H. Lee, H. G. Yoon, H.S. Park, S.J. Baek, Y.S. Cho, N.J. Kwak, H.C. Sohn, S.C. Moon, K.D. Yoo, J.G. Jeong, J.W. Kim, S.J. Hong, and S.W. Park, "Highly scalable saddle-fin (S-Fin) transistor for sub 50 nm DRAM technology," in VLSI Symp. Tech. Dig.,pp.147 - 148, 2006.

[2] W. Xiong, J.W. Park and J.P. Colinge "Corner effect in multiple-gate SOI MOSFETs" SOI Conference, pp.111, 2003.

[3] B. Doyle, B. Boyanov, S. Datta, M. Doczy, S. Hareland , B. Jin, J. Kavalieros, T. Linton, R. Rios and R. Chau "Tri-gate fully depleted CMOS transistors: Fabrication, design and layout" VLSI Technology , pp.133, 2003.

[4] Sentaurus Device User Guide version A-2007.12, December 2007.

[5] G. Paasch and H. Übensee, "A Modified Local Density Approximation: Electron Density in Inversion Layers," Physica Status Solidi (b), vol. 113, no. 1, pp. 165 - 178, 1982.

[6] H¨ansch W., Vogelsang T. Kircher R., and Orlowski M. "Carrier transport near the Si/SiO2 interface of a MOSFET" Solid-State Electronics 32(10): pp. 839-849, 1989.

저 자 소 개

세 드(학생회원)
2006년 NWFP UET Peshawar Pakistan 학사 졸업.
2010년 서울대학교 전기공학부 석사 졸업
2006년~2008년 Electrical Lab. Engineer Ghulan Ishaq Khan Institute Swabi Parkistan.
<주관심분야 : Nano CMOS>

김 희 상(학생회원)
1995년 POSTECH 물리학과 학사 졸업
1997년 POSTECH 전기전자 공학부 석사 졸업
2008년~현재 서울대학교 전기공학부 박사 과정 재학.
1997년~2007년 Hynix Semiconductor.
<주관심분야 : CMOS device characterization and modeling>

라 흐 만(학생회원)
2006년 NWFP UET Peshawar Prkistan 학사 졸업.
2010년 서울대학교 전기공학부 석사 졸업.
<주관심분야 : Process Integration>

신 형 철(평생회원)
1985년 서울대학교 전기공학부 학사 졸업.
1987년 서울대학교 전기공학부 석사 졸업.
1993년 미국 UC Berkeley 전자공학과 박사 졸업.
1994년~1996년 Motorola
1996년~2003년 한국과학기술원 교수.
2001년~2002년 Berkana Wireless.
2003년~현재 서울대학교 교수.
<주관심분야 : Flash Memory, Nano CMOS, CMOS RF, DRAM>

이 종 호(평생회원)
1987년 경북대학교 전자공학과 학사 졸업.
1989년 서울대학교 전기공학부 석사 졸업.
1993년 서울대학교 전기공학부 박사 졸업.
1994년~2002년 원광대학교 부교수.
2002년~2009년 경국대학교 교수.
2009년~현재 서울대학교 교수.
<주관심분야 : 3차원 나노 CMOS, 나노 CMOS 제작 및 모델링, 3-D 웨이퍼 본딩>

박 병 국(평생회원)
1982년 서울대학교 전기공학부 학사 졸업.
1984년 서울대학교 전기공학부 석사 졸업.
1990년 미국 Stanford Electrical Engineering 박사 졸업.
1990년~1993년 AT&T Bell Lab..
1993년~1994년 Texas Instrument.
1994년~현재 서울대학교 교수
2008년~현재 서울대학교 반도체공동연구소 소장
<주관심분야 : The design and fabrication of nanoscale CMOS, flash memories, silicon quantum devices and organic thin film transistors>