특집

Design and Characteristics of Modern Power MOSFETs for Integrated Circuits

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I. Introduction

Recently, 0.18-μm high voltage technology (HV18) 13.5V (operating voltage) high voltage well-based symmetric EDMOSTs (Extended Drain Metal Oxide Semiconductor Transisotrs) have been fabricated together with low-voltage logic and medium-voltage MOSFETs for display driver ICs. Although most of high voltage devices[1] have STI (Shallow Trench Isolation), the HV18 technology implements MTI (Medium Trench Isolation) of a depth of 1 μm to reduce the chip size while maintaining an acceptable isolation breakdown voltage between two adjacent devices.

An asymmetric NMOSFET for low-voltage applications was proposed for improving device performance and short-channel immunity in [2]. In this paper, characteristics of asymmetric high voltage well-based EDNMOS and EDPMOS are explored, using TCAD simulation, and compared with symmetric EDMOSTs. The asymmetric EDMOS proves to have better performance, short-channel immunity and size than the symmetric one. Well-designed asymmetric EDMOS can be an excellent candidate for future low-power display driver in a smaller chip.

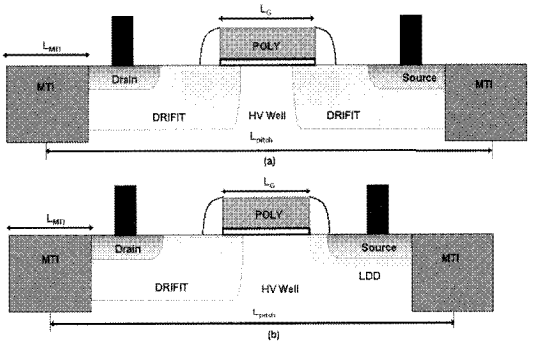
Modern power integrated circuit has high-voltage/power devices such as EDMOS and LDMOS integrated with low-voltage logic devices on a single chip. The integration of high and low voltage devices has made the process costly and complex. High-voltage/power MOSFETs need high voltage well/drift implant and additional high-temperature long-time thermal process. Recently, power DMOSTs have been implemented in CMOS logic technology[3-5]. In this paper, we propose an improved logic well-based n-channel EDMOS integrated in 0.18-μm CMOS logic technology for high-performance (large

drive current) low-power (small off-current) BVDSS = 15V ~ 20V applications, including mobile mixed-signal products, etc. Unlike ordinary EDMOSTs[4], our EDMOSTs have low-voltage logic wells and need neither high-voltage well/drift implant nor additional high-temperature long-time thermal process. Compared to the conventional EDMOS[3], the overlap zone of p- and n-wells of our improved logic well-based EDMOS provides an additional device design variable. The improved logic well-based nEDMOS has advantages over the conventional one in terms of the drive current, sensitivity of drain saturation current to drain bias, off-current and breakdown voltage, and also has much better figure-of-merit R_{sp} / BVDSS[6] than the conventional one at a short length of the n-well drift region.

II. Device Structures

1. High Voltage Well-Based EDMOS

HV18 13.5V symmetric and asymmetric EDMOS structures are shown in <Fig. 1> Replacing the high-resistance drift region on the source side of the symmetric EDMOS with the low-resistance logic LDD (Lightly-Doped Drain), we can increase I_{Dsat}, reduce the pitch size (L_{pitch}), specific on-resistance and improve short channel



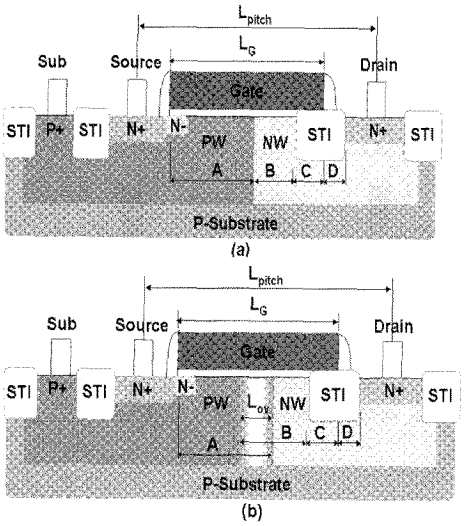
<Fig. 1> Cross-sectional views of (a) symmetric and (b) asymmetric EDMOSTs

immunity.

The gate length L_G = 1.5-μm symmetric EDNMOS and EDPMOS were fabricated, using 0.18-μm high voltage MTI technology. The MTI is 0.6 μm long and 1.0 μm deep. The MTI is filled with oxide and liner nitride. The physical gate oxide thickness is 330 Å. The oxide was formed through the processes of oxide deposition, anneal and low-voltage MOS oxidation. Elimination of high-voltage oxidation process step can prevent boron dopant loss and phosphorus dopant pile-up at the channel surface of EDNMOS, and lead to the increase of BVDSS and the effective channel length.

2. Low Voltage Logic Well-Based EDMOS

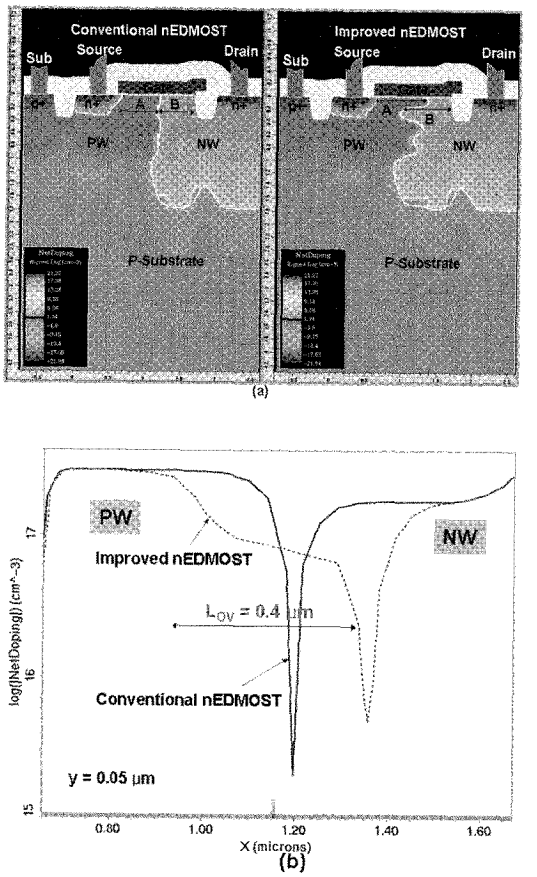
The cross-sectional views of the conventional and improved logic well-based EDMOSTs with RESURF STI are shown in <Fig. 2> Note that, unlike the conventional EDMOS in [3], our conventional EDMOS



〈Fig. 2〉 Cross-sectional views of (a) conventional and (b) improved nEDMOSTs

has RESURF STI beside the drain region.

The nEDMOSTs were simulated and fabricated, using 0.18-μm CMOS logic technology. The parameters A, B, C and D are device design variables. L_{pitch} = 1.98 μm, L_G =1.25 μm, G_{ox} (gate oxide thickness) = 125 Å, W_D (gate width) = 10 μm, and C = D = 0.15 μm are fixed for all simulations. The parameters A and B are the lengths of mask windows prepared before implanting impurity ions of the logic p- and n-wells, respectively. The conventional EDMOS has A = 0.6 μm and B = 0.5 μm, and the improved one A = 0.8 μm, B = 0.7 μm and L_{ov} = 0.4 μm. L_{ov} is the length of overlap area at which the p- and n-wells overlap each other. 〈Fig. 3〉 shows the simulated 2D and 1D net doping profiles of the nEDMOSTs. The net doping concentration in the overlap zone of the improved EDMOS is lower than that of the adjacent p- or n-well due to the doping compensation.

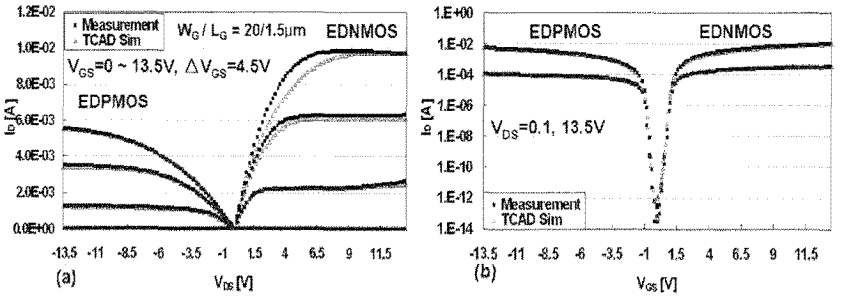


〈Fig. 3〉 Simulated (a) 2D and (b) 1D net doping profiles of conventional and improved nEDMOSTs

III. Electrical Characteristics and TCAD Simulation

1. High Voltage Well-Based EDMOS

〈Fig. 4〉 shows measured I_D-V_{DS} and I_D-V_{GS} characteristics of HV18 13.5V

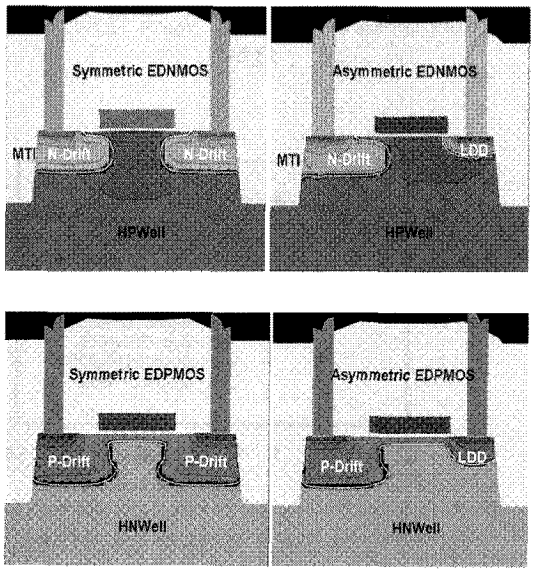


〈Fig. 4〉 (a) Output and (b) subthreshold characteristics of HV18 13.5V symmetric EDMOS

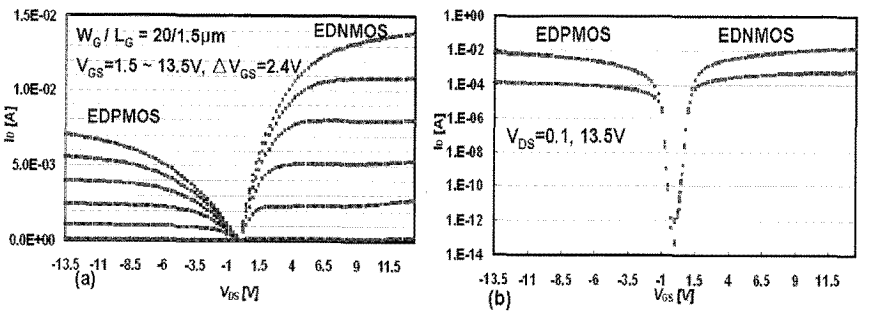
symmetric EDMOS, which are in good agreement with TCAD simulation results. Synopsys TSUPREM4 and MEDICI model parameters were calibrated to fit the simulated I-V curves to the measured data. In particular, to simulate the self heating at the saturation region of the high voltage EDNMOS, the heat equation model was used.

〈Fig. 5〉 shows simulated 2-D net doping profiles and junction boundaries of EDMOSTs.

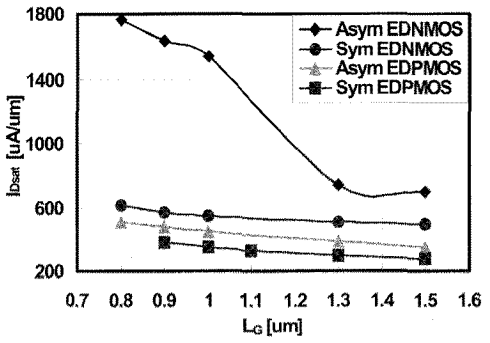
Using the same model parameters calibrated for the symmetric EDMOS, the I-V characteristics of the asymmetric EDMOS were simulated with reasonable confidence, and the simulation results are shown in 〈Fig. 6〉. 〈Figs. 7-12〉 show that the asym-



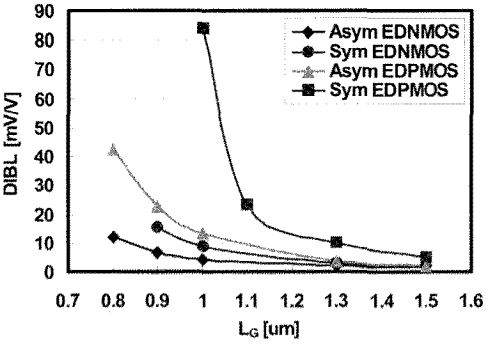
〈Fig. 5〉 Simulated net-doping profiles of (a) EDNMOS and (b) EDPMOS. All the devices have n-type polysilicon gates.



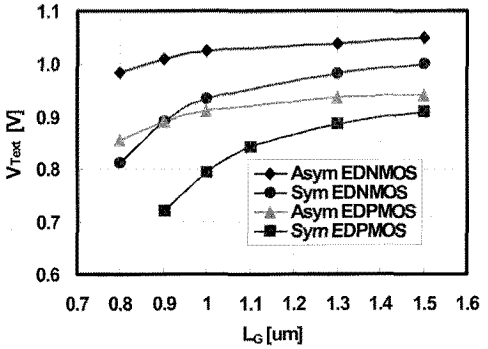
〈Fig. 6〉 Simulated (a) output and (b) subthreshold characteristics of HV18 13.5V asymmetric EDMOS



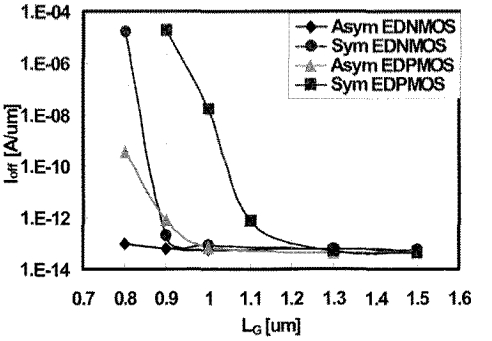
〈Fig. 7〉 Dependence of the drain saturation current on L_G of EDMOSTs. V_{GS} = 13.5V, V_{DS} = 13.5V



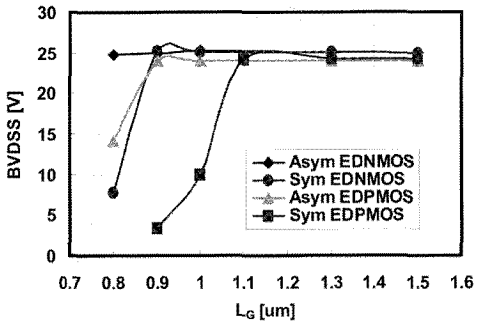
〈Fig. 8〉 Dependence of DIBL on L_G of EDMOSTs. DIBL≡$|V_{G1}(I_{D1}, V_{DS}=13.5) - V_{G2}(I_{D2}, V_{DS}=0.1)|$ / 13.4V, $I_{D1} = I_{D2} = 5\times10^{-10}$ [A/um]



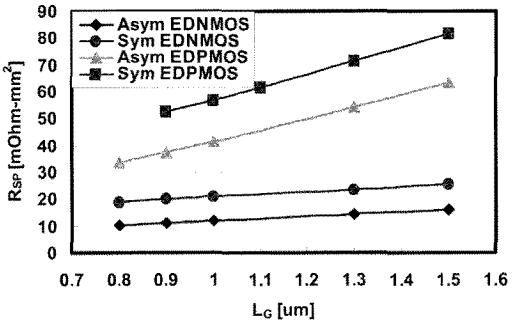
〈Fig. 9〉 Dependence of the threshold voltage on L_G of EDMOSTs. V_{DS} = 0.1V



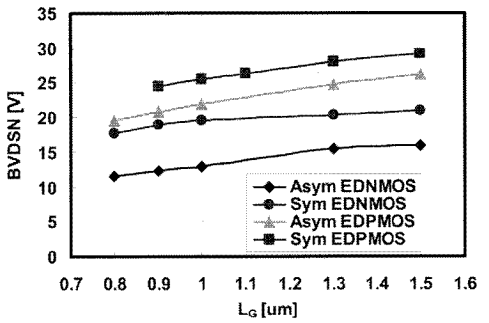
〈Fig. 10〉 Dependence of off-state current on L_G of EDMOSTs. V_{GS} = 0V, V_{DS} = 13.5V



〈Fig. 11〉 Dependence of the breakdown voltage on L_G of EDMOSTs. V_{GS} = 0V.



〈Fig. 12〉 Dependence of the specific on-resistance on L_G of EDMOSTs. V_{GS} = 13.5V, V_{DS} = 0.1V.

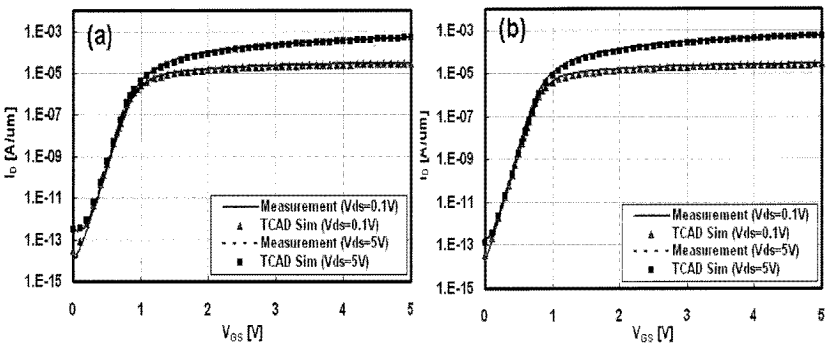


〈Fig. 13〉 Dependence of the snapback voltage on L_G of EDMOSTs. V_{GS} = 13.5V

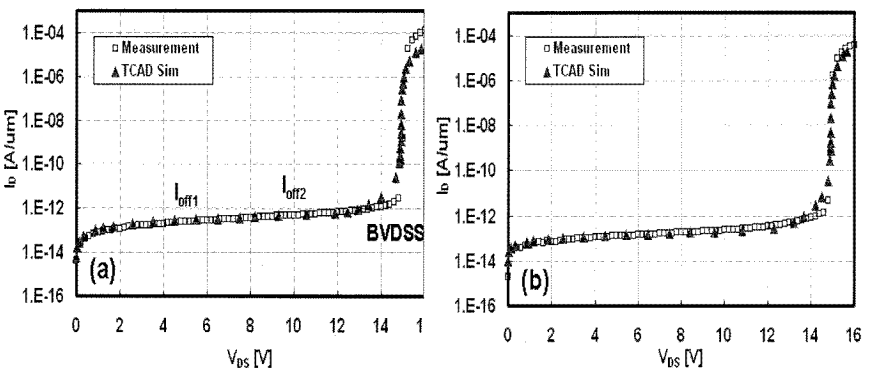
metric EDMOS has better performance, short-channel immunity and pitch size than the symmetric EDMOS. From 〈Figs. 11-12〉, we know that the figure-of-merit R_{sp} / BVDSS of the asymmetric EDMOS is better than the symmetric one. BVDSN of the asymmetric EDNMOS in 〈Fig. 13〉 can be improved by reducing the overlap between the gate polysilicon and the drift region at the expense of the device performance.

2. Low Voltage Logic Well-Based EDMOS

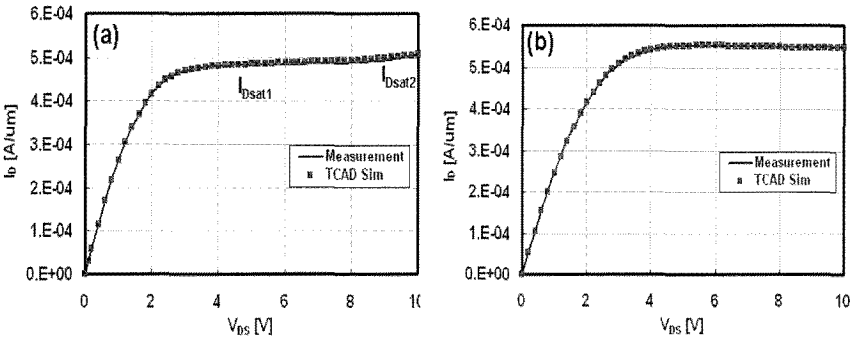
〈Figs. 14-16〉 show TCAD simulation results on I-V curves of the improved and



〈Fig. 14〉 Subthreshold characteristics of (a) conventional and (b) improved nEDMOSTs



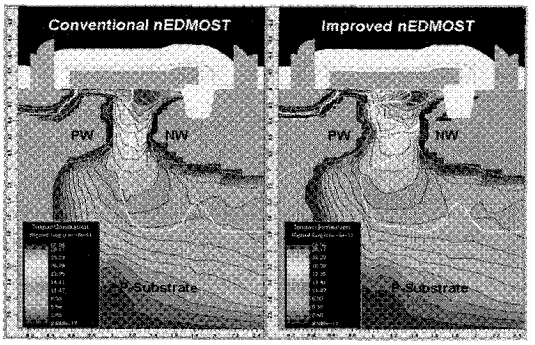
〈Fig. 15〉 I_D-V_{DS} curves at VGS = 0 V of (a) conventional and (b) improved nEDMOSTs



〈Fig. 16〉 I_D–V_{DS} curves at V_{GS} = 5 V of (a) conventional and (b) improved nEDMOSTs

conventional nEDMOSTs, which were verified against measurements. A few Synopsys TSUPREM4 and MEDICI model parameters were calibrated to fit the simulated I–V curves to the measured data. <Table 1> lists the electrical parameters of the improved and conventional nEDMOSTs. The snapback voltage (BVDSN) of the improved EDMOS is 22% higher than that of the conventional one, because the high impact ionization rate area of the improved nEDMOS stays away from the Si–SiO_2 interface while the high rate area of the conventional one close to the interface.

<Figs. 17–18> show the impact ionization rate and potential distributions at V_{GS} = 5 V

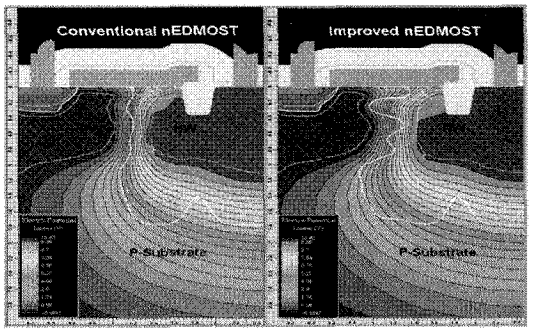


〈Fig. 17〉 Simulated 2D impact ionization rate distribution at V_{GS} = 5 V and V_{DS} = 10 V

and V_{DS} = 10 V, which are similar to those at the snapback voltages. R_{sp} = 7.45 [mΩ-mm^2] is comparable to the recently published ultra-low on-resistance of LDMOS[5]. The low R_{sp} values of our nEDMOSTs mainly result from the high doping level of

〈Table 1〉 Electrical parameters and bias conditions of the logic well-based improved and conventional nEDMOSTs

	V_{Text} [V] at V_{DS}=0.1V	R_{sp} [mΩ-mm^2] at V_{GS}=5V, V_{DS}=0.1V	I_{Dsat1} [uA/um] at V_{GS}=5V, V_{DS}=5V	I_{Dsat2} [uA/um] at V_{GS}=5V, V_{DS}=10V	BVDSS [V] at V_{GS}=0V, I_D=1×10^{-9} [A/um]	BVDSN [V] at V_{GS}=5V, I_D=1.25× I_{Dsat1}	I_{off1} [A/um] at V_{GS}=0V, V_{DS}=5V	I_{off2} [A/um] at V_{GS}=0V, V_{DS}=10V
Improved	0.749	7.45	549	546	15.0	17.1	1.24×10^{-13}	2.36×10^{-13}
Conventional	0.829	6.70	484	506	15.0	15.0	2.45×10^{-13}	5.02×10^{-13}

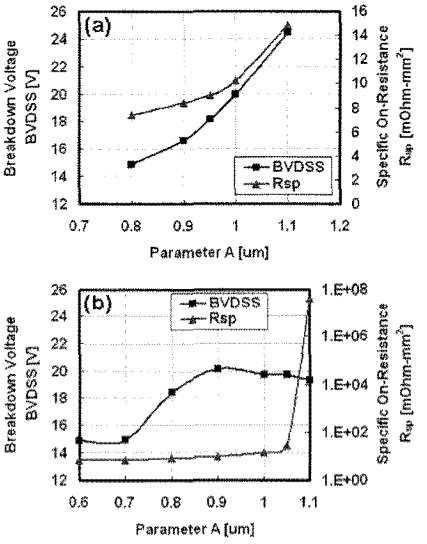


〈Fig. 18〉 Simulated 2D electric potential distribution at V_{GS} = 5 V and V_{DS} = 10 V

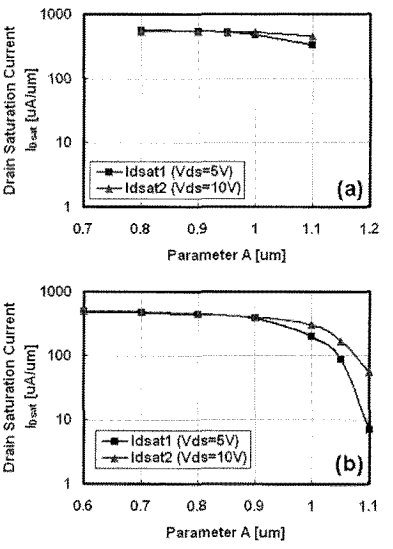
the logic n-well drift region.

The improved EDMOS has 7.91% ~ 13.4% larger drain saturation current, smaller variation of I_{Dsat} with V_{DS} than the conventional one, because the improved EDMOS has lower threshold voltage, shorter effective channel length, higher mobile electron concentration and lower net doping density due to the overlap zone. The off-current of the improved EDMOS is 49% ~ 53% smaller than that of the conventional one, because the net rate of Shockley-Read-Hall electron-hole pair generation-recombination of the improved EDMOS is lower than the conventional one especially at the drift depletion region.

〈Fig. 19〉 shows that R_{sp} / BVDSS of the improved EDMOS is dramatically lower than that of the conventional one at the short length of the n-well drift region. I_{Dsat} roll-off of the improved EDMOS is much smaller than the conventional one as the n-well drift length becomes shorter as shown in 〈Fig. 20〉



〈Fig. 19〉 Simulated variations of BVDSS and R_{sp} with the parameter A of (a) improved EDMOS with B = 0.7 μm and L_{pitch} = 1.98 μm, and (b) conventional EDMOS with B = 1.1 μm - A and L_{pitch} = 1.98 μm



〈Fig. 20〉 Simulated variations of I_{Dsat} with the parameter A of (a) improved EDMOS with B = 0.7 μm and L_{pitch} = 1.98 μm, and (b) conventional EDMOS with B = 1.1 μm - A and L_{pitch} = 1.98 μm

IV. Summary

0.18-μm high voltage technology 13.5V high voltage well-based symmetric EDMOS isolated by MTI was designed and fabricated. Using calibrated process and device model parameters, the character-istics of the symmetric and asymmetric EDMOS have been simulated. The asym-metric EDMOS has higher performance, better R_{sp} / BVDSS figure-of-merit, short-channel immunity and smaller pitch size than the symmetric EDMOS. The asym-metric EDMOST is a good candidate for low-power and smaller source driver chips.

The low voltage logic well-based EDMOS process has advantages over high voltage well-based EDMOS in process cost by eliminating the process steps of high-volt-age well/drift implant, high-temperature long-time thermal steps, etc. The specific on-resistance of our well-designed logic well-based EDMOSTs is compatible with the smallest one published. TCAD simu-lation and measurement results show that the improved logic well-based nEDMOS has better electrical characteristics than those of the conventional one. The im-proved EDMOS proposed in this paper is an excellent candidate to be integrated with low voltage logic devices for high-per-formance low-power low-cost chips.

References

[1] H. Wang, et al., Proceedings of ISPSD, (2008), P.20-23.

[2] J. P. Kim, et al., IEEE Trans. Electron Dev., Vol.54, No.11, (2007), P.2969-2974.

[3] J. C. Mitros, et al., IEEE Trans. Electron Dev., Vol.48, No.8, (2001), P.1751-1755.

[4] V. W. Y. Ma, et al., IEEE Conf. on Electron Devices and Solid-State Circuits, (2003), P.301-304.

[5] K. Shirai, et al., Proceedings of ISPSD, (2009), P.77-79.

[6] T. Letavic, et al., Proceedings of ISPSD, (2008), P.60-63

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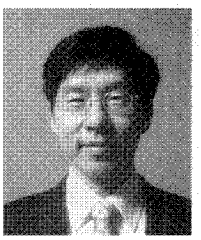

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