Effective Estimation Method of Routing Congestion at Floorplan Stage for 3D ICs

Byung-Gyu Ahn, Jaehwan Kim, Wenrui Li, and Jong-Wha Chong

Abstract—**Higher integrated density in 3D ICs also brings the difficulties of routing, which can cause the routing failure or re-design from beginning. Hence, precise congestion estimation at the early physical design stage such as floorplan is beneficial to reduce the total design time cost. In this paper, an effective estimation method of routing congestion is proposed for 3D ICs at floorplan stage. This method uses synthesized virtual signal nets, power/ground network and clock network to achieve the estimation. During the synthesis, the TSV location is also under consideration. The experiments indicate that our proposed method had small difference with the estimation result got at the post-placement stage. Furthermore, the comparison of congestion maps obtained with our method and global router demonstrates that our estimation method is able to predict the congestion hot spots accurately.**

Index Terms—**Congestion estimation, floorplan stage, 3D IC, EDA, VLSI**

I. INTRODUCTION

With the number of cells in a typical design growing exponentially and the electrical properties of metal wires scaling poorly, the competition for preferred routing resources between the various interconnects that must be routed is becoming more severe. The optimization of routing congestion has become a major concern in physical design due to over-congestion which will deteriorate circuit performance or even lead to an unroutable solution [1-2]. Recently, three-dimensional integrated circuits (3D ICs) are deemed to an attractive solution for reducing the chip area, total wirelength and interconnect delay. Unfortunately, routing congestion is still an unsolved problem. Accurate estimation to routing congestion in early stages conduces to reduce the occurrence ratio of over-congestion and re-design. .

Previous works on routing congestion estimation at the early stages of physical design have been proposed [2-4]. Most of them [2, 4] were implemented at placement stage; authors of [3] proposed a estimation method at floorplan stage. However, the computation of estimation at floorplan stage takes several to dozens of seconds while at placement stage it usually uses more than hundreds of seconds. What's more, none of them paid close attention to 3D ICs. Even through Cheng [5] proposed one model for 3D routing but which didn't concrete the process of synthesizing the various routing demand. Hence, multiple demands considered and accurate estimation method at floorplan stage is needed.

In this paper, an effective estimation methodology for 3D ICs is proposed using a model which takes the signal nets, power/ground network and clock network into consideration at floorplan stage.

The rest of the paper is organized as follows: Section II describes the estimation methodology and Section III presents experimental results. Finally, a conclusion is given in Section IV.

II. PROPOSED ESTIMATION METHOD

A conventional standard cell-based design contains the

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wires that implement power supply network, clock network and signal nets. All these wires share the same set of routing resources. At routing stage, the power supply network is created first and the clock network is routed next. Both of them are routed in specific metal layers. The signal nets are routed last and can only use the routing resources that have not been occupied by the power supply and clock wires. However, the residual routing resources in the metal layers which are occupied by the power and clock networks are still available for signal nets. Besides, at floorplan stage considering the three routing demands for different metal layers takes long runtime and has less significance. So in floorplan stage, we focus on the total routing demand of each grid cell instead of estimate various routing demand separately.

For 3D ICs, the routing congestion of each die is independent. Every die is divided into several rectangular grid cells, as shown in Fig. 1. Each grid only accommodates a finite number of routing wires, which depends on the industrial technology and the numbers of metal layers. Routing congestion can be defined as the proportion of the total routing demand and the wire track supply. The flow diagram of proposed method is described in Fig. 2.

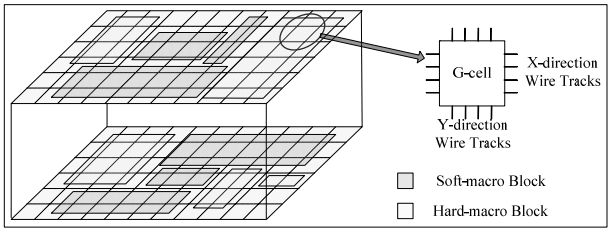


Fig. 1. Floorplan example and routing grids for a two-dies 3D IC.

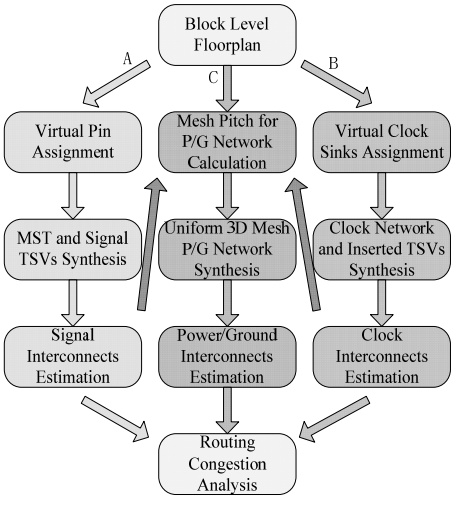


Fig. 2. Flow diagram for routing congestion analysis.

1. Signal Nets Estimation

As the direction A flow in Fig. 2, the signal nets estimation at the floorplan stage analyzes both inter-block and intra-block interconnects. Because there are no fixed pins for soft-macro blocks, the intersection-to-intersection method is used to estimate reasonably positions of the virtual I/O pins. For the two blocks located on the same die, we first draw a "fly-line" from the center of one block to another and then the nearest pin candidate from the fly-line is selected as a virtual pin. If the nearest pin candidate has already been selected for another virtual pin, the next closest pin is chosen. For the case of two blocks located on different dies, top view and projective profile are adopted. With top view, the projective profile of block is made from upper die to lower die. Then the intersection-to-intersection method can be used. Note that if overlapping occurs during projecting, the intersections of block bound and projective profile are selected as virtual pins.

After the virtual pin assignment, virtual routing is constructed based on the Minimum Steiner Tree. In 3D ICs, the length of TSVs is insignificant comparing with the length of signal nets. In other words, the effect of multilayer is ignored temporarily and pins are assumed on one die. It facilitates the generating the MST using classical algorithm. After the SMT generating, TSVs are needed for the nets which pins are located at different dies. So, signal TSVs are inserted and the best way to place the signal TSV is near the source pin [6]. As embedding TSVs, inter-die signal interconnections are divided into several segments on different dies. Coordinates of TSVs are regarded as the end points of the segments. Every segment only occupies the routing resource of the die it located. Therefore, segments should be calculated separately in order to get the routing demand for each die.

Rent's rule-based wire length distribution model and fan-out distribution model [7] are used to estimate the total wirelength of intra-block interconnection. The wire length per unit area can be considered as the routing demand. Therefore, the average routing demand of the

macro block i on X-direction is defined as

$$d_{avg}^{x}(i) = L_{total} \frac{W_i}{W_i + H_i} \frac{1}{W_G} \frac{1}{N_G^i} \quad (1)$$

where L_{total} is the intra-block total wirelength, W_i and H_i stand for the width and height of the macro block, W_G and N^i_G denote the weight of the g-cell and the number of g-cells the macro block includes respectively. The average routing demand of the macro block in Y-direction can be defined in the same way.

The final virtual signal nets estimation are used to synthesize the power/ground network.

2. Clock Network Estimation

The steps of clock network estimation are described as the direction B flow in Fig. 2. The clocks, which synchronize the sequential elements in the design, have strict signal integrity and skew requirements. So both the intra-block and inter-block interconnects are considered to meet the condition of zero skew.

At the floorplan stage, the locations of clock sinks in the soft-macro block are unknown. However, the number of clock sinks is known. The clock sinks are located by using an equal distribution within the block boundaries. After the virtual sinks assignment, H-tree model [8] is used to estimate the clock interconnect of intra-block. The Manhattan distance from the H-tree root to each sink is defined as intra-block-depth.

According to the initial clock topology generated by the H-tree model in the previous step, we apply the 3D-MMM/DME algorithm to estimate the inter-block clock network of 3D ICs. First, the roots of H-tree are regarded as a terminal set. 3D-MMM algorithm [9], which takes the upper bound for TSV count into account, is used to generate the inter-block abstract tree for 3D ICs. During this phase, clock TSV locations are decided. Then, the classic DME algorithm [10] is used to synthesize the virtual clock network. Note that the intra-block-depth needs to be considered in DME algorithm to achieve the zero skew.

After virtual clock network is generated, the routing demand is measured in the same way in Section II.1. The virtual clock network is also used for P/G network synthesis.

3. Power/Ground Network Estimation

The direction C flow as shown in Fig. 2 is the process of virtual P/G interconnection. The power supply network is designed accounting for several factors such as the current requirements of the design, acceptable bounds on the noise in the supply voltage, and electromigration constraints.

The uniform 3D mesh model [11] is used to synthesize the virtual P/G network. First, the total power consumption of each die is estimated by adding the power consumption of interconnects to the power consumption of blocks. Then, the value of the metal pitch of the power mesh for each die is determined by the analytical model proposed in [12]. It is assumed that the number of power pads is adequate, the positions of the power pads are fixed, and the metal width of the P/G network are set to max value of the design rule. For the die i, the analytical equation to determine the length of each mesh segment and the metal coverage to meet the IR-Drop constraint in the peripheral wire-bond system can be expressed as

$$m_i = \frac{16\delta V_{DD}^2 H}{P_{itot}\rho_w} \quad (2)$$

$$\%Cov = \frac{2m_i - 1}{m_i^2} \quad (3)$$

where m_i is the number of squares in the each mesh segment that denotes metal pitch, δ is the normalized IR-drop, V_{DD} is the voltage, H is the metal thickness, P_{itot} is the total power consumption and ρ_w is the metal resistivity. The metal pitch of die i equals m_i times of the metal width. Using the minimum value of m_i, the P/G network can be generated for each die. Then TSVs are used at each node of the P/G network to get the uniform 3D P/G mesh. Likewise, the same synthesizing method is valid for the ground network. Finally, the routing demand of P/G network is calculated.

4. Routing Congestion Analysis

After finishing the estimation of the signal net, clock and P/G network, routing congestion is performed at

each g-cell. Because of the strict signal integrity and skew requirements, the clock wires are typically shielded or spaced so that the signals on the neighboring wires do not distort the clock waveform; the shielding and spacing also consume some routing resources. So, the weight value for the clock network is set to three. Then the congestion for each grid can be estimated as

$$C_k = \frac{D_{signal} + 3 \cdot D_{clock} + D_{P/G}}{S_k} \quad (4)$$

where D_{singal}, D_{clock}, $D_{P/G}$ denote the routing demand number of each grid respectively, S_k is the number of wire track supply and C_k is the percentage to measure the congestion for g-cell k.

III. EXPERIMENTS

We mainly implemented our proposed estimation method in C++ and tested on Intel Pentium 4 2.8 GHz Linux machine. To evaluate the accuracy of the proposed routing congestion estimation method, simple two-dies ICs were used. The technology and setting parameters are shown in Table 1. Table 2 gives some detail information of the experimental chips. For these chips, routing congestion of each die was estimated respectively.

Table 1. Various technology and setting parameters used in our experiments

Item	Value
Number of dies	2
Bonding type	face-to-back
Si base layer thickness (μm)	50
Bonding layer thickness (μm)	10
Routing grid size (μm)	40
TSV diameter (μm)	40
TSV pitch (μm)	400

1. Comparison with Conventional Estimation Result at Post-placement Stage

In this experiment, both the proposed method at floorplan stage and conventional estimation method at post-placement stage were used. And we regarded the conventional post-placement estimation results as the normalized form because it could get similar result with really global routing. The post-placement estimation method used the three-step approach proposed by C. Sham in [2].

In order to evaluate the accuracy exactly, the numbers of g-cells for each routing congestion level were counted. The estimation results at post-placement stage were regarded as the base and the percentages of estimation results with the proposed method are calculated. We used the error ratios between the proposed method and conventional estimation method at post-placement stage to demonstrate the accuracy of the proposed method. According to the statistics, the error rates for different congestion levels were summarized in Table 3. It indicates that the proposed method had 15.8%~24.8% error ratios and on average the value was 18.8%.

Additionally, the routing congestion maps estimated at the floorplan stage and the post-placement stage were used to prove the similitude of estimation results. In Fig. 3, the congestion maps of one experimental chip, Industrial I in Table 2, are given. Since die1 is much more crowded than die2, we only present the congestion

Table 2. Parameters of experimental chips

Chip		Chip size (μm)	# of instances	# of nets	# of IOs	# of soft macro blocks	# of hard macro blocks	# of routing grids	# of metal layers
Industrial I	Die1	2560 x 2560	-	-	110	15	19	64 x 64	8
	Die2	2560 x 2560	-	-	-	21	18	64 x 64	8
	Total	-	127304	157196	110	36	37	-	-
Industrial II	Die1	3280 x 3280	-	-	195	22	24	82 x 82	8
	Die2	3280 x 3280	-	-	-	25	17	82 x 82	8
	Total	-	205193	231970	195	47	41	-	-
Industrial III	Die1	4000 x 4000	-	-	303	51	30	100 x 100	8
	Die2	4000 x 4000	-	-	-	46	32	100 x 100	8
	Total	-	282039	348226	303	97	62	-	-

Table 3. Difference between post-placement estimation result and the proposed method at floorplan stage for different congestion levels

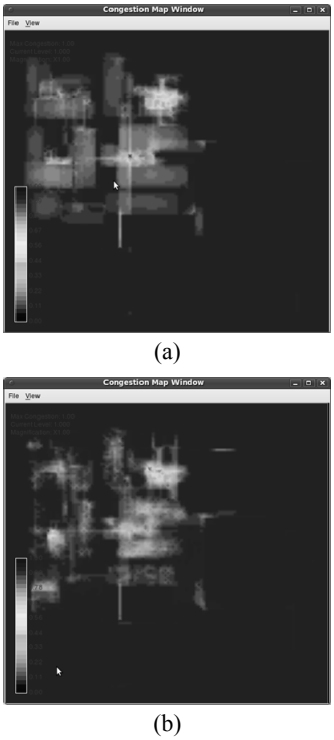
Chip		Difference for each congestion level (%)					Average (%)
		≥100%	90%~ 100%	80%~ 90%	70%~ 80%	≤70%	
Industrial I	Die1	-18.2	+23.8	-31.7	-13.1	+37.2	24.8
	Die2	-15.5	-26.9-	+21.7	-15.1	+16.2	19.1
Industrial II	Die1	+20.7	-21.4	-11.9	-14.6	+19.4	17.6
	Die2	-11.4	-27.6-	+16.8	-14.4	+19.8	18.0
Industrial III	Die1	+27.3	-16.9	-10.4	+19.4	-13.0	17.5
	Die2	+12.6	+9.4	-17.1	-21.1	+18.7	15.8
Total average		-	-	-	-	-	18.8

maps of die1.

The lighter areas stand for where have higher congestion degrees and the dark areas have lower congestion degrees. It clearly shows that the proposed estimation has almost identical result in overall appearance with post-placement estimation. Because the placement of cells hasn't been decided in floorplan, extremely precise estimation is impossible. So an estimation result with similar overall appearance and 18.8% error ratio is sufficiently accurate to be accepted.

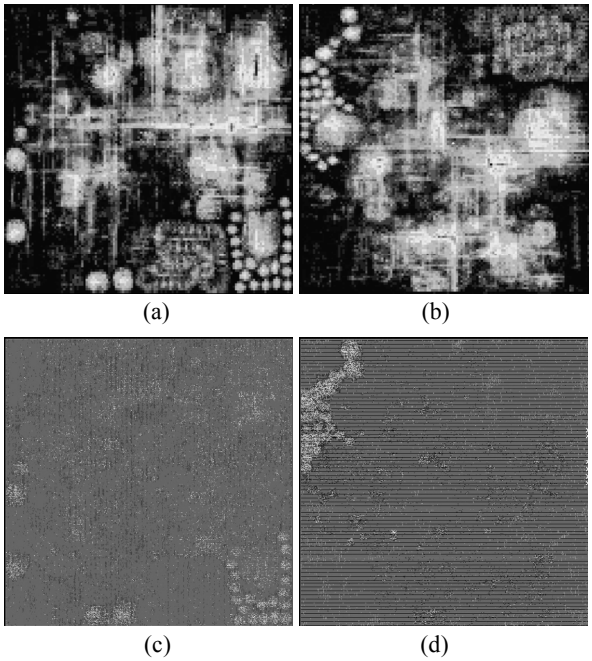
2. Comparison with Conventional Result at Routing Stage

In this experiment, we compared the congestion maps got by our proposed methodology with those got at routing stage. Also, the experimental chips in Table II were implemented by two-dies 3D ICs with face-to-back stacked. The third-party global router was used at routing stage. In Fig. 4, we present the congestion maps got by various methods for the Industrial III. Fig. 4(a) and (b) are the congestion maps predicted by our proposed methodology; while Fig. 4(c) and (d) are the congestion maps created by a third-party global router. Fig. 4(a) and (c) are congestion maps for die1; Fig. 4(b) and (d) are congestion maps for die2. In general, it is challenging to have the gird-by-grid accuracy between the estimated and actual congestion. However, the comparison of the two sets of congestion maps shows that we are able to accurately predict the congestion hot spots using our proposed methodology both in die1 and die2.



(a) (b)

Fig. 3. Routing congestion maps of die1 for Industrial I. (a) Congestion map estimated with proposed method at the floorplan stage, (b) Congestion map estimated with conventional method at the post-placement stage.



(a) (b)

(c) (d)

Fig. 4. Routing congestion maps for Industrial III. (a) and (b) are congestion maps of die1 and die2 got by our proposed method. (c) and (d) are congestion maps of die1 and die2 got by the third-party global router.

IV. CONCLUSIONS

In this paper, an estimation method of routing congestion for 3D ICs at floorplan stage has been proposed. This method considers both TSV location and various kinds of routing demand. The experiments demonstrate the accuracy of the method and we are able to accurately predict the congestion hot spots using our proposed methodology. Furthermore, it could be linked to a congestion aware floorplanner which minimizes routing failure. Optimizing the routing congestion using the proposed method would be a promising research topic in the future for 3D ICs.

ACKNOWLEDGMENTS

This research was supported by the MKE(The Ministry of Knowledge Economy), Korea, under the ITRC(Information Technology Research Center) support program supervised by the NIPA(National IT Industry Promotion Agency) (NIPA-2011-C1090-1100-0010).

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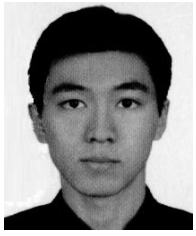

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