Journal of Information Display
Vol. 12, No. 4, December 2011, 213–217

Taylor & Francis
Taylor & Francis Group

Printed flexible OTFT backplane for electrophoretic displays

Gi-Seong Ryu, Myung Won Lee and Chung Kun Song*

Department of Electronics Engineering, Dong-A University, 840 Hadan-2 dong, Saha-gu, Busan 604-714, Republic of Korea

(*Received 17 July 2011; Revised 4 August 2011; Accepted 10 August 2011*)

Printing technologies were applied to fabricate a flexible organic thin-film transistor (OTFT) backplane for electrophoretic displays (EPDs). Various printing processes were adopted to maximize the figures of each layer of OTFT: screen printing combined with reverse offset printing for the gate electrodes and scan bus lines with Ag ink, inkjet for the source/drain electrodes with glycerol-doped Poly (3,4-ethylenedioxythiophene): Poly (styrenesulfonate) (PEDOT:PSS), inkjet for the semiconductor layer with Triisopropylsilylethynyl (TIPS)-pentacene, and screen printing for the pixel electrodes with Ag paste. A mobility of 0.44 cm^2/V s was obtained, with an average standard deviation of 20%, from the 36 OTFTs taken from different backplane locations, which indicates high uniformity. An EPD laminated on an OTFT backplane with 190 × 152 pixels on an 8-in panel was successfully operated by displaying some patterns.

Keywords: printing technology; OTFT; EPD; backplane; screen printing; inkjet printing; reverse offset printing

1. Introduction

In a ubiquitous-information society, any type of information should be capable of being obtained at any time and at any place. Thus, the displays should be flexible, with a high freedom-of-form factor, so that they can be installed at any place, such as on tables, walls, round-type pillars, and ceilings. In addition, as many displays will be needed to install them anywhere, they should be cheap. Thus, fabrication processes with an ultralow cost should be employed, such as printing technologies. Therefore, flexibility and printing technology are the keywords of the future displays.

Although several transistors are available as driving devices, the organic thin-film transistor (OTFT) is the most appropriate one in terms of flexibility and printing process. Various articles have reported on OTFT using solution processes for discrete devices [1–4]. Reports on the printed OTFT backplane, however, are rare [5,6].

In this study, printing technologies were developed for the flexible OTFT backplane, and the possibility and limitation of a printing technology for the OTFT backplane were determined.

2. Printing processes

The printing technology to be used should be carefully selected to maximize the unique functionality of each layer of OTFT because OTFT is an important device that determines the quality of displays. Its fabrication process is shown in Figure 1. At every step, a specific printing technology was applied: screen and reverse offset printing for the gate electrodes and scan bus lines, spin-coating for the gate dielectric, inkjet printing for the source and drain electrodes, inkjet printing for the semiconductor layer, spin-coating for the interlayer, and screen printing for the pixel electrodes. The important issues and results are described in the following sections.

2.1. Screen/reverse offset printing for the gate electrodes and scan bus lines

The material for the gate electrodes should be very highly conductive because the gate electrodes are connected to the long scan bus lines and, thus, the signal delay due to the resistance of the line should be minimized. The thickness of the gate electrodes should also be thin enough so that the subsequent gate dielectric could be deposited on the gate electrodes with good step coverage.

The processes that were used in this study were as follows. First, an Ag film was uniformly deposited onto a polycarbonate substrate via screen printing with nano-Ag ink. It was then cured at 200°C for 60 min to eliminate the organic components, such as the solvent and surfactant. Subsequently, the etching resist (ER) was printed on the Ag film via reverse offset printing, to form the gate electrode pattern. The final pattern of the Ag gate electrode was obtained after the chemical etching of the Ag film and the stripping off of the residual ER layer. A screen mask made of a stainless-steel fabric with 640 mesh count/inch was used, including a 5-μm-thick emulsion layer. The viscosity of the Ag ink was adjusted to make the Ag film less than 100-nm

*Corresponding author. Email: cksong@dau.ac.kr

ISSN 1598-0316 print/ISSN 2158-1606 online

http://dx.doi.org/10.1080/15980316.2011.621336
http://www.tandfonline.com

thick, to achieve good step coverage of the polyvinylphenol (PVP) gate dielectric on the gate [7].

As shown in Figure 2(a), the thickness of the Ag film was about 70 nm, and the PVP dielectric layer nicely covered the gate electrode. The resistivity was $7.5 \times 10^{-6}\ \Omega$ cm compared with $1.5 \times 10^{-5}\ \Omega$ cm of the thermally evaporated Al

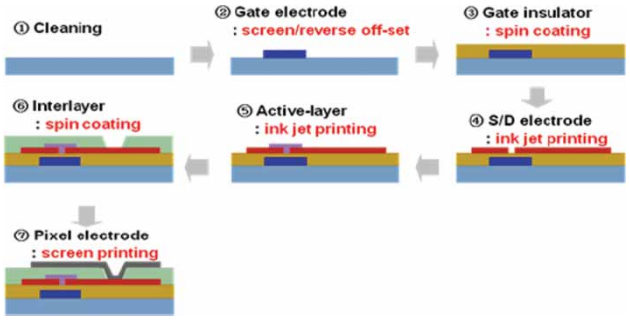

Figure 1. Schematics of the fabrication process of the OTFT backplane with printing technologies.

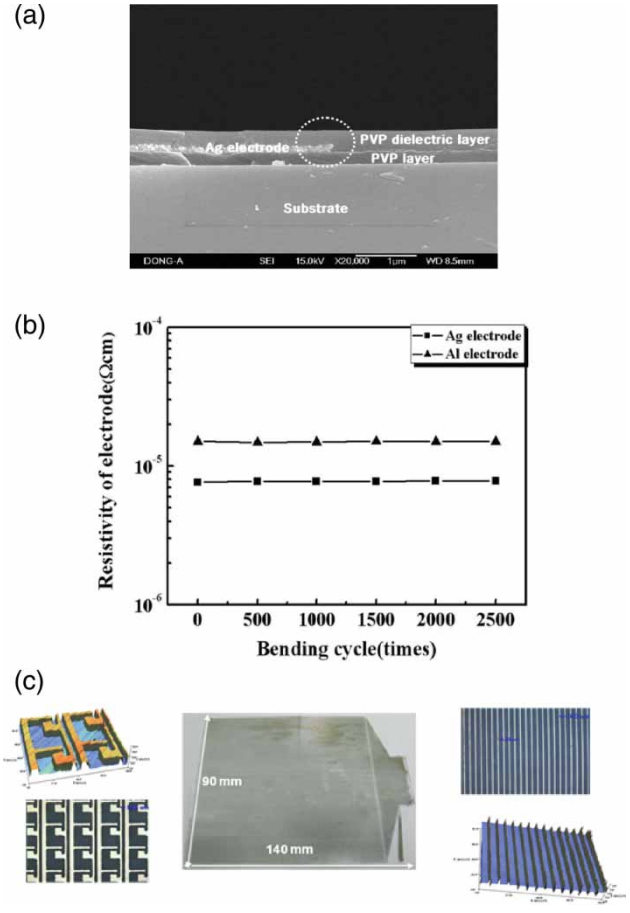

Figure 2. (a) FESEM images of the screen-printed Ag film. The Ag film is clearly shown, and the PVP dielectric layer is covered with the Ag film with good step coverage. (b) Resistivity of the Ag film compared with that of the evaporated Al. The resistivity was sustained after 2500 bendings. (c) The gate electrodes and scan bus lines with 30 μm line widths.

electrode, as shown in Figure 2(b). Moreover, the resistivity was not varied and was not peeled off even after the 2500-time bending test. The final pattern of the gate electrode is presented in Figure 2(c). The 30 μm line width was reliably produced.

2.2. *Spin-coating for the gate dielectric layer*

PVP was used for the gate dielectric and was deposited via spin-coating. With a dielectric constant of 3.6 at 1 MHz, the PVP gate insulator yields a high capacitance density with a value of 9.1 nF/cm^2 at 350 nm. Despite a large root mean square roughness of 2.5 nm from the PC substrate, the leakage current density of PVP at an applied field of 1 MV/cm was less than 10 nA/cm^2 when measured over a 0.004-cm^2 contact area.

2.3. *Inkjet printing for the source/drain electrodes and data bus lines*

The conducting polymer of PEDOT:PSS was used for the source and drain electrodes. The high resistivity of PEDOT:PSS was drastically reduced to $3 \times 10^{-3}\ \Omega$ cm by adding 10 wt% glycerol, which was about 3000 times smaller than that of the pristine PEDOT:PSS. The enhancement of the conductivity can be achieved through the conformational change of the PEDOT chain from coil to linear, through the interaction between glycerol and PEDOT [8]. The detailed description of the PEDOT process can be found in the article of Lee *et al*. [9]. The viscosity of the glycerol-doped PEDOT:PSS (G-PEDOT:PSS) was adjusted to be less than 20 cps for inkjet printing. The G-PEDOT:PSS ink was inkjetted and was nicely confined within the prepatterned S/D electrode area, as shown in Figure 3(a). The contact resistance to the evaporated pentacene semiconductor was 30 kΩ cm at $V_{GS} = -25$ V, comparable to that of the thermally evaporated Au electrode, as shown in Figure 3(b). The small contact resistance of G-PEDOT:PSS is attributed to the small injection barrier energy of G-PEDOT:PSS, such as 0.25 eV.

2.4. *Inkjet printing for the TIPS-pentacene semiconductor layer*

Inkjet printing is an appropriate method of conserving the expensive organic semiconductor because it can jet droplets only on a specific area. TIPS-pentacene ink was used for the semiconductor, and the TIPS-pentacene molecules were dissolved in an anisole solvent.

Usually, the droplet of TIPS-pentacene produces a coffee stain on the contact line of the droplet after drying, as shown in Figure 4(a), because the molecules continuously move to the contact line from the center while the contact line is fixed during drying. As most of the molecules accumulate on the coffee stain, the number of molecules in the middle of the droplet is not sufficient to be transported by

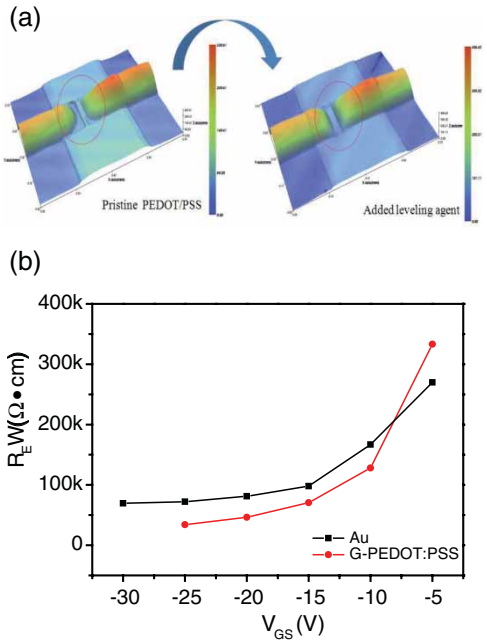

Figure 3. (a) 3D image of the S/D electrode that was inkjetted with glycerol-doped PEDOT:PSS on a PVP dielectric. (b) Contact resistance of the inkjetted G-PEDOT:PSS to a pentacene semiconductor compared with the evaporated Au electrodes.

the carriers, resulting in performance degradation. One way of removing coffee stain is by applying heat to the droplet during drying so that the contact line can continuously move toward the center during drying, generating a uniform layer after drying. As shown in the cross-section of the TIPS-pentacene layer in Figure 4(b), there was no longer any coffee stain. Moreover, the layer was very uniform, with a 45 nm thickness across the whole area. The morphology was dependent on the applied temperature. The appropriate temperature was determined to be 46°C in this case, which was extracted by varying the temperature and examining the morphology of TIPS-pentacene at each temperature. The detailed results will be published soon.

2.5. Spin-coating of the interlayer and screen printing for the pixel electrodes

The interlayer plays the role of separating the OTFT backplane from the electrophoretic display (EPD) sheet, which is laminated on the OTFT backplane and, thus, the electrical signal is provided to the EPD sheet only through the drain electrode. A two-layer system was used in this study for the interlayer consisting of water-soluble polyvinylacryl (PVA) and photoacryl. First, PVA was spin-coated on the TIPS-pentacene because water-soluble materials such as PVA minimize the damage to the organic semiconductor [10]. Subsequently, a thick photoacryl was deposited and patterned via lithography to make a via-hole for a pixel electrode. Finally, the pixel electrode was screen printed with

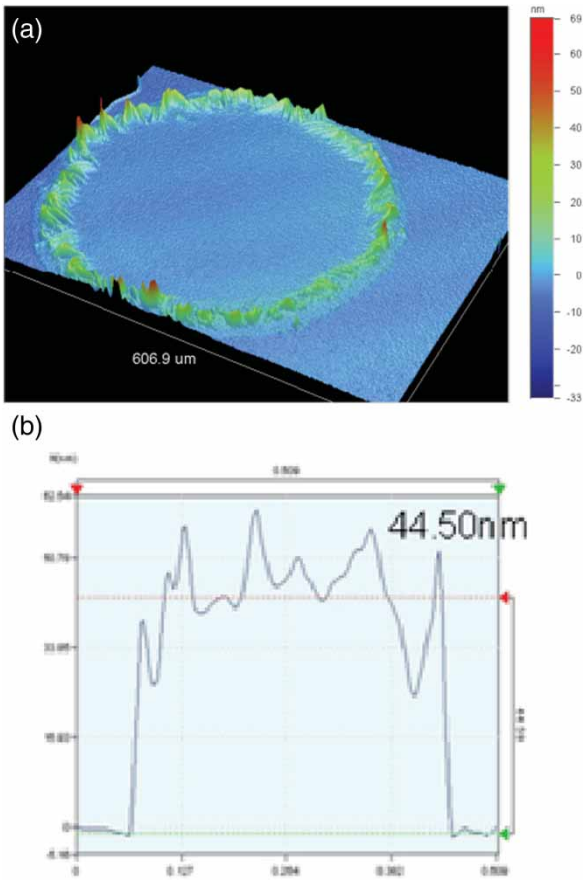

Figure 4. (a) A coffee stain formed by the inkjetted TIPS-pentacene droplet. (b) Cross-section of the heated TIPS-pentacene layer during drying. There was no coffee stain, and the uniform thickness was about 45 nm.

Ag paste on the interlayer. The via-hole and pixel electrodes are shown in Figure 5.

3. OTFT backplane for an EPD panel

A flexible OTFT backplane 8 in long in the diagonal direction and consisting of 150 × 192 pixels was designed. A pixel circuit consisted of one OTFT and one capacitor. As the turn-on time of the EPD was 130 ms, the frame frequency was selected to be 6.5 Hz ($t_{\text{frame}} = (1/6.5\text{Hz}) = 153\,\text{msec} > 130\,\text{msec}$). Based on the design rule, the OTFTs should supply an on-current larger than 0.52 μA ($I_{\text{on}} = (C_t \times V_{\text{on}}/\tau)$), where V_{on} is the on-voltage and τ is the time constant, which are 30 V and 0.204 ms, respectively, to charge up the total capacitor (C_t) of 3.57 pF, including the storage capacitance and the parasitic capacitance, in a limited scanning time of 1.02 ms. The off-state current should also be less than 38 pA ($I_{\text{off}} = (C_t \times \Delta V/t_{\text{frame}})$), where ΔV is the allowed voltage loss and 1.63 V, to sustain the voltage across the storage capacitor during the time frame of 153 ms.

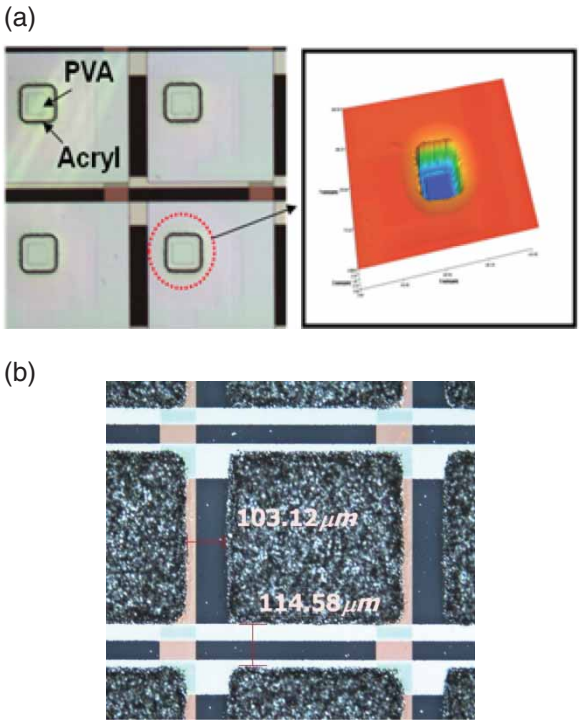

Figure 5. (a) The via-holes in the interlayer. (b) The pixel electrodes printed via screen printing.

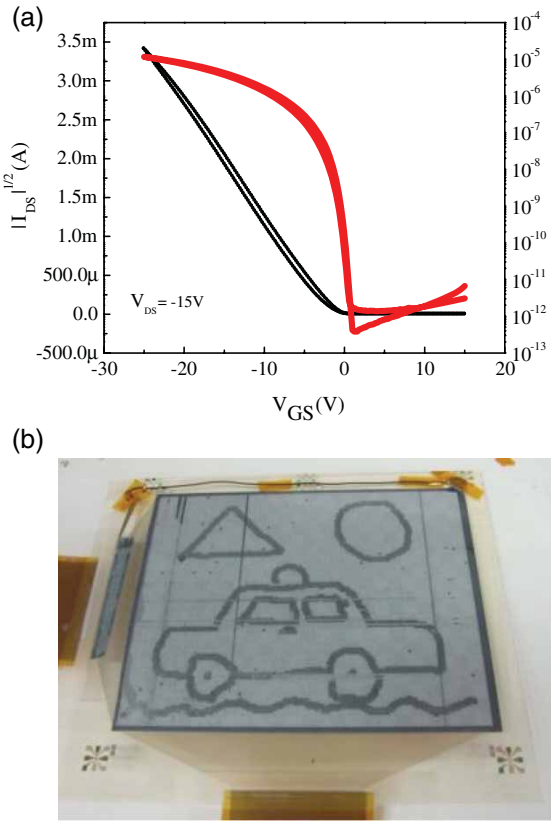

Figure 6. (a) Transfer characteristics of the TIPS-pentacene TFTs of the backplane. (b) The final EPD panel driven by the printed OTFT backplane.

In Figure 6(a), the transfer curve of the OTFT is presented together with the output curve. The on-current was 5 μA at $V_G = -10$ V, which was sufficiently large to charge up the storage capacitor within 0.8 ms. The off-state current was about 1 pA, which was sufficiently small to keep the voltage across the capacitor sustainable. What is interesting is that the turn-on voltage was exactly equal to 0 V, which indicates small interface states [11,12]. The performance parameters are summarized in Table 1, which were averaged from the 36 OTFTs located on different locations in the backplane. The mobility was 0.44 cm^2/V s, with a 20% standard deviation, exhibiting a very uniform performance considering the 28,800 OTFTs made over an 8-in area. The final panel was successfully operated to display some patterns, as shown in Figure 6(b).

4. Conclusion

A flexible OTFT backplane for EPDs was fabricated using printing processes. Screen printing combined with reverse offset printing was applied for the gate electrodes and scan bus lines, using Ag ink. The 30 μm line width was reliably produced. Especially, it was a meaningful result in terms of overcoming screen printing's drawback of the difficulty of making a film thinner than 1 μm, by achieving 70 nm thickness via screen printing. For the source and drain electrodes and the TIPS-pentacene semiconductor layer, inkjet printing was adopted to make fine patterns and to conserve the expensive semiconductor material. S/D electrodes were successfully patterned using glycerol-doped PEDOT:PSS, producing a small contact resistance of 30 kΩ cm at $V_{GS} = -25$ V, comparable to that of the Au electrode. A uniform thick TIPS-pentacene layer without coffee stain was obtained by heating the jetted droplet during drying. The thickness was uniformly 45 nm across the whole layer.

The flexible OTFT backplane was fabricated with the above printing processes, with a Quarter Video Graphic Array (QVGA) with 190 × 152 pixels on an 8-in substrate. The mobility of the OTFTs was 0.44(±0.08) cm^2/V s, which was averaged from the 36 OTFTs located on different places

Table 1. The performance parameters averaged from the 36 TIPS-pentacene OTFTs.

μ_{FET} (cm^2/V s)	$I_{on/off}$	V_{th} (V)	SS (V/dec)	I_{off} (pA/μm)
0.44(±0.08)	8.88(±5.76)×10^6	−1.57(±0.29)	0.33(±0.09)	5.31(±1.78)×10^{-3}

in the backplane. The EPD panel with the OTFT backplane was successfully operated to display some patterns.

Acknowledgements

This paper was supported by A Research Grant 2011 of Dong-A University.

References

[1] Y. Horii, K. Sakaguchi, M. Chikamatsu, R. Azumi, K. Yase, M. Kitagawa, and H. Konishi, Appl. Phys. Exp. **3**, 101601 (2010).

[2] H. Sirringhaus, Proc. IEEE **97**, 1577 (2009).

[3] S. Seo, C. Choi, Y. Hwang, and B. Bae, J. Phys. D: Appl. Phys. **42**, 035106 (2009).

[4] A.C. Huebler, F. Doetz, H. Kempa, H.E. Katz, M. Bartzsch, N. Brandt, I. Hennig, U. Fuegmann, S. Vaidyanathan, J. Granstrom, S. Liu, A. Sydorenko, T. Zillger, G. Schmidt, K. Preissler, E. Reichmanis, P. Eckerle, F. Richter, T. Fischer, and U. Hahn, Org. Elect. **8**, 480 (2007).

[5] R.A. Street, W.S. Wong, S.E. Ready, R. Lujan, A.C. Arias, and R. Apte, IS&T **20**, 1 (2005).

[6] K. Suzuki, K. Yutani, M. Nakashima, A. Onodera, S. Mizukami, M. Kato, T. Tano, H. Tomono, M. Yanagisawa, and K. Kameyama, in *Proc. International Display Workshops (IDW)*, Miyazaki, Japan, 1581 (2009).

[7] M.W. Lee, M.Y. Lee, and C.K. Song, J. Inform. Disp. **10**, 131 (2009).

[8] J. Ouyang, C.W. Chu, F.C. Chen, Q. Xu, and Y. Yang, Adv. Funct. Mater. **2**, 203 (2005).

[9] M.W. Lee, M.Y. Lee, J.C. Choi, J.S. Park, and C.K. Song, Org. Electron. **11**, 854 (2010).

[10] K. Tsukagoshi, I. Yagi, K. Shigeto, K. Yanagisawa, J. Tanabe, and Y. Aoyagi, Appl. Phys. Lett. **87**, 183502 (2005).

[11] H.L. Gomes, P. Stallinga, F. Dinelli, M. Murgia, F. Biscarini, D.M. Leeuw, T. Muck, J. Geurts, L.W. Molenkamp, and V. Wagner, Appl. Phys. Lett. **84**, 3184 (2004).

[12] S. Mathijssen, M. Colle, H. Gomes, E. Smits, B. Boer, I. McCulloch, P. Bobbert, and D.M. Leeuw, Adv. Mat. **19**, 2785 (2007).