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Highly stable amorphous indium–gallium–zinc-oxide thin-film transistor using an etch-stopper and a via-hole structure

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Highly stable amorphous indium–gallium–zinc-oxide (a-IGZO) thin-film transistors (TFTs) were fabricated with an etch-stopper and via-hole structure. The TFTs exhibited 40 cm^2/V s field-effect mobility and a 0.21 V/dec gate voltage swing. Gate-bias stress induced a negligible threshold voltage shift (ΔV_{th}) at room temperature. The excellent stability is attributed to the via-hole and etch-stopper structure, in which, the source/drain metal contacts the active a-IGZO layer through two via holes (one on each side), resulting in minimized damage to the a-IGZO layer during the plasma etching of the source/drain metal. The comparison of the effects of the DC and AC stress on the performance of the TFTs at 60°C showed that there was a smaller ΔV_{th} in the AC stress compared with the DC stress for the same effective stress time, indicating that the trapping of the carriers at the active layer–gate insulator interface was the dominant degradation mechanism.

Keywords: TFT; oxide semiconductor; stability

1. Introduction

Amorphous oxide semiconductors (AOSs) are promising candidates for channel materials in thin-film transistors (TFTs) for large-area, transparent, and/or flexible flat-panel displays. AOS TFTs exhibit a superior field-effect mobility of $>10\,cm^2/V$ s, which is sufficiently large for driving active-matrix organic light-emitting diode (AMOLED) displays and large-area active-matrix liquid crystal displays (AMLCDs), and operate at low voltages (<5 V) owing to their small gate voltage swing of ∼200 mV/dec [1,2]. The main research focus of late is to find a way to attain their improved long-term stability [3–7].

In this paper, highly stable amorphous indium–gallium–zinc-oxide (a-IGZO) TFTs fabricated on a glass substrate are demonstrated. Their stability is attributed to their via-hole and etch-stopper structure, which minimizes the damage to the a-IGZO layer during the TFT fabrication process. The impact of the thermal DC and AC stress on the performance of the TFTs was investigated to test the device stability.

2. TFT fabrication

Figure 1 shows a cross-sectional view of the a-IGZO TFTs that were used in this study. The TFTs have an inverted, staggered structure similar to that of the conventional a-Si TFTs, with an etch stopper and via holes. The via-hole structure is used to minimize the damage to the a-IGZO layer during the TFT fabrication process steps, such as source/drain metal formation, passivation, and a-IGZO etching.

The fabrication process was as follows: a 60 nm thick Mo was deposited on glass and was patterned as the gate electrode, then a 200 nm SiO_2 layer was deposited through plasma-enhanced chemical vapor deposition (PECVD) at 420°C, and a 20 nm a-IGZO layer (InO_3:Ga_2O_3:ZnO = 1 : 1 : 1 mol%) was deposited through reactive sputtering at 200°C. To protect the a-IGZO layer from damage, a 100 nm SiO_2 layer was deposited through PECVD at 200°C as an etch stopper. The SiO_2 and a-oxide were then wet-etched to form an active layer island and via holes. After this, a 100 nm Mo was deposited and patterned as the source/drain electrode. Finally, a 200 nm SiO_2 layer was deposited as the passivation layer, after which, via holes were formed and the Mo electrodes were patterned as shown in Figure 1. The samples were annealed at 250°C in vacuum for 2 h as a post annealing step.

3. Results and discussion

Figure 2 shows the transfer characteristics of the fabricated a-IGZO TFTs with 55 μm channel widths and 11 μm lengths. The saturation field-effect mobility extracted from the square root of the drain current ($\sqrt{(I_{ds})}$) when $V_{gs} = V_{ds}$ was ∼40 cm^2/V s at $V_{gs} = 15$ V. The threshold voltage extracted from the linear extrapolation of $\sqrt{(I_{ds})}$ was ∼2.6 V. The gate voltage swing at $V_{ds} = 0.1$ V was

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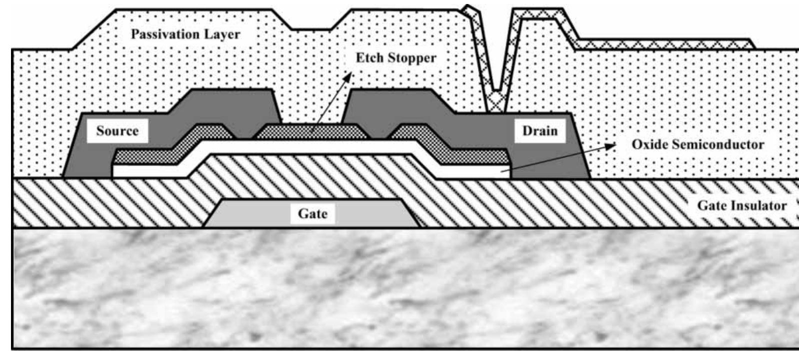

Figure 1. Cross-sectional view of the inverted, staggered a-IGZO TFT with via holes and an etch stopper.

~210 mV/dec. The off-current values were below 1×10^{-13} A even at $V_{ds} = 10$ V. The output characteristics (inset of Figure 2) showed no current crowding, indicating good ohmic contact.

To check the thermal stability of the TFTs, the transfer characteristics were measured at different temperatures, from room temperature (RT) to 80°C. Figure 3 shows the results, which clearly indicate high thermal stability. The activation energy was extracted from the Arrhenius plot of log (I_{ds}) versus the inverse of temperature, and the results are shown in the inset of Figure 3. The activation energy was less than 20 meV, indicating that the Fermi level was very close to the conduction band and that the a-IGZO has a very steep tail-state distribution.

The impact of the gate-bias stress on the performance of the a-IGZO TFTs was also investigated. Figure 4 shows the results of the application of the DC stress at RT. A DC gate bias of +20 V was applied for 5000 s while the source and drain electrodes were being grounded. The transfer characteristics barely changed after the application of the stress, indicating that the a-IGZO TFTs that were used in this study have high electrical stability. The same experiment was repeated for the AC stress, in which, an AC signal of 0–20 V, with a frequency of 5 kHz and a 50% duty ratio, was applied for 10,000 s while the source and drain electrodes were being grounded. A negligible change in the transfer characteristics was also observed at RT.

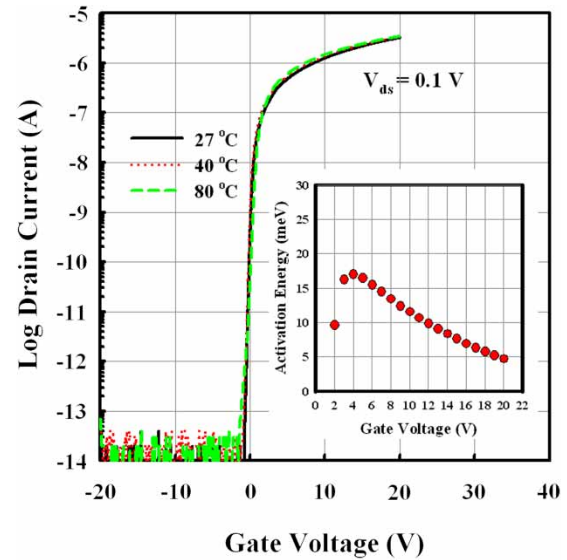

Figure 3. Transfer characteristics at different temperatures and the activation energy (inset) extracted from the Arrhenius plot of log (I_{ds}) versus $1000/T$.

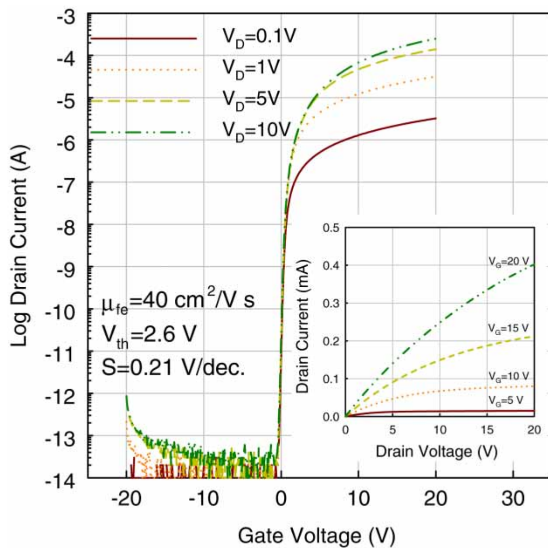

Figure 2. The transfer and output (inset) characteristics of the a-IGZO TFTs.

Change was observed only when the gate-bias stress-induced degradation was thermally activated. At 60°C, a small positive threshold voltage shift (ΔV_{th}) was observed after the application of either the DC or AC stress. The changes were still small, further confirming the electrical stability of the a-IGZO TFTs.

For a clearer analysis, the ΔV_{th} was plotted as a function of the effective stress time (T_{s_eff}) at RT and 60°C, for the DC and AC stress, as shown in the inset of Figure 4. For the

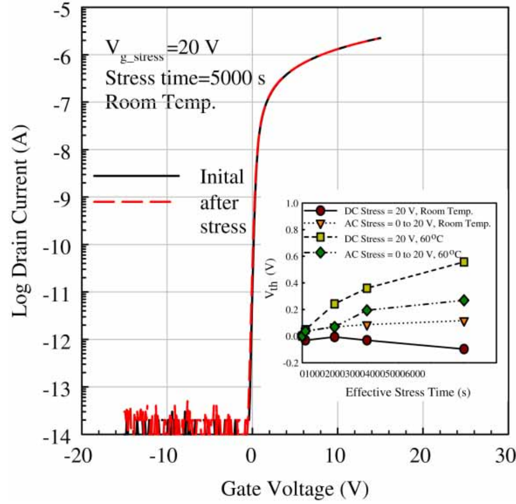

Figure 4. The transfer characteristics before and after the application of the DC stress at RT. The inset shows ΔV_{th} as a function of the effective stress time (T_{s_eff}) for the DC and AC stress at RT and 60°C. For the DC stress, the experimental stress time (T_s) was the same as T_{s_eff}. The AC pulse had a frequency of 5 kHz and a duty ratio of 50%. For the AC stress, T_{s_eff} was thus equal to $T_s/2$.

DC stress, the experimental stress time (T_s) was the same as T_{s_eff}, and for the AC stress, $T_{s_eff} = T_s/2$, because the duty ratio was 50%. At RT, ΔV_{th} was almost negligible for either the AC or DC stress. At 60°C, however, ΔV_{th} was approximately equal to 0.3 and 0.6 V after 5000 s effective stress time, respectively, for the AC and DC stress. This is a clear indication of charge trapping and detrapping during the application of the AC stress. The saturation mobilities and gate voltage swings of the TFTs showed no significant change after the application of either stress (AC or DC). This is due to the fact that the charge was trapped into the existing trap sites at the a-IGZO/SiO_2 interface and/or bulk oxide semiconductor, without the generation of new traps. When the transfer characteristics were measured after the application of stress, the trapped charge (electrons) screened the applied electric field, thereby reducing the effective gate voltage. This is the reason for the positive ΔV_{th}. It is also worth noting that the transfer characteristics can be recovered to the initial state by annealing at 250°C in vacuum for 2 h.

The ΔV_{th} of all the TFTs in this investigation is thus well described by the stretched-exponential equation [8,9]

$$\Delta V_{th}(t) = V_0 \left\{ 1 - \exp\left[-\left(\frac{t}{\tau} \right)^{\beta} \right] \right\}, \qquad (1)$$

where $V_o = V_{gs_stress} - V_{th0}$ is approximately the saturation ΔV_{th}, where V_{th0} is the initial V_{th} and τ is the characteristic trapping time of the carriers. The thermal activation energy is given by $E_a = E_\tau \beta$, with β being the stretched-exponential exponent, in which, E_τ is the average effective energy barrier that the electrons in the a-IGZO TFT channel need to overcome before they can enter the insulator [4,8]. Using the data for the DC stress at 60°C, a perfect fit with the experimental data was obtained when $\tau \sim 1.03 \times 10^5$ and $\beta \sim 0.2823$, yielding a characteristic trap-state (T_0) temperature of ∼1063 K. These results are in perfect agreement with the others [8,9]. In this study, the extracted β value is smaller compared with those in the previous reports. Apart from the use of an etch stopper and of via holes, this can also be attributed to the fact that the a-IGZO layer in this study was deposited at 200°C, whereas in the other studies [9–11], radio frequency sputtering was performed at RT. Moreover, in this study, a passivation layer was used to prevent the contamination of the active layer. It is believed that these factors, among others, enhanced the stability of the TFTs. Taking $E_a \sim 5 \times 10^{-3}$ eV at $V_{gs} = 20$ V (inset of Figure 3), $E_\tau \sim 1.77 \times 10^{-2}$ eV. The light-induced stability of the a-IGZO TFTs is described elsewhere [12].

In conclusion, highly stable, high-performance a-IGZO TFTs with an etch-stopper and via-hole structure were manufactured in this study to minimize the damage to the a-IGZO during the TFT fabrication process. The TFTs exhibited excellent device performance, with field-effect mobilities of 40 $cm^2/V\,s$ and gate voltage swings of 210 mV/dec. The thermal and electrical stability of these TFTs was also shown to be outstanding. While the device performance was unaffected by the DC and AC stress at RT, only a slightly positive threshold voltage shift was observed when the TFTs were stressed at 60°C. The shift is attributed to the charge trapping into the existing trap sites at the a-IGZO-SiO_2 interface and/or bulk oxide semiconductor, without the generation of new traps.

Acknowledgements

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