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Transferrable single-crystal silicon nanomembranes and their application to flexible microwave systems

Jung-Hun Seo[a], Hao-Chih Yuan[a], Lei Sun[a], Weidong Zhou[b] and Zhenqiang Ma[a]*

[a]*Department of Electrical and Computer Engineering, University of Wisconsin-Madison, WI, 53706, USA;*
[b]*Department of Electrical Engineering, University of Texas, Arlington, TX 76019, USA*

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This paper summarizes the recent fabrication and characterizations of flexible high-speed radio frequency (RF) transistors, PIN-diode single-pole single-throw switches, as well as flexible inductors and capacitors, based on single-crystalline Si nanomembranes transferred on polyethylene terephthalate substrates. Flexible thin-film transistors (TFTs) on plastic substrates have reached RF operation speed with a record cut-off/maximum oscillation frequency (f_T/f_{max}) values of 3.8/12 GHz. PIN diode switches exhibit excellent ON/OFF behaviors at high RF frequencies. Flexible inductors and capacitors compatible with high-speed TFT fabrication show resonance frequencies (f_{res}) up to 9.1 and 13.5 GHz, respectively. Robust mechanical characteristics were also demonstrated with these high-frequency passives components.

Keywords: flexible electronics; nanomembrane; radio frequency thin-film transistors; RF switches; inductors and capacitors

1. Introduction

Traditionally, flexible electronics are mostly based on organic or low temperature deposition compatible amorphous semiconductor (Si) materials. Devices made from these materials can only be operated at very low speed ($<<1$ GHz) because of the inferior carrier properties of these materials. Regardless of the low speed, these flexible electronics are suitable for applications in products such as flexible displays [1], electronic tags [2], etc. In these applications, the mechanical flexibility of electronics is of critical importance. On the other hand, a number of other applications do require the use of extremely high-speed devices (>1 GHz, the radio frequency (RF) speed), such as Wi-Fi devices, wearable radios, RF identification devices, foldable phased-array antennas, large-area radars for remote sensing, surveillance [3], etc. Nonetheless, current high-speed devices have been predominantly made of rigid chips and none of the traditional flexible active semiconductors can satisfy the requirements of high-speed applications.

A promising solution toward high-speed flexible electronics has emerged with the recent development of transferrable single-crystal Si nanomembranes (SiNMs) [4–7]. By releasing high-quality flexible materials from silicon-on-insulator (SOI) and other types of substrates and transferring them to a new host substrate, high carrier mobility comparable with that of the bulk counterpart has been demonstrated [5].

In this paper, we summarize our recent work on the fabrication and characterizations of flexible high-frequency transistors, PIN-diode single-pole single-throw (SPST) switches, based on transferrable single-crystal Si NMs, as well as flexible inductors and capacitors on polyethylene terephthalate (PET) substrates. These can be integrated together with the flexible actives on the same substrate.

2. Experiment

In order to fabricate high-speed active devices, thin-film transistors (TFTs) using high mobility and transferrable NMs, one critical step is to realize very low parasitic resistance for the TFTs (aside from using small device feature sizes). To minimize the source and drain (S/D) resistance of field-effect type TFTs, heavy doping is the straightforward approach to making low-resistance ohmic contacts at the source and the drain. For Si processing, heavy doping can be realized with thermal diffusion and ion implantation, which (particularly the latter) are commonly used in the Si CMOS industry. However, both doping methods require high temperature processing (>800 °C) procedures. For SiNMs to be preferably transferred on low-cost, flexible substrates such as PET (softening temperature: 170 °C), such high temperature processing is not allowed. To solve the problem, we proposed and successfully implemented an effective pre-release doping method for transferrable Si NMs [8]. Figure 1 presents an illustration of the generic process flow.

*Corresponding author. Email: mazq@engr.wisc.edu

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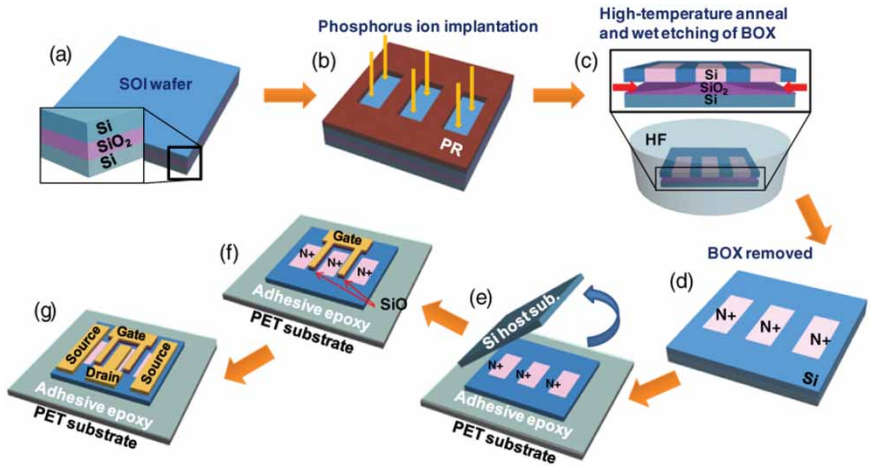

Figure 1. Generic process flow of TFT fabrication. (a) SOI. (b) Ion implantation. (c) High-temperature anneal to activate dopants and BOX wet etching. (d) Removal of BOX. (e) Direct flip transfer of SiNMs to PET. (f) Low-temperature gate stack formation. (g) Source/drain metallization.

For the fabrication of N-type TFTs, the top Si layer starting with a lightly P-type doped SOI substrate (Figure 1(a)) with a typical thickness of 200–300 nm, was patterned, using photolithography for the S/D region formation. Phosphorous ion implantation was performed to heavily dope the opened S/D areas (Figure 1(b)). The selection of ion implantation dose and energy depends on a number of factors, including the transfer method (stamp-assisted transfer or direct flip transfer) and the Si NM thickness. If stamp-assisted transfer method for Si NMs is utilized [5], the top surface of the Si NMs must have a high dopant concentration. Otherwise, the bottom surface of Si NMs must have a sufficient high dopant concentration, since the Si NMs will be flipped over during the transfer under the direct flip transfer method. For the studies summarized in this paper, flip transfer was used in all the devices. The low resistance S/D regions were formed after a furnace anneal (typically 850 °C) was performed to activate the implanted dopants (Figure 1(c)). The minimum device feature sizes of the TFTs are largely determined by the ion implantation and the annealing steps.

The pre-doped Si layer was then released from the SOI (Figure 1(c)). The releasing step can be done by first patterning the Si layer into strips or a membrane form with mesh holes. The patterned SOI substrate was immersed in hydrofluoric acid in order to undercut the buried oxide (BOX) layer selectively [8]. Depending on the thickness of the BOX, the released Si layer, now referred to as SiNMs, can fall and register with the handling Si substrate (if BOX is thin enough) (Figure 1(d)) or float up in the HF. In the latter case, some anchors need to be designed to hold the SiNMs in place during the release process. For the studies summarized in this paper, all BOX layer thickness ranged from 145–200 nm, which is thin enough for the SiNMs to be held on the handling substrate via van der Waals force [9]. Using the thin-BOX SOI made the SiNMs release and subsequent transfer easier.

The released SiNM was then transferred to a new flexible host, PET. With the flip transfer, a glue layer such as SU-8 was spin-coated on the new host. The new host is then brought to the SOI and the Si handling substrate is detached. The released SiNM will be flipped over and transferred to the PET substrate (Figure 1(e)). A backside UV-curing will permanently fix the SiNMs on the PET substrate. Subsequent TFT fabrication steps were carried on the new host. The device isolation was realized using dry plasma etching down the SU-8 layer. Gate stack with low-temperature gate dielectric (such as evaporated SiO) was formed (Figure 1(f)) followed by metallizations for gate, S/D (Figure 1(g)). Since the heavily doped source/drain regions were formed prior to the gate stack formation, this process of metal-oxide-semiconductor TFT fabrication can be referred to as a gate-after-source/drain process, different from the self-aligned bulk Si MOSFET fabrication. By changing the source/drain and the gate formation order, we successfully circumvented the high temperature requirement for low-resistance source/drain formation, but at the same time prohibited the PET substrate.

The PIN diode fabrication process is very similar to the TFT fabrication, except that a P-type ion implantation was added after the N-type ion implantation before SiNM was released [10,11]. No gate stack was needed for PIN diodes. A series-shunt configuration was used to connect two PIN diodes and form a SPST RF switch on PET.

The fabrication of passive components (inductors and capacitors) starts with the fabrication of a metal layer (M1) of 30 nm/400 nm Ti/Au, which functions as the bottom electrode of metal–insulator–metal (MIM) capacitors, or the center lead metal of spiral inductors. SiO was deposited on top of M1. Another metal layer (M2) was then evaporated and lifted off as the top electrode to form the MIM structure of the capacitors. Finally, a 30 nm/1.5 μm Ti/Au top interconnect metal (M3) was evaporated to form the spiral metal

of the inductors and to establish interconnects for both the inductors and the capacitors. This fabrication process for passives is very similar to that used for passives fabricated on a rigid substrate. To enhance mechanical flexibility under bending, we used SU-8 as the inter-metal dielectric instead of SiO [12].

3. Results

Figure 2 presents three flexible TFTs with varying device critical dimensions. Figure 2(a) shows a typical device picture on PET while Figure 2(b) shows the transfer curve along with the transconductance of each device. As shown in Figure 2(b), the unit-gate-length transconductance values

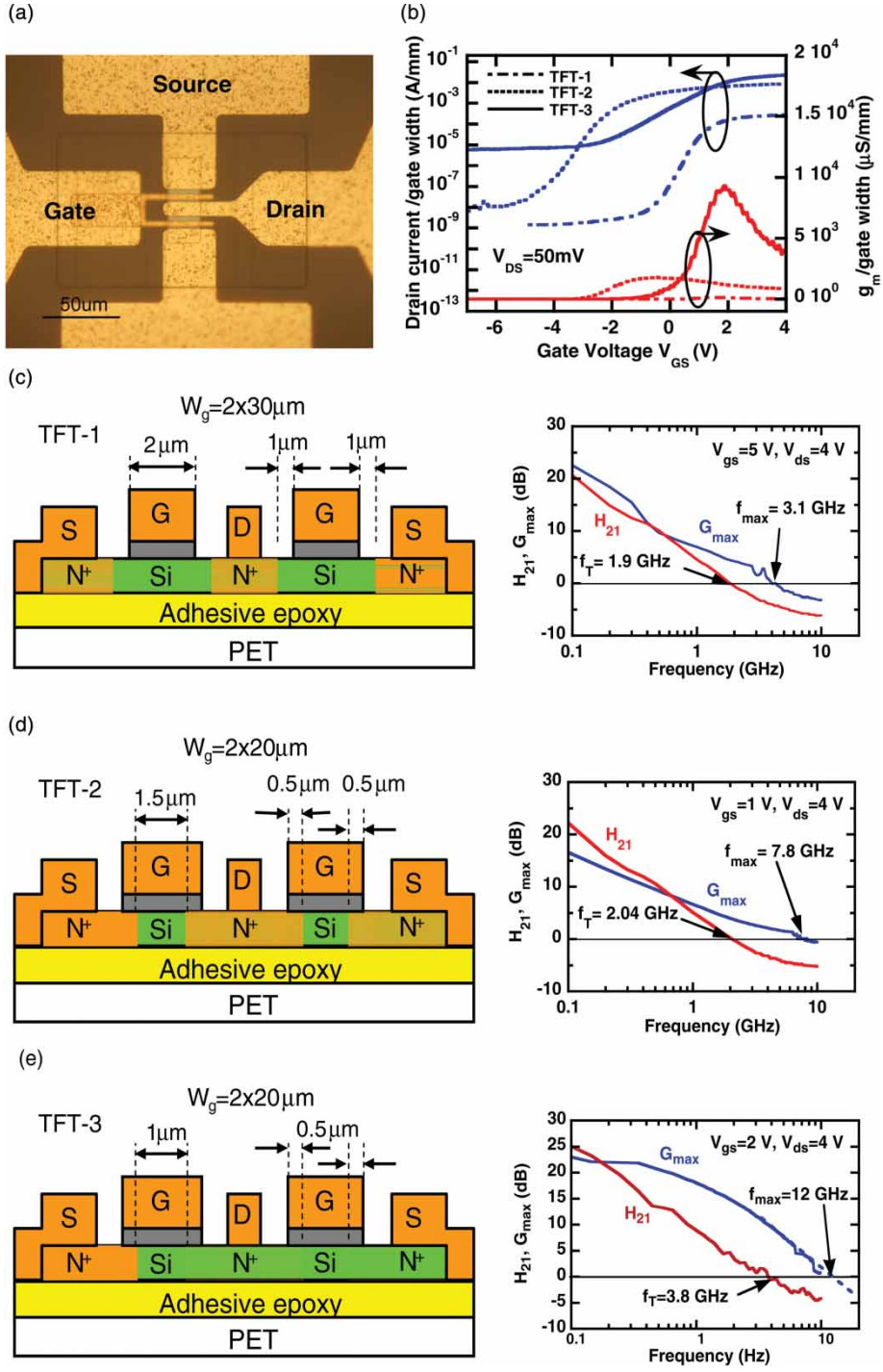

Figure 2. (a) An optical image of a typical fabricated TFT on PET. (b) Measured unit-gate-length transconductance values of TFTs having different device critical dimensions. Three TFT cross-sections showing the variations of the critical dimensions along with their measured frequency response characteristics: (c) TFT-1, (d) TFT-2 and (e) TFT-3.

(g_m/mm) continues to increase with the decrease in the device critical dimension. The peak values for the three devices are 146.8, 1777.5, and 9315 μS/mm. The estimated corresponding effective mobilities are 230, 331 and 423 $cm^2/V \cdot s$, respectively. The cut-off frequency (f_T) was also increased with the reduction of the critical dimensions, as shown in Figure 2(c)–(d). The maximum oscillation frequency (f_{max}) dramatically increases with the increase of f_T and particularly with the reduction of the parasitic/access resistance [8,10,11]. Forming smaller feature sizes (e.g. 1–1.5 μm gate lengths) for the TFTs on a PET substrate is rather difficult due to the thermal expansion of the soft substrate during photoresist baking and due to misalignment with pre-doped regions caused by SiNM transfer. To overcome these problems, we investigated a local gate alignment TFT process. Conceptually similar to the lithography using a stepper on a large-diameter Si wafer, we align the gate stacks with the pre-doped SiNMs in a smaller area, where

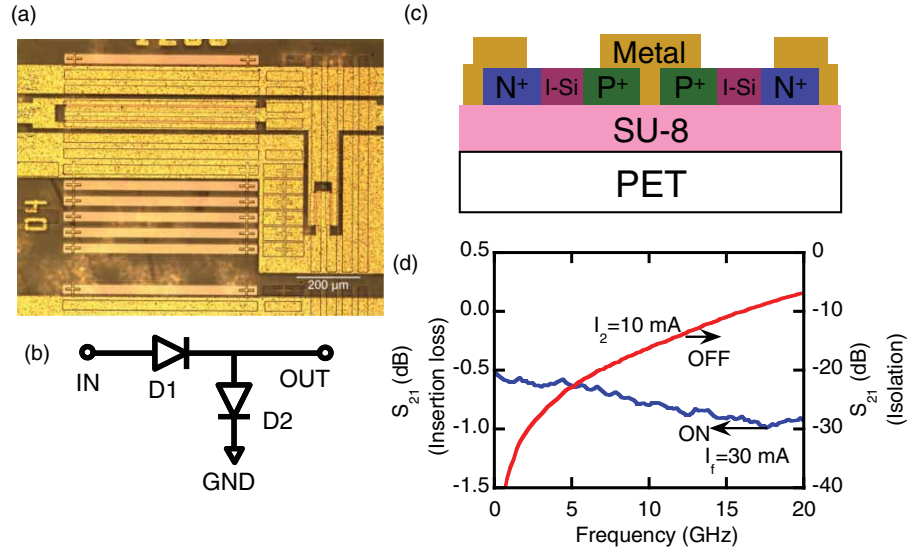

Figure 3. (a) An optical image of a PIN diode RF switch on PET. (b) Series-shunt configuration of the RF switch. (c) Cross sectional view of PIN diodes. (d) Measured small-signal RF characteristics of the RF switch.

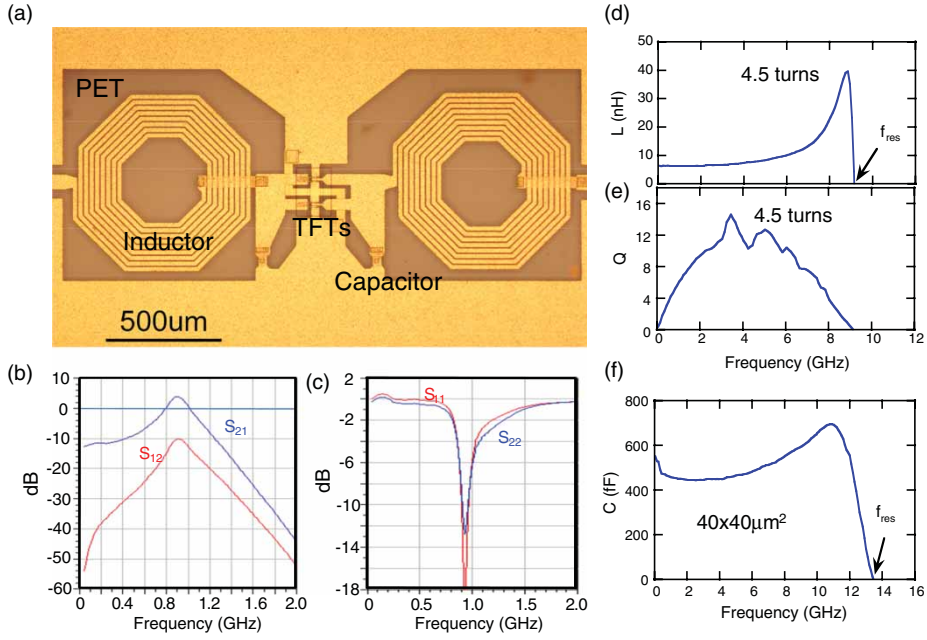

Figure 4. (a) An optical image of an RF amplifier integrating TFTs, spiral inductors and MIM capacitors, all fabricated on PET. (b) and (c) Simulated amplifier performance with measured TFT ($f_{max} = 7.8$ GHz), inductor and capacitor S-parameters. (d) Measured L values and (e) measured Q value of a 4.5-turn spiral inductor, and (f) measured C values of a 40 × 40 μm^2 MIM capacitor as a function of frequency under flat condition.

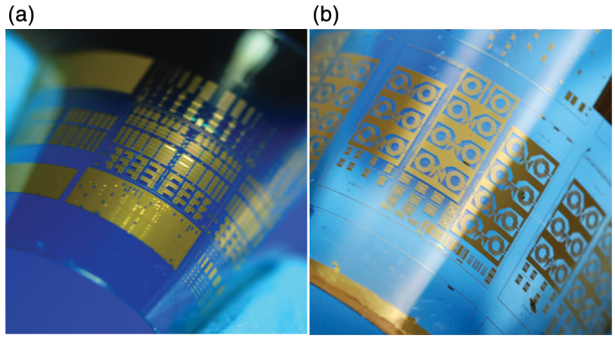

Figure 5. (a) An array of RF switches on a bent PET substrate. (b) An array of RF amplifier (integrating TFTs, inductors and capacitors) on a bent PET substrate.

misalignment is tolerable within the desired range. The alignment procedure was repeated until the entire chip was exposed. This local alignment allowed us to fabricate TFTs on PET with gate lengths as small as 1 μm [13]. Remarkable device speed, 12 GHz, has been achieved as shown in Figure 2(e).

Figure 3 shows the small-signal RF characteristics of a series-shunt PIN diode switch. The series and shunt diodes have an area of 240 and 40 μm^2, respectively. As can be seen, the RF switch exhibited superior performance up to very high frequencies (20 GHz) [11,12].

Figure 4 shows the flexible inductors and capacitors fabricated on PET and integrated with TFTs (7.8 GHz). The simulated amplifier performance is shown in Figure 4(b) and (c). The individual inductor and capacitor performance characteristics are shown in Figure 4(d)–(f) [14]. For a 4.5-turn inductor, a resonant frequency (f_{res}) of 9.1 GHz was realized. The peak Q of 14.6 was measured at 3.45 GHz. For a 40 × 40 μm^2 capacitor, a value of 0.45 pF at 4 GHz was obtained with a f_{res} of 13.5 GHz. The Q value obtained is 6.4 at 4 GHz.

Figure 5 shows some bent images of the RF switch array and RF amplifier array on PET substrates. All these devices exhibited superior bending characteristics. A bending radius as small as 28.5 mm was attempted without inducing cracks on the devices.

The above examples clearly indicated the feasibility of fabricating high-speed flexible electronics at RF frequencies using transferrable SiNMs. Higher speed operation of TFTs and high-performance practical RF amplifiers on flexible substrates are also possible by applying advanced lithography on the SiNMs.

4. Summary

Utilizing transferrable SiNMs, microwave TFTs and PIN diode switches were demonstrated on low temperature flexible substrates. RF amplifiers and other circuits can be realized on flexible substrates with the flexible TFTs having a f_T of 3.8 GHz and f_{max} of 12 GHz. The RF switches exhibit insertion loss better than 0.62 dB and isolations higher than 22.9 dB up to 5 GHz. Flexible inductors and capacitors demonstrated on the same flexible substrate have f_{res}'s of 9.1 and 13.5 GHz and Q values of 14.6 and 6.4, respectively. These results strongly indicate the feasibility of high-speed flexible electronics employing properly processed, transferrable SiNMs. Further investigations on SiNMs will lead to flexible microwave systems characterized by both higher-performance and mechanical flexibility for various wireless applications.

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References

[1] J. Park, T. Kim, D. Stryakhilev, J. Lee, S. An, Y. Pyo, D. Lee, Y. Mo, D. Jin, and H. Chung, Appl. Phys. Lett. **95**, 013503 (2009).
[2] V. Subramanian, P.C. Chang, J.B. Lee, S.E. Molesa, and S.K. Volkman, IEEE Trans. Compon. Packag. Technol. **28**, 742 (2005).
[3] R.H. Reuss, B.R. Chalamala, A. Moussessian, M.G. Kane, A. Kumar, D.C. Zhang, J.A. Rogers, M. Hatalis, D. Temple, G. Moddel, B.J. Eliasson, M.J. Estes, J. Kunze, E.S. Handy, E.S. Harmon, D.B. Salzman, J.M. Woodall, M.A. Alam, J.Y. Murthy, S.C. Jacobsen, M. Oliver, D. Markus, P.M. Campbell, and E. Snow, Proc. IEEE **93**, 1239 (2005).
[4] A. Tilke, M. Rotter, R.H. Blick, H. Lorenz, and J.P. Kotthaus, Appl. Phys. Lett. **77**, 558 (2000).
[5] E. Menard, K.J. Lee, D.-Y. Khang, R.G. Nuzzo, and J.A. Rogers, Appl. Phys. Lett. **84**, 5398 (2004).
[6] E. Menard, R.G. Nuzzo, and J.A. Rogers, Appl. Phys. Lett. **86**, 093507 (2005).
[7] Y. Sun, S. Kim, I. Adesida, and J.A. Rogers, Appl. Phys. Lett. **87**, 083501 (2005).
[8] H.-C. Yuan and Z. Ma, Appl. Phys. Lett. **89**, 212105, 2006.
[9] G. M. Cohen, P.M. Mooney, V.K. Paruchuri, and H.J. Hovel, Appl. Phys. Lett. **86**, 251902 (2005).
[10] H.-C. Yuan, G.K. Celler, and Z. Ma, J. Appl. Phys. **102**, 034501, 2007.
[11] H.-C. Yuan, G. Qin, G.K. Celler, and Z. Ma, Appl. Phys. Lett. **95**, 043109, 2009.
[12] G. Qin, H.-C. Yuan, G.K. Celler, W. Zhou, and Z. Ma, J. Phys. D, Appl. Phys. **42**, 234006, 2009.
[13] L. Sun, G. Qin, J.-H. Seo, G.K. Celler, W. Zhou, and Z. Ma, Small **6**(22), 2553, 2010.
[14] L. Sun, G. Qin, H. Huang, H. Zhou, N. Behdad, W. Zhou, and Z. Ma, Appl. Phys. Lett. **96**, 013509, 2010.