An Accurate Small Signal Modeling of Cylindrical/Surrounded Gate MOSFET for High Frequency Applications

Pujarini Ghosh*, Subhasis Haldar, R. S. Gupta***, and Mridula Gupta***

Abstract—**An intrinsic small signal equivalent circuit model of Cylindrical/Surrounded gate MOSFET is proposed. Admittance parameters of the device are extracted from circuit analysis and intrinsic circuit elements are presented in terms of real and imaginary parts of the admittance parameters. S parameters are then evaluated and justified with the simulated data extracted from 3D device simulation.**

Index Terms—**Small signal equivalent circuit, short channel effect (SCEs), cylindrical/surrounded gate MOSFET (CGT/SGT), S-parameters, Y-parameters, unilateral transducer power gain (U_T), maximum stable power gain (Gms), maximum unilateral transducer power gain ($G_{TU\,\max}$)**

I. INTRODUCTION

The designing of the analog and digital integrated circuits requires an authentic device model, which is an important tool to carry out high-speed digital applications. A large-signal model should be used which will describe the active device over the whole operating range from dc to tera hertz region. The most suitable method to examine a MOSFET at high frequencies involves S-parameter measurements [1]. For the characterization of the broadband behavior of a MOSFET device, measurements have to be performed at many bias settings over the frequency range of interest, as the electrical properties of MOSFET strongly depend on the applied gate bias and drain to source bias. This enormous amount of S-parameter data of a single MOSFET can be reduced to a set of fifteen frequency-independent variables using an equivalent circuit of physically meaningful elements. Several commercially available programs exist which optimize some or all of these fifteen parameters [2], although in general the measured S-parameter data are approximated in an acceptable manner by these methods and the resulting element values depend on the starting values and may differ considerably from their actual physical values [1-3]. The analytical methods [4-7] on the other hand allow us to extract the equivalent circuit parameters in a straightforward manner. The most favorable extraction method was originally proposed by Minasian et al. [7] and was later modified by Dambrine et.al [5] and Berroth & Bosch [6]. This method first extracted the series and shunt parasitic elements of the device by measuring the S parameters under suitable passive modes of its operations. Once these parasitic elements are carefully determined, the S-parameters are then measured under active mode of device operation. These are then successively transformed into Z and Y-parameters. In the present analysis, a similar equivalent circuit model has been extended for CGT/SGT MOSFET [8, 9] where the Y parameters are analytically calculated from the equivalent circuit and then S parameters are

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* Semiconductor Device Research Laboratory, Department of Electronic Science, University of Delhi, South Campus, New Delhi , 110021, India
Tel : 91-11-24115580; Fax : 91-11-24110606
E-mail : mridula@south.du.ac.in, puja510@gmail.com.
** Department of Physics, Motilal Nehru College, University of Delhi, New Delhi, 110021 India
*** Department of Electronic and Communication engineering, Maharaja Agrasen Institute of Technology, Rohini, Delhi 110085, India

extracted from that. The advantage of CGT/SGT MOSFET is that it allows excellent control of the charges over the channel thus controlling the scaling limitations caused due to the short channel effects (SCEs), there by increasing the device performances. In CGT/SGT MOSFET design as shown in Fig. 1. the source, drain and gate are arranged vertically and the sidewalls of the pillar are used as the channel region due to which the structure has a large effective channel width even in a small-occupied area. As a result, the channel length can be adjusted without changing the occupied area of the MOSFET resulting in high packing density.

In this paper, a model with intrinsic equivalent circuit of CGT/SGT MOSFET (Fig. 2) is proposed. Admittance parameters of CGT/SGT MOSFET are solved using circuit analysis and intrinsic circuit elements are presented in terms of real and imaginary part of the admittance parameters. S-parameters and gains are then evaluated over the tera hertz frequency range. The analytical results are compared with S-parameters of CGT/SGT MOSFET and bulk MOSFET evaluated from the device simulator and a good agreement is obtained between model and simulated data which validates our theoretical analysis. Different gains for CGT/SGT MOSFET are compared with bulk MOSFET and found that CGT/SGT architecture gives better gain as compared to bulk MOSFET hence better device efficiency.

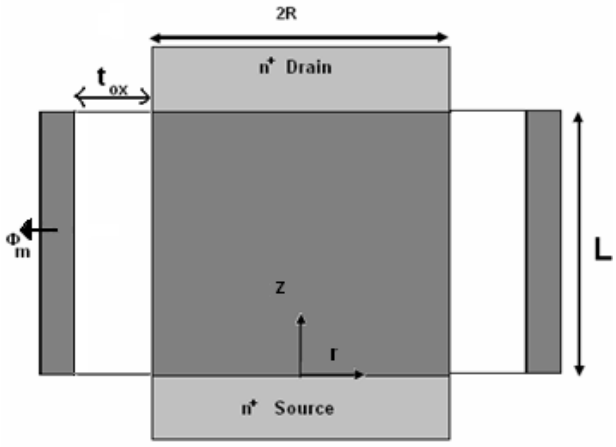

Fig. 1. Cross sectional view of Cylindrical/Surrounded gate MOSFET. t_{ox}=2.5 nm, R=10 nm, L=50 nm, Φ_m=4.8 eV, N_D^+=5 x 10^{19} cm^{-3}, N_A=10^{16} cm^{-3}, V_{gs}=0.5 V & 1 V and V_{ds}=0.5 V unless stated otherwise. [10]

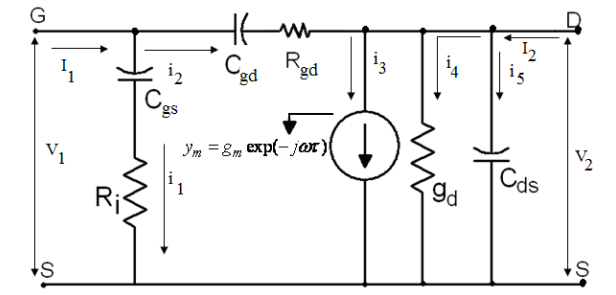

Fig. 2. Small signal equivalent circuit of Cylindrical/ Surrounded gate MOSFET used for network analysis.

II. ANALYTICAL MODELING

The small signal equivalent circuit of CGT/SGT MOSFET consisting of intrinsic device elements is shown in Fig. 2. Using network analysis techniques, the Y parameters for the simplified circuit model can be derived from Fig. 2.

$$I_1 = i_1 + i_2 \tag{1}$$

$$I_2 = i_4 + i_5 + i_3 - i_2 \tag{2}$$

Using nodal analysis, I_1 and I_2 can be obtained as,

$$I_1 = \frac{V_1\left(j\omega C_{gs}\right)}{\left(j\omega C_{gs}R_i + 1\right)} + \frac{\left(V_1 - V_2\right)\left(j\omega C_{gd}R_{gd}\right)}{\left(1 + j\omega C_{gd}R_{gd}\right)} \tag{3}$$

$$I_2 = V_2 j\omega C_{ds} + V_2 g_d + \frac{V_1}{1 + j\omega C_{gs}R_i} g_m\left(-j\omega\tau\right) - \frac{\left(V_1 - V_2\right)\left(j\omega C_{gd}\right)}{1 + j\omega C_{gd}R_{gd}} \tag{4}$$

The different Y- parameters can be obtained as follows:

(i) The input admittance Y_{11} is defined as

$$Y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2=0} \tag{5}$$

From (3) using V_2=0 we have

$$Y_{11} = \frac{\omega^2 C_{gs}{}^2 R_i^2}{D} + \frac{\omega^2 C_{gd}{}^2 R_{gd}}{D'} + \frac{j\omega C_{gs}}{D} + \frac{j\omega C_{gd}}{D'} \tag{6}$$

where,

$$D = 1 + \omega^2 R_i{}^2 C_{gs}{}^2 \tag{7}$$

$$D' = 1 + \omega^2 R_{gd}{}^2 C_{gd}{}^2 \tag{8}$$

Since R_{gd} is very small (6) can be simplified as,

$$Y_{11} = \frac{\omega^2 C_{gs}{}^2 R_i}{D} + j\omega\left(\frac{C_{gs}}{D} + C_{gd}\right) \tag{9}$$

(ii) Y_{12}, the reverse transfer admittance is defined as,

$$Y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1=0} \tag{10}$$

putting $V_1=0$ in (3)

$$Y_{12} = \frac{-j\omega C_{gd}}{D_2} - \frac{\omega^2 C_{gd}{}^2 R_{gd}}{D_2} \tag{11}$$

Which on neglecting R_{gd}, Y_{12} becomes,

$$Y_{12} = -j\omega C_{gd} \tag{12}$$

(iii) Y_{21}, is defined as forward transfer admittance

$$Y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2=0} \tag{13}$$

substituting $V_2=0$ in (4)

$$Y_{21} = \frac{g_m \exp(-j\omega\tau)}{1 + j\omega C_{gs} R_i} - \frac{j\omega C_{gd}}{1 + j\omega R_{gd} C_{gd}} \tag{14}$$

neglecting R_{gd} again, Y_{21} becomes

$$Y_{21} = \frac{g_m \exp(-j\omega\tau)}{1 + j\omega C_{gs} R_i} - j\omega C_{gd} \tag{15}$$

(iv) Y_{22}, the output admittance is calculated as

$$Y_{22} = \left.\frac{I_2}{V_2}\right|_{V_{1=0}} \tag{16}$$

substituting $V_1=0$ in (4) gives,

$$Y_{22} = g_d + j\omega\left[C_{ds} + \frac{C_{gd}}{D'}\right] + \frac{\omega^2 C_{gd}{}^2 R_{gd}}{D'} \tag{17}$$

which on neglecting R_{gd} the Y_{22} becomes

$$Y_{22} = g_d + j\omega(C_{ds} + C_{gd}) \tag{18}$$

ω is given as

$$\omega = 2\pi f \tag{19}$$

where f is the frequency of operation.

The intrinsic small signal elements such as transconductance g_m, drain conductance g_d, gate-to-source capacitance C_{gs} and gate-to-drain capacitance C_{ds} are obtained from the dc characteristics of current and charge as a function of applied gate potential V_{gs} and drain potentials V_{ds}. The Poisson's equation is solved using unified charge control model, [11, 12] to obtained the expressions for current, I_{ds} and total inversion charge, Q_{Tol}.

$$I_{DS} = \frac{2\pi R\mu}{L}\left[2\frac{kT}{q}(Q_s - Q_d) + \frac{Q_S{}^2 - Q_d{}^2}{2C_{ox}} + \frac{kT}{q}Q_0 \log\left(\frac{Q_d + Q_0}{Q_s + Q_0}\right)\right] \tag{20}$$

$$Q_{Tol} = -(2\pi R)^2 \frac{\mu}{I_{DS}} \int_0^{V_{DS}} Q^2 dV \tag{21}$$

where Q_s and Q_d are the charges at the source end and drain end respectively, Q represents the mobile charge sheet density per unit area, q is the electronic charge, μ is the effective mobility of the electrons, L is the channel length, $2\pi R$ is the device width and R is the radius of the device.

The transconductance g_m and drain conductance g_d are defined as

$$g_i = \left[\frac{dI_{ds}}{dV_{js}}\right]_{V_{ks}} \tag{22}$$

where, $i = m$ when $j = g$ & $k = d$

$i = d$ when $j = d$ & $k = g$

The capacitances C_{gs} gate-to-source and C_{gd} gate-to-drain [13] is defined as

$$C_{gj} = \frac{dQ_G}{dV_j} \tag{23}$$

where, j = d and s

Similarly

C_{ds} drain-to-source capacitance is defined as

$$C_{ds} = \frac{dQ_D}{dV_s} \tag{24}$$

where Q_G and Q_D is the charge stored in the gate region and drain region respectively and Q_G defined as

$$Q_G = -Q_{Tol} - Q_{ox} \tag{25}$$

Q_D calculated using Ward's channel charge partitioning scheme [14] where Q_{Tol} is the total inversion charge and Q_{ox} is the total oxide fixed charge at the oxide-silicon interface and can be neglected.

For short channel devices resistance R_i [15] is given as

$$R_i = \frac{L_g}{v_{sat} C_{gs}} \tag{26}$$

where, v_{sat} is saturation velocity of mobile electrons.

Transit time, τ is defined as the time taken by the electrons to cross the length of the channel in the velocity-saturated region and in general decides the speed of the device [16].

$$\tau = \frac{1}{2\pi f_t} \tag{27}$$

unity gain cut-off frequency f_t is the figure of merit and defined as the frequency at which the current gain (in dB) of the device becomes unity and is given as

$$f_t = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{28}$$

Substituting the above values from (22) to (28) in (9) (12) (15) and (18) to obtain the values of intrinsic Y-parameters. Conversion of Y-parameters into intrinsic S-parameters is done using [17]

$$S_{11} = \frac{(1 - Z_o Y_{11})(1 + Z_o Y_{22}) + Z_o{}^2 Y_{12} Y_{21}}{\nabla} \tag{29}$$

$$S_{12} = \frac{-2(Z_o Y_{12})}{\nabla} \tag{30}$$

$$S_{21} = \frac{-2(Z_o Y_{21})}{\nabla} \tag{31}$$

$$S_{22} = \frac{(1 + Z_o Y_{11})(1 - Z_o Y_{22}) + Z_o{}^2 Y_{12} Y_{21}}{\nabla} \tag{32}$$

where $$\nabla = (1 + Z_o Y_{11})(1 + Z_o Y_{22}) - Z_o{}^2 Y_{12} Y_{21} \tag{33}$$

and $Z_o = 50\Omega$, characteristics impedance at each port.

III. GAINS

Power gains play an important role in designing of an amplifier in microwave frequency range.

(1) **Unilateral Power gain (U_T)** is the maximum available power gain when the two-ports are simultaneously matched and the two feedback parameters have been neutralized.

Unilateral power Gain (U_T) is expressed as [18]

$$U_T = \frac{\frac{1}{2}\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{k\left|\frac{S_{21}}{S_{12}}\right| - \mathrm{Re}\left[\frac{S_{21}}{S_{12}}\right]} \tag{34}$$

k is stability factor defined as

$$k = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12} S_{21}|} \tag{35}$$

$$\Delta = S_{11} S_{22} - S_{12} S_{21} \tag{36}$$

This gain is the highest possible gain that can be achieved by an active port. The frequency where the unilateral gain becomes unity defines the boundary between an active and a passive network and is known as maximum frequency of oscillation.

It determines the stability of the device or its resistance to oscillations. [$k>1$] and [$\Delta<1$] forms the primary condition for the device to be stable. Higher is the frequency up to which the device is stable (i.e. $k>1$), more will be the device suitable for Low noise amplifier and RF applications.

(2) **Maximum Stable power gain (*Gms*)** [19, 20] given as

$$Gms = \frac{|S_{21}|}{|S_{12}|} \tag{37}$$

This is the gain that can be achieved by resistively loading the two-port such that the stability factor (k) is unity and then simultaneously matching the input and output ports. For conditionally stable two-ports, the maximum stable gain, *Gms* is an upper limit to power gain that can only be achieved when the input and output mismatch is reduced. If a simultaneous conjugate match is attempted, the two port will oscillate if k<1.

(3) **Maximum unilateral Transducer power gain ($G_{TU\max}$)** [18, 19] given as

$$G_{TU\max} = \frac{|S_{21}|^2}{\left(1-|S_{11}|^2\right)\left(1-|S_{22}|^2\right)} \tag{38}$$

IV. VERIFICATION WITH SIMULATED RESULTS AND DISCUSSION

In this section, the proposed intrinsic equivalent circuit model is used to extract the S-parameters and then the corresponding gains of CGT/SGT MOSFET. The analysis of CGT/SGT MOSFET has been carried out for a channel length L=50 nm, device radius R=10 nm, oxide thickness t_{ox}=2.5 nm, uniformly doped source/drain region, N_D^+ with doping density of $5x10^{19}$ cm^{-3}, P type substrate, N_A with a doping density of 10^{16} cm^{-3}, the metal gate work function (Φ_m) is 4.8 eV and drain-to-source voltage V_{ds}=0.5 V unless stated otherwise. The analytical results are compared with the simulated results of ATLAS 3D [21] at various gate biases and then compared with the bulk MOSFET at channel length L=50 nm, Width W=1 μm and gate oxide thickness t_{ox}=2.5 nm.

Fig. 3, 4, 5 and 6 show the variation S-parameters (S_{11} Input reflection coefficient, S_{12} Reverse transmission Coefficient, S_{21} Forward transmission Coefficient and S_{22} output reflection coefficient) both in real and imaginary form as a function of frequency ranging from 1 GHz to 1000 GHz range.

These parameters are calculated analytically using intrinsic equivalent circuit model and then compared with the results obtained from 3-D device simulation at V_{gs}=0.5 V & V_{gs}=1 V and a drain bias of V_{ds}=0.5 V. A good agreement is obtained between the simulated and analytical results for both the gate bias.

Fig. 3(a) and Fig. 3(b) show the variation of real and imaginary part of input reflection coefficient as a function of frequency respectively. And inset of both the figures shows the comparison between the bulk-MOSFET and CGT/SGT MOSFET in terms of real and imaginary input reflection coefficients.

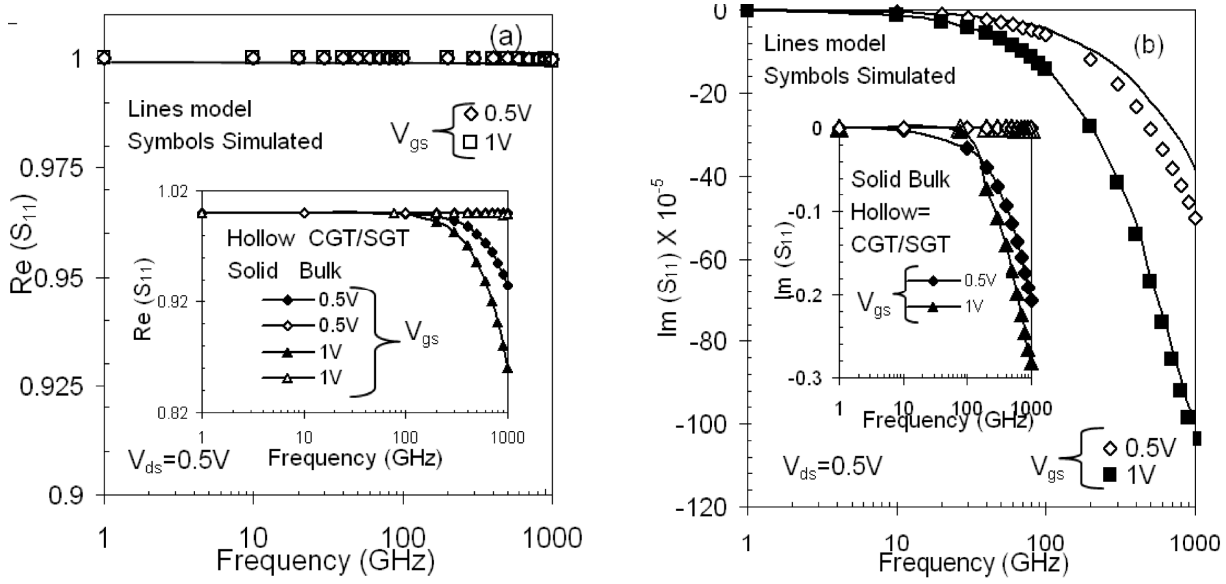

Fig. 3. (a) Real part of input reflection coefficient Re[S_{11}] as a function of frequency for CGT/SGT MOSFET. Inset graph compares Re[S_{11}] with respect to frequency for CGT/SGT and Bulk MOSFET. (b) Imaginary part of input reflection coefficient Im[S_{11}] as a function of frequency. Inset graph compares Im[S_{11}] with respect to frequency for CGT/SGT and Bulk MOSFET. At V_{gs}=0.5 V &1 V and V_{ds}=0.5 V.

From the inset figure it is observed that for CGT/SGT MOSFET the input reflection coefficient remains constant as compared to the bulk one. Which implies that due to the incorporation of cylindrical architecture the CGT/SGT MOSFET is better as compared to the bulk one.

Fig. 4(a) and Fig. 4(b) show the variation of real and imaginary part of Reverse transmission coefficient as a function of frequency. And inset of both the figures shows the comparison between the bulk-MOSFET and CGT/SGT MOSFET in terms of real and imaginary reverse transmission coefficients. From the figure it is analyzed that reverse transmission coefficient for CGT/SGT MOSFET is very less as compared to bulk one, which is most desirable for better device performances. And a good matching between the analytical and simulated data validates the model.

Fig. 5(a) and Fig. 5(b) show the variation of real and imaginary part of Forward transmission coefficient with respect to frequency. And inset of both the figures shows the comparison between the bulk-MOSFET and CGT/SGT MOSFET in terms of real and imaginary forward transmission coefficient as a function of frequency. From the figure a perfect matching between the model and simulated data validates the model.

Fig. 6(a) and Fig. 6(b) show the variation of real and imaginary part of output reflection coefficient as a function of frequency. And the inset of both the figures show the comparison between the bulk-MOSFET and CGT/SGT MOSFET in terms of real and imaginary output reflection coefficient. And CGT/SGT MOSFET output reflection coefficient keeps on decreasing as compared to bulk MOSFET, which is most desirable.

Fig. 7 shows the variation of Unilateral power gain (U_T) as a function of frequency upto 1 THz, at a constant drain bias V_{ds}=0.5 V and gate bias of V_{gs}=0.5 V & V_{gs}=1 V. It is defined as the highest possible gain that an active port can achieve. The manufacturers commonly know this as high power high gain capability of the device. Unilateral power gain is obtained using Eq. (34). From the figure, it is observed that there is an exponential decrease in the unilateral power gain as the frequency increases. By extrapolating the curve of unilateral power gain f_{max} is obtained, which comes out to be around 250 GHz. f_{max} is known as the maximum frequency of oscillation at which unilateral power gain become unity or 1dB. A good matching between the simulated results with the analytical data validates the model.

Fig. 8 indicates the variation of Maximum stable power gain (*Gms*) with respect to frequency upto 1 THz. *Gms* is a figure of merit (FOM) defined as highest value of power-gain, achieved before the instability is occurred,

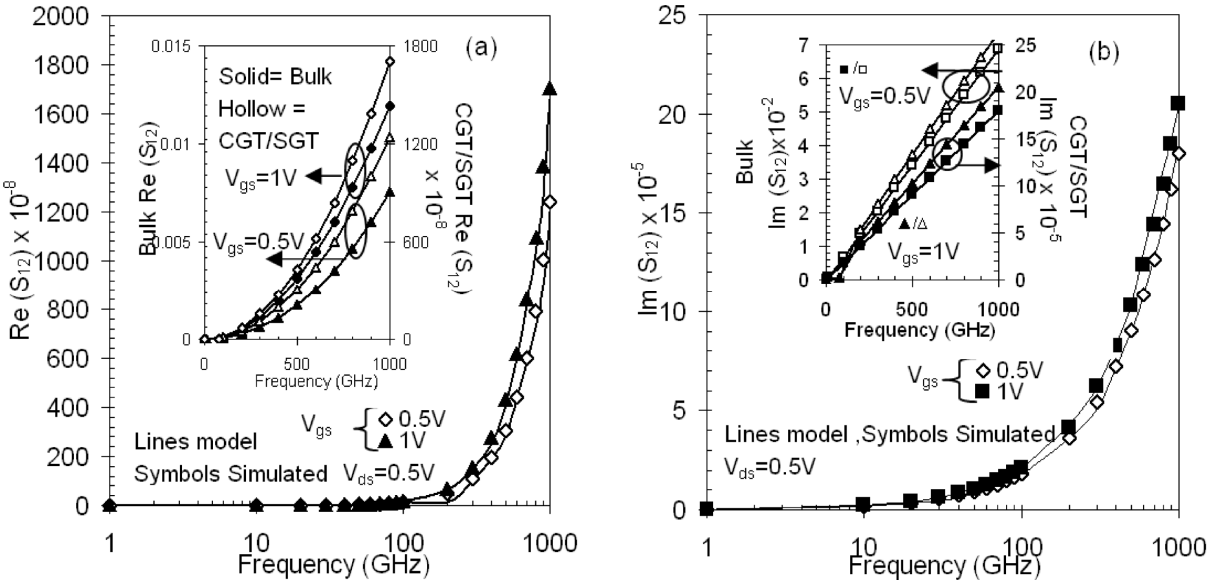

Fig. 4. (a) Real part of Reverse transmission coefficient Re[S_{12}] as a function of frequency for CGT/SGT MOSFET. Inset graph compares Re[S_{12}] with respect to frequency for CGT/SGT and Bulk MOSFET, (b) Imaginary part of reverse transmission coefficient Im[S_{12}] as a function of frequency. Inset graph compares Im[S_{12}] with respect to frequency for CGT/SGT and Bulk MOSFET. At V_{gs}=0.5V &1 V and V_{ds}=0.5 V.

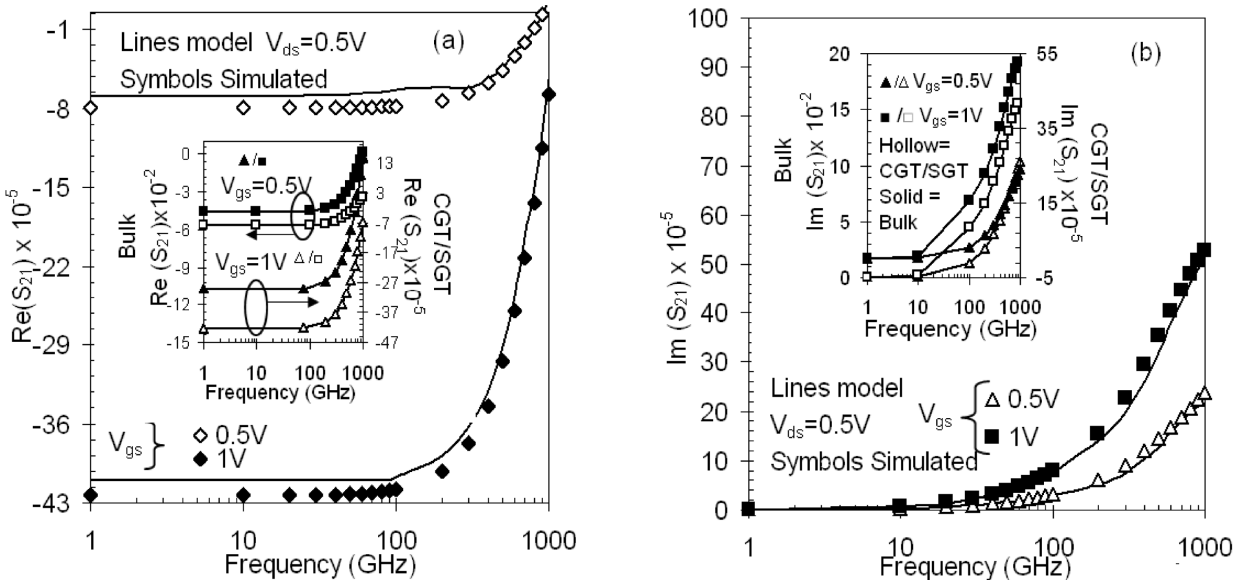

Fig. 5. (a) Real part of forward transmission coefficient Re[S_{21}] as a function of frequency for CGT/SGT MOSFET. Inset graph compares Re[S_{21}] with respect to frequency for CGT/SGT and Bulk MOSFET, (b) Imaginary part of forward transmission coefficient Im[S_{21}] as a function of frequency. Inset graph compares Im[S_{21}] with respect to frequency for CGT/SGT and Bulk MOSFET. At V_{gs}=0.5 V & 1 V and V_{ds}=0.5 V.

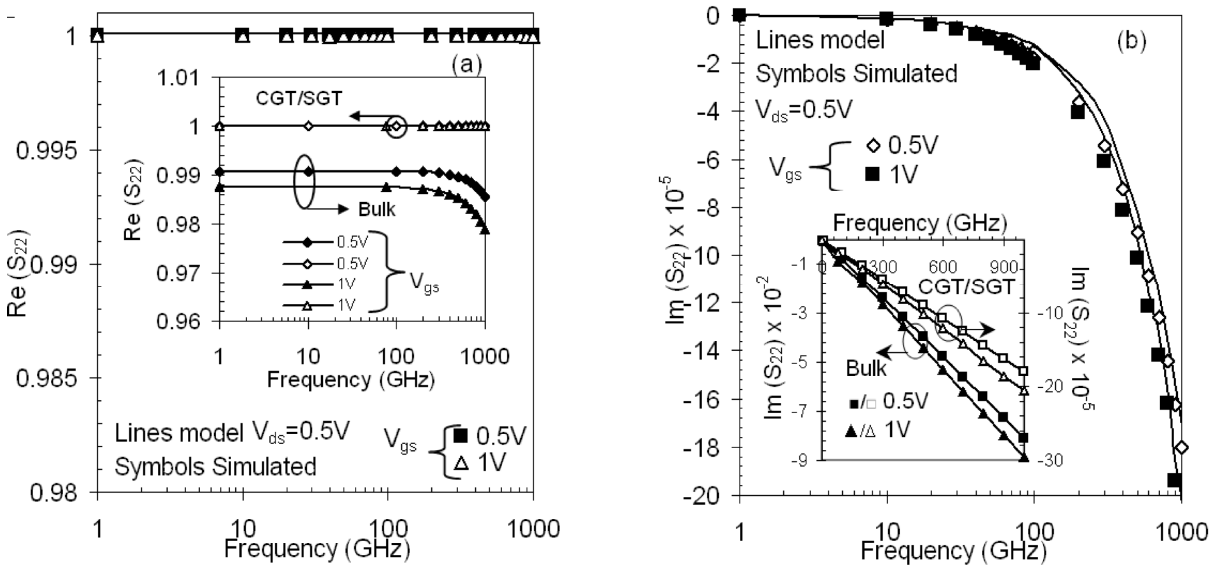

Fig. 6. (a) Real part of output reflection coefficient Re[S_{22}] as a function of frequency for CGT/SGT MOSFET. Inset graph compares Re[S_{22}] with respect to frequency for CGT/SGT and Bulk MOSFET, (b) Imaginary part of output reflection coefficient Im[S_{22}] as a function of frequency. Inset graph compares [ImS_{22}] with respect to frequency for CGT/SGT and Bulk MOSFET. At V_{gs}=0.5 V & 1 V and V_{ds}=0.5 V.

i.e., at *k=1*. Maximum stable power gain, *Gms* is an important parameter used for low noise amplifier designing (LNA). The maximum stable power gain, *Gms* predicts the input and output mismatch, and it is found that, as the frequency increases, the input and output mismatch decreases. Thus, a simultaneous conjugate match has been obtained in the analysis. A good agreement between the analytical model and simulated data is obtained.

Fig. 9 anticipates the variation of Maximum unilateral Transducer power gain (G_{TUmax}) as function of frequency upto 1 THz range. It is obtained when the source and the load reflection coefficient are so adjusted that $\Gamma_g = S_{11}^*$ and $\Gamma_L = S_{22}^*$ and the Maximum

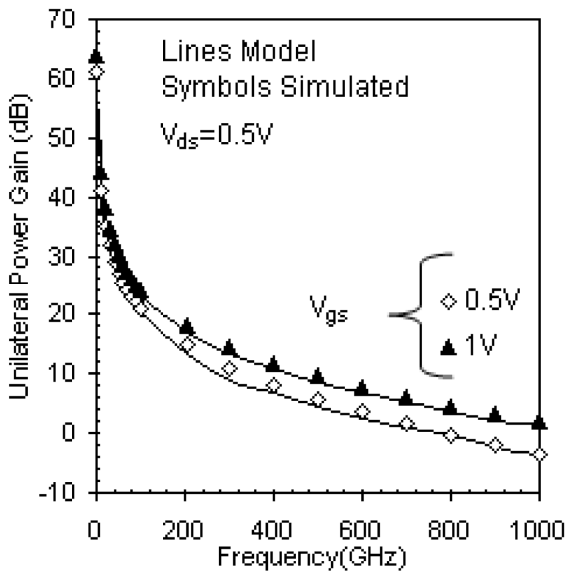

Fig. 7. Variation of Unilateral Power gain (U_T) (in dB) as a function of frequency.

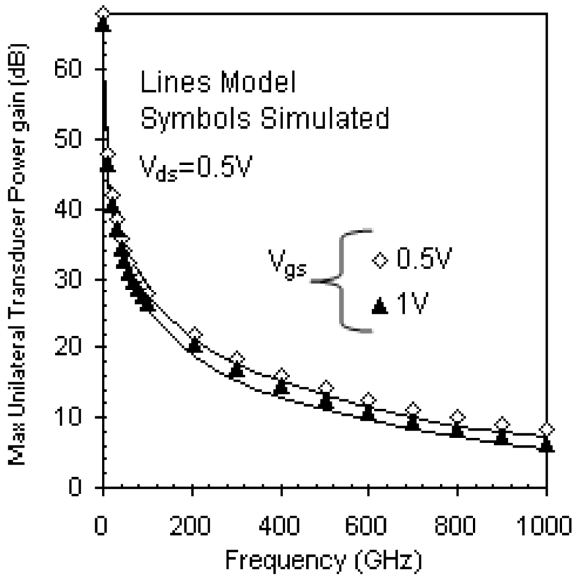

Fig. 9. Variation of Maximum unilateral transducer power gain (G_{TUmax}) (in dB) as a function of Frequency.

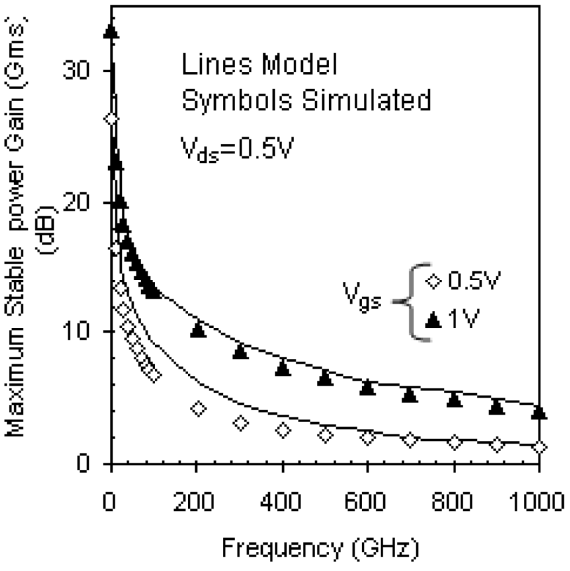

Fig. 8. Variation of Maximum Stable power gain (*Gms*) (in dB) as a function of frequency.

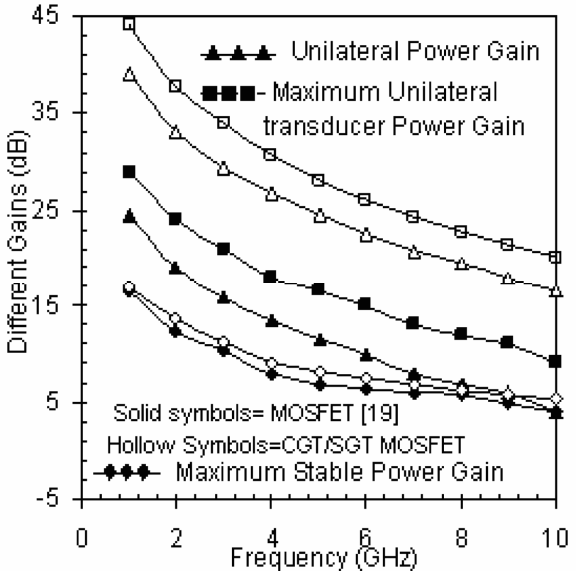

Fig. 10. Variation of different gains with frequency for both MOSFET and CGT/SGT MOSFET at L= 0.8 μm and V_{ds}=3 V.

Unilateral Transducer Power Gain (G_{TUmax}) is obtained. This is given by the Eq. (38). Analytical results closely matched with simulated results, which validate the model.

Fig. 10 predicts the variation of different gain namely unilateral power gain, Maximum Unilateral transducer power gain and maximum stable gain as a function of frequency for both MOSFET and CGT/SGT MOSFET at L=0.8 μm. From the figure, it can be analyzed that all the gains are increasing for CGT/SGT MOSFET as compare to bulk MOSFET, this is only because of the better gate controllability by the Cylindrical/Surrounded architecture results improvement of different gains. Hence, CGT/SGT MOSFET device is useful for microwave frequency applications.

V. CONCLUSIONS

An intrinsic circuit model for CGT/SGT MOSFET has been proposed from where microwave characteristics in terms of scattering parameters (S_{11} Input reflection

coefficient, S_{12} Reverse transmission Coefficient, S_{21} Forward transmission Coefficient and S_{22} output reflection coefficient) and power gains in terms of unilateral power gain, Maximum Unilateral transducer power gain and maximum stable gain have been obtained. The model results so obtained are then compared with bulk MOSFET. And found that CGT/SGT device has better device performance in terms of S parameters. Also the results show that the circuit is useful in microwave applications. This circuit can be used for high frequency performances and to improve the device performance through proper designing and optimization of the structure itself. Improvement in the CGT/SGT MOSFET as compared to bulk MOSFETs concluded that cylindrical /surrounded architecture has a better gate control as compared to bulk MOSFET. Calculated modeled results of S parameters are found to be in good agreement with the results obtained from the 3D device simulator in the tera-hertz frequency range and which validates the model.

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Pujarini Ghosh was born in Assam, India, in 1985. She received the B.A Sc (H) Electronic Science from University of Delhi and M.Sc. Electronics from Jadavpur University in the year 2006 and 2008 respectively. Her doctoral Research involves the modeling design and simulation of gate material engineered Surrounded /Cylindrical Gate MOSFET for RF IC applications. She is currently working as University Teaching Assistant (UTA), University of Delhi. Currently she has authored 14 international journals and international conference proceedings. Her other areas of interest and activities cover VHDL and P Spice implementation.

Subhasis Haldar was born in India in 1967. He received the B. Sc (Hon.) and M. Sc degrees both in physics and the Ph.D Degree in electronics from University of Delhi. In 1988, 1990 and 1995 respectively. He joined the SDRL , Department of electronic Science, University of Delhi, South Campus in 1991 and developed analytical models of both MOSFET and MESFET devices. HE joined Moti Lal Nehru College, University of Delhi in 1993 as a lecturer and is now associate professor. Currently his area of interest is in miniaturization of devices, study and suppression of hot carrier effects considering LDD and FOLD structures, single and double gate MOSFET, Surrounded/Cylindrical gate MOSFET and poly silicon. Currently he has 175 technical papers published in various journals and conference proceedings. Dr. Haldar was a member of ISRAMT'93, APMC 2004 and ISMOT 2009. He was joint secretary of APMC'96.

R. S. Gupta received B Sc. and M Sc. degrees from Agra University India in 1963 and 1966 respectively and the Ph.D. degree in electronic engineering from the Institute of Technology, Banaras Hindu University, Varanasi, India, in 1970. In 1971, he was with Ramjas College, University of Delhi, Delhi, India. In 1987, he was with the Department of Electronic Science, University of Delhi South Campus, New Delhi, India, as a Reader and later as a Professor from 1997 to 2008, later he was an Emeritus Scientist and with the Semiconductor Devices Research Laboratory. Currently is with Maharaja Agrasen Institute of Technology He heads several major research projects sponsored by the Ministry of Defence, the Department of Science and Technology, the Council of Science, and the Industrial Research and University Grants Commission. In 1988, he was a Visitor with the University of Sheffield, Sheffield, U.K., under the ALIS Link exchange program and also visited several U.S. and Spanish universities in 1995 and 1999, respectively. He also visited the Czech Republic in August 2003; Korea in November 2003; RPI Troy, NY, in August 2004, and China in December 2005. He has authored or coauthored

over 580 papers in various international and national journals and conference proceedings. He contributed the chapter entitled "MOSFET Modeling" in the Encyclopedia on RF and Microwave Engineering (Wiley, 2005). He has supervised 46 Ph.D. students. His current interests and activities cover modeling of SOI submicrometer MOSFETs and LDD MOSFETs, modeling and design of HEMTs, hot-carrier effects in MOSFETs, and modeling of GaAs MESFETs for high-performance microwave and millimeter-wave circuits and quantum effect devices. Dr. Gupta was an Executive Member of the IEEE Electron Devices (ED)/ Microwave Theory and Techniques (MTT) Chapter India Council. His name has also appeared in the Golden List of IEEE TRANSACTIONS ON ELECTRON DEVICES in December 1998, 2002, and 2004. He is a Fellow of the Institution of Electronics and Telecommunication Engineers (India), a Life Member of the Indian Chapter of the International Centre for Theoretical Physics (ICTP), and a Life Member of the Semiconductor Society of India. He was the Secretary of ISRAMT'93 and the 1996 Asia-Pacific Microwave Conference (APMC'96), and the Chairman of the Technical Programme Committee of APMC'96. He edited the proceedings of both of these international conferences. He was the Chairman of APMC'2004, held in New Delhi, India, in December 2004.

Mridula Gupta received the B.Sc. degree in physics, the M.Sc. degree in electronics, the M.Tech. degree in microwave electronics, and the Ph.D. degree in optoelectronics from the University of Delhi, Delhi, India, in 1984, 1986, 1988, and 1998, respectively. Since 1989, she has been with the Department of Electronic Science, University of Delhi South Campus, New Delhi, India, where she was previously a Lecturer and is currently an Associate Professor and with the Semiconductor Devices Research Laboratory. She has authored or coauthored approximately 312 publications in international and national journals and conference proceedings. She has supervised 14 Ph.D. students. She contributed the chapter entitled "MOSFET Modeling" in the Encyclopedia on RF and Microwave Engineering (Wiley, 2005). Her current research interests include modeling and simulation of MOSFETs, MESFETs, and HEMTs for microwave-frequency applications. Dr. Gupta is a Fellow of the Institution of Electronics and Telecommunication Engineers (India) and a Life Member of the Semiconductor Society of India. She was the Secretary of the 2004 Asia–Pacific Microwave Conference, and was General Secretary of 12th ISMOT 2009 which were held in New Delhi, India.