A Design of Vernier Coarse-Fine Time-to-Digital Converter using Single Time Amplifier

Jongsuk Lee and Yong Moon

Abstract—**A Coarse-Fine Time-to-Digital Converter (TDC) using the single time amplifier is proposed. A vernier delay line is used to overcome process dependency and the 2-stage time amplifier is designed to have high resolution by increasing the gain of the time amplifier. Single time amplifier architecture reduces the silicon area of the TDC and alleviates mismatch effect between time amplifiers. The proposed TDC is implemented in 0.18 μm CMOS process with the supply voltage of 1.8 V. The measured results show that the resolution of the TDC is 0.73 ps with 10-bit digital output, although high-end process is not applied. The single time amplifier architecture reduces 13% of chip area compared to previous work. By reducing the supply voltage, the linearity of the TDC is enhanced and the resolution is decreased to 1.45 ps.**

Index Terms—**Time-to-digital converter (TDC), time amplifier, vernier, coarse-fine architecture**

I. INTRODUCTION

Phase-locked loop (PLL) is an important component in communication, radar and so on [1]. Nowadays All-Digital PLL (ADPLL) has been researched widely to replace conventional analog PLL, because it is free from large loop filter, leakage and matching. ADPLL has advantages in area because it does not use passive element, and shows fast locking time and has easy scalability to process shrinking. Time-to-Digital Converter (TDC) in ADPLL replaces phase detector and charge pump and play a role to convert time difference of two signals into digital bits [2]. TDC is often used in high speed communication system based on PLL and affects the resolution of ADPLL and noise performance, so a high performance TDC is required more and more [3-5]. TDC is currently an important topic in mixed-signal circuits and several architectures are proposed like flash TDCs, pipelined TDCs and SAR-TDCs. The pipelined TDC using time amplification method has advantages in sub-gate-delay resolution, but it requires large area, high-end process and has mismatch problem.

In this paper, we focus on a high performance TDC for ADPLLs, and propose the single time amplifier method to reduce area and mismatch. A vernier delay line is used to reduce the dependency on process and the 2-stage time amplification method is also proposed to increase the resolution of the TDC and the linearity of the time amplifier.

This paper is organized as follows. The architecture and scheme of the proposed TDC are described in Section II. Section III describes the implementation of critical building blocks of the TDC. The simulation and measurement results are given in Section IV, and conclusions are drawn in Section V.

II. TDC ARCHITECTURE

Fig. 1 shows the block diagram of the proposed vernier single time amplifier Coarse-Fine TDC, and resolution is 10-bit which is composed of the 5-bit Coarse TDC and the 5-bit Fine TDC. Two Fine TDCs are used to correct errors due to the time amplification, but

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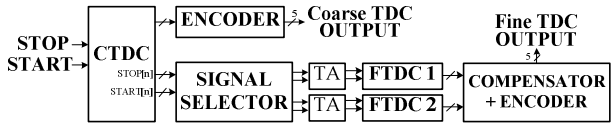

Fig. 1. Block diagram of the proposed vernier single time amplifier Coarse-Fine TDC.

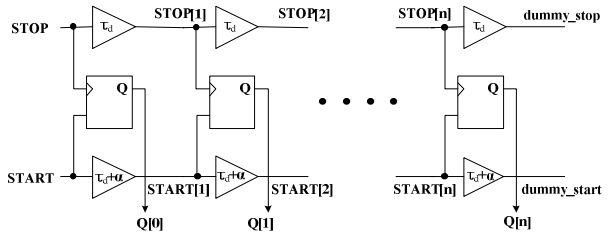

Fig. 1. Vernier delay line for the TDC.

each Fine TDC uses only one time amplifier. This architecture reduces layout area about 13% in total TDC area compared to the previous work which uses many time amplifiers proportional to the number of delay buffers [2]. The previous architecture requires 32(=2^5) time amplifiers, if we want 5-bit resolution. And the single time amplifier architecture also reduces mismatch problems among time amplifiers.

The vernier delay line which is shown in Fig. 2 is used in this work. It is preferred not to use a vernier delay line for reducing the mismatch of the delay buffer, but buffer delay is limited by process [1]. However vernier delay line is the only way to overcome the buffer delay limitation, so the vernier delay line method is adapted in this design to consider that PLL is widely used not only in state-of-the-art process but in many general processes [6].

As mentioned in previous works, the problem of vernier delay line method is mismatch and large number of buffer stages. So we add dummy inverters each stage and use the time amplification method to limit the number of buffer stages. In our study, the rising and falling characteristics of upper and lower delay line is somewhat different, so it could cause wrong conversion in the Coarse TDC. So we add the lower inverter as dummy to the upper inverter, and the upper inverter as dummy to the lower inverter. The dummy inverters waste some silicon area, but this area is not large and we could get good rising/falling characteristics to amplify the time interval of two input signals. The vernier delay line is used in the Coarse TDC, so the time resolution of the Coarse TDC is:

$$\text{Resolution} = (\tau_d+\alpha) - \tau_d = \alpha \qquad (1)$$

We could get and control the time resolution of the Coarse TDC using the vernier delay line independent of process. And 10 ps resolution is used in this design to consider area and time amplification.

III. CIRCUIT DESCRIPTION

1. Vernier Time Amplifier

The previous time amplifier in TDCs uses different NAND gate and metastability [2]. We use the same architectures to amplify time interval. The previous time amplifier shows good amplification characteristics in small time interval, but it requires small gate delay and does not guarantee correct operation to amplify large time interval.

But the gate delay is dependent on process, so we also adopted vernier method in the time amplifier. The vernier time amplifier used in this work is shown in Fig. 3.

We could get small time delay using vernier method, so the dependency on process is alleviated. But some verification steps should be done after layout to check its operation.

The time amplifier gain is decided by the delay of gate before SR latch, and the gain limits the resolution of TDCs. The delay of gate is replaced by the delay difference of two gates using vernier method. But this approach does not guarantee the linearity and the gain of the time amplifier. We use 2-stage time amplification method to increase gain and widen the input range of the

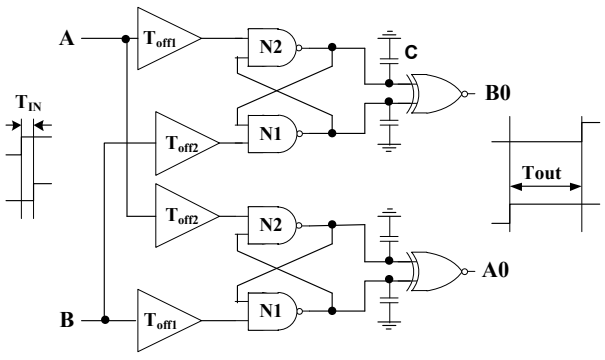

Fig. 3. Vernier time amplifier.

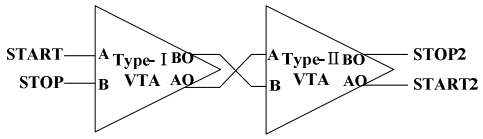

Fig. 4. Block diagram of the 2-stage vernier time amplifier.

time amplifier with good linearity. It is difficult to obtain the gain of 32 by a single-stage time amplifier. Even if we get the gain over 32 using a single-stage time amplifier, but the linearity of the time amplifier is poor to use in TDCs. But the gain over 32 is mandatory, if we want 5-bit resolution in the Fine TDC. So we use the 2-stage time amplification method to meet the gain value and linearity. Fig. 4 shows the block diagram of the 2-stage time amplifier used in the proposed TDC.

The proposed 2-stage time amplifier consists of two different time amplifier. The Type-I time amplifier used in the first stage has small input range with large gain and the Type-II amplifier used in the second stage has larger input range and smaller gain compared to the Type-I amplifier. The gain of the Type-I amplifier is around 20 and the gain of the Type-II is around 2. So the total gain is about 40 using the 2-stage structure.

If the gain of TA is not large, single-stage TA is better than 2-stage TA in terms of gain error. Because the gain error of 2-stage TA is the multiplication of each stage. But if the gain of TA is large, 2-stage TA is better than single-stage TA in gain linearity. Because when the time interval of two input signals increases, the nonlinearity of single-stage TA increases. The gain error of the 2-stage TA is corrected in the Compensator block.

2. Coarse TDC

As shown in Fig. 1, the two input signals (START, STOP) which have the time interval between each other enter the Coarse TDC. Two signals pass different delay lines which compose the vernier delay line and the interval is reduced by 10 ps after passing one delay stage. The leading and lagging characteristics of two input signal is inverted at some stage of the vernier delay line. If this happens at [n+1] stage, the time interval of two signal is lower than 10ps at n-stage. So one of MUXs selects START[n] and STOP[n] as shown in Fig. 2 to amplify in the 2-stage time amplifier. The input signals of the 2-stage time amplifier which have small time difference less than 10 ps are amplified and go in the Fine TDC. The schematic of the Coarse TDC is shown in Fig. 5.

The total number of delay stages is 31 to obtain 5-bit resolution in the Coarse TDC. The time difference of the vernier delay line is 10 ps, and this value is realized to vary the width of the delay buffers for START and STOP signal. The dummy gates with different width are attached output of delay stage to match the characteristics of rising/falling, and the loading effect of the Flip-Flop is considered. The parasitic capacitance due to layout is also considered. The input range of the proposed TDC is 320 ps, because of the number of the vernier delay line buffers. The input range could be increased, if we add more delay buffers in the delay line. But this value is decided by system, so we use 5-bit in this design.

3. Signal Selector

The structure of a Signal Selector is important, because it plays a major role to reduce the number of time amplifiers in TDCs. The schematic of the Signal Selector is shown in Fig. 6.

We add the Delay Stage block to use the single time amplifier, because the signals to be amplified are

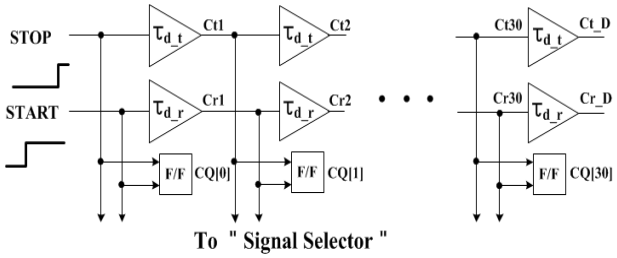

Fig. 5. Schematic of the 5-bit Coarse TDC.

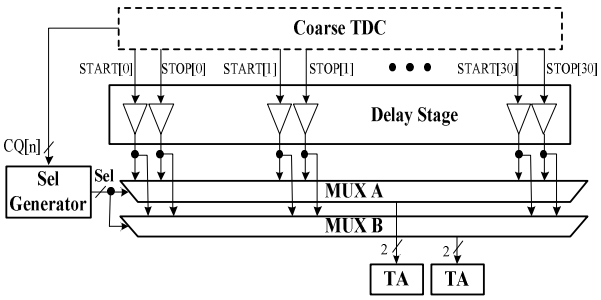

Fig. 6. Schematic of the Signal Selector.

somewhat earlier than "Sel" signal which is generated by "Sel Generator" using the outputs of the Flip-Flop's which are used in the Coarse TDC. The signals to be amplified are close to zero-second pass the MUXs, and the outputs of the MUXs go in the 2-stage time amplifier. This method also generates mismatch problem in the Delay Stage and the MUXs, but we think that this effect is lower than the mismatch problem caused by using many time amplifiers. And it also reduces the silicon area a lot.

4. Fine TDC

The output of time amplifier is the input of the Fine TDC (FTDC), but the gain of the time amplifier is not fixed to the desired value. The expected gain of the time amplifier is 32, but it is very difficult to maintain this value. So we design the Fine TDC as 7-bit resolution to compensate the error of the time amplifier. The block diagram of the Fine TDC is shown in Fig. 7.

The Fine TDC needs two converting blocks to know the exact gain of the time amplifier and this value is used in the Compensation block. Each converting block has two vernier lines to calculate a positive value and a negative value when the interval of two input signal is very small or shows some offset. But cases which generate negative value are rare [2], so the number of delay stages for the negative gain is smaller compared to the positive gain calculation. 7-bit for positive quantization and 5-bit for negative quantization could reduce the burden of delay stages in the Fine TDC. The gain of the time amplifier is over 32 in general, so 2-bit resolution increment in the Fine TDC is adequate.

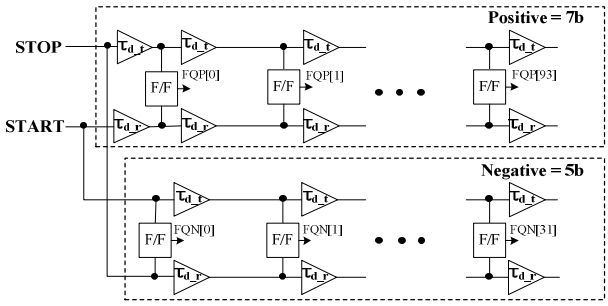

Fig. 7. Block diagram of the Fine TDC.

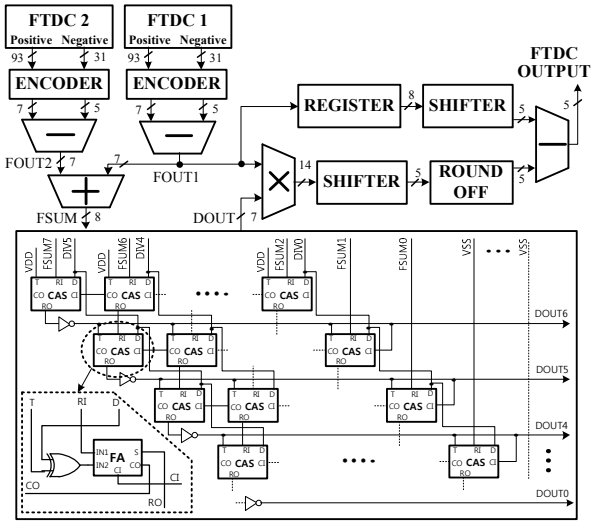

Fig. 8. Block diagram of the Compensator.

5. Compensator

The block diagram of the Compensator is shown in Fig. 8.

The major problem of the time amplification TDC is the gain nonlinearity of time amplifiers. So the 7-bit Fine TDC and the Compensator block are used to overcome this problem.

And the second problem of the vernier time amplifier is offset. The proposed TDC calculates offset by entering the same signal to START and STOP input, and the digital output of the TDC is stored in the register which has 8-bit storage. The stored digital value when the input has no time difference is subtracted from the round-off value of the Fine TDC. So the final digital output of the Fine TDC is determined.

IV. MEASUREMENT RESULTS

The proposed TDC was fabricated in 0.18 μm CMOS process. The vernier 2-stage time amplifier is simulated to check input range and total gain. The simulation results of the vernier time amplifier is shown in Fig. 9.

"TO" shows the characteristics of the Type-I time amplifier in Fig. 9(a). "TO2" shows the input-output characteristic of the 2-stage vernier time amplifier. Fig. 9(b) shows the total gain according to input time interval. If the input interval is less than 10 ps, the linearity of the time amplifier is appropriate. And we could know the total gain of the 2-stage time amplifier is over 32. The

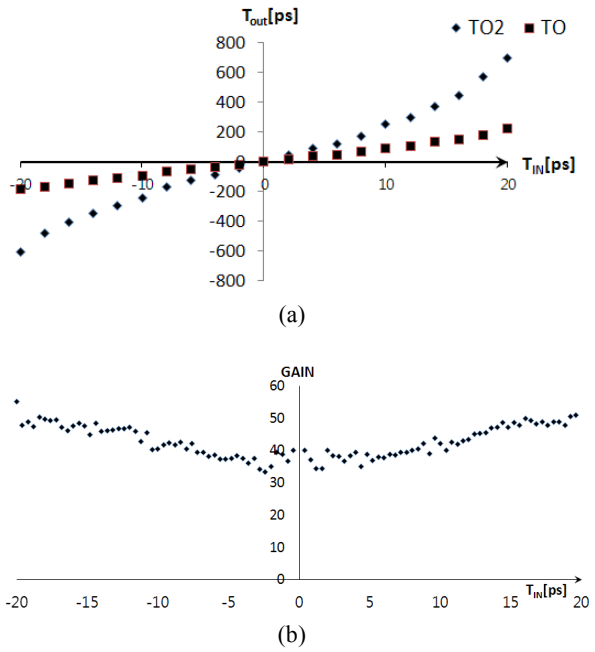

Fig. 9. (a) The output of the time amplifier vs. input interval, (b) Simulation of the 2-stage time amplifier gain distribution.

Table 1. Simulated results of the Fine TDC correction circuit

T_{IN}(ps)	FTDC1 (7bit)		FTDC2 (7bit)		FTDC OUTPUT (5bit)	
0	1111111	-1	0101011	43	00000	0
0.875	0000010	2	0100101	37	00010	2
1.75	0000110	6	0100000	32	00101	5
2.625	0001001	9	0011100	28	01000	8
3.5	0001100	12	0011000	24	01010	10
4.375	0010000	16	0010100	20	01101	13
5.25	0010011	19	0010001	17	10000	16
6.125	0010111	23	0001110	14	10011	19
7	0011010	26	0001010	10	10110	22
7.875	0011111	31	0000111	7	11001	25
8.75	0100011	35	0000100	4	11100	28
9.625	0101000	40	0000001	1	11111	31

error due to gain variation is compensated by the Compensator, and its simulated results are shown in Table 1. The compensated output is drawn in Fig. 10.

The implemented Vernier Single Time Amplifier TDC is measured using test board. Input signal is generated by Function Generator, and digital outputs are monitored by a Logic Analyzer and analog signals are measured by an Oscilloscope. Fig. 11 shows the photograph of fabricated chip. The rectangular area of the TDC is 2.1 ㎜×0.8 ㎜ (1.68 ㎟), but the area used by circuit is about 0.82 ㎟.

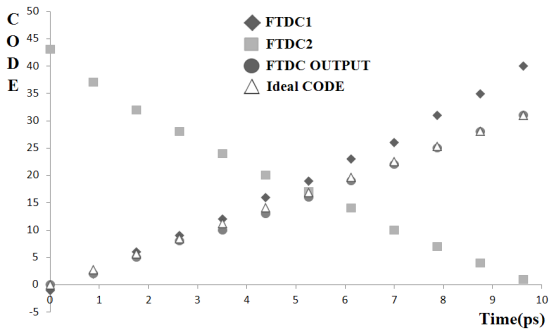

Fig. 10. Correction operation for the FTDC in compensator.

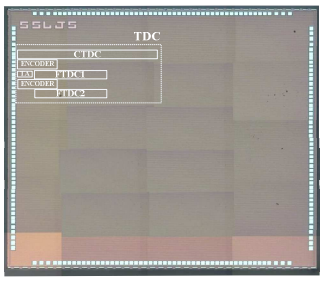

Fig. 11. The photograph of the fabricated TDC.

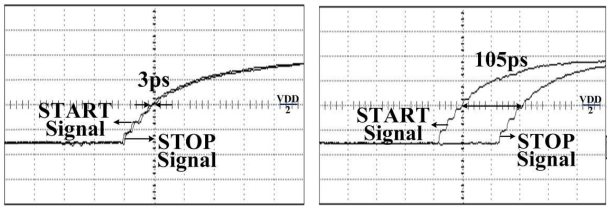

Fig. 12. (a) The input signals of the time amplifier, (b) The output signals of the time amplifier.

The supply voltage is 1.8 V and 3.3 V supply is used for digital interface. The additional time amplifier block is implemented solely to check the operation. Fig. 12 shows the captured images of the oscilloscope which show the input and output signals of the 2-stage time amplifier.

Fig. 13 shows the digital outputs of the TDC according to input interval.

The measured results show that the resolution of 0.73 ps is obtained. This value is somewhat larger than simulation because process variation is involved in fabrication. And we change the supply to check the effect of the delay lines. Fig. 14 shows the output code of the measured TDC results according to input interval, when we change the supply voltage from 1.8 V to 1.6 V. Plot

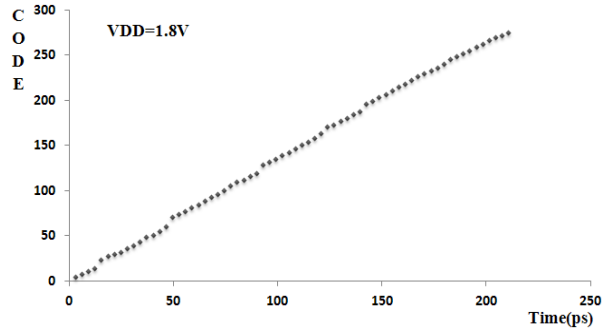

Fig. 13. The measured digital code of the TDC.

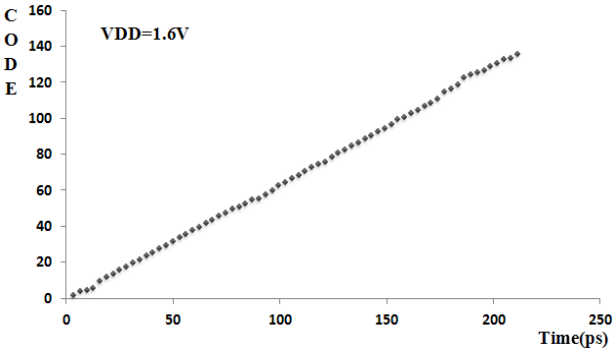

Fig. 14. Measured results of the TDC at reduced supply.

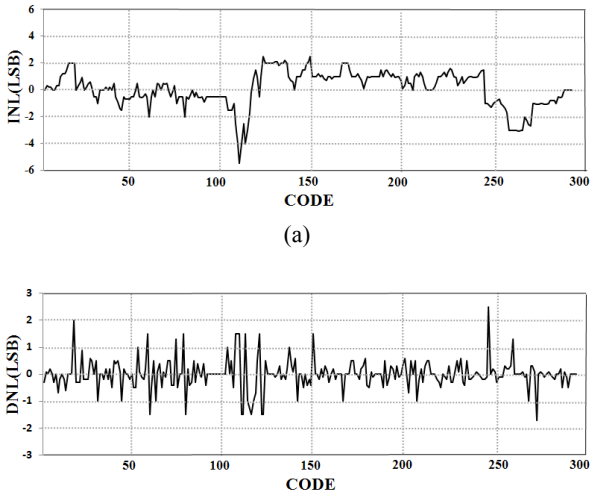

Fig. 15. (a) Measured INL, (b) Measured DNL.

shows that the linearity is improved but the resolution is deteriorated as expected.

The resolution of the TDC is reduced to 1.45 ps, but the linearity is somewhat improved. The power consumption of the TDC is 2.8 ㎽ excluding the power dissipated by PADs at 1.6 V supply. The measured outputs already include offset compensation.

Table 2. The performance summary and comparisons

	[2]JSSC 2007	[7]JSSC 2009	[8]DDECS 2010	[9]ISSCC 2011	This work
Process	90 ㎚ CMOS	0.18 ㎛ CMOS	90 ㎚ CMOS	0.13 ㎛ CMOS	0.18 ㎛ CMOS
Resolution	1.25 ps	6 ps	6.8 ps	10.5 ps	0.73 ps /1.45 ps
Time Amplifier Gain	> 16	N/A	> 4	N/A	> 32
Input Range	640 ps	20 ns	12 ps~ 9.5 ns	20 ns	320 ps
Input Frequency	10 MHz	1 MHz	105 MHz	5 MHz	1 MHz
Area	0.6 ㎟	0.04 ㎟	N/A	0.11 ㎟	1.68 ㎟
Power Consumption	3 ㎽	2.2~ 21 ㎽	0.24 ㎽	1.7 ㎽	2.8 ㎽
Supply	1 V	1.5 V	0.5 V	1.2 V	1.8 V /1.6 V

Fig. 15 shows INL and DNL from measured results at 1.6 V supply. The INL is ±5.2LSB and DNL is ±2.4LSB.

Finally, Table 2 summarized the performance comparison between the proposed work and recently reported TDCs.

V. CONCLUSIONS

The 10-bit Vernier Coarse-Fine Time-to-Digital Converter using single time amplifier is proposed and designed in 0.18 ㎛ CMOS process. The 2-stage vernier time amplifier method is used to improve the linearity of time amplifier and secure high gain over 32. The vernier architecture reduces the dependency on process, so sub-ps resolution is obtained although 0.18 ㎛ CMOS process is used. The proposed single time amplifier structure reduces layout area about 13% in total TDC area. The measured results show the resolution of 0.73 ps and 1.45 ps is obtained according to supply voltages and the feasibility of the proposed chip.

The proposed TDC could increase the popularity of ADPLL and could be used in various processes.

ACKNOWLEDGMENTS

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