A Fully-Integrated Low Power K-band Radar Transceiver in 130nm CMOS Technology

Seong-Kyun Kim, Chenglin Cui, Byung-Sung Kim, and SoYoung Kim

Abstract—**A fully-integrated low power K-band radar transceiver in 130 nm CMOS process is presented. It consists of a low-noise amplifier (LNA), a down-conversion mixer, a power amplifier (PA), and a frequency synthesizer with injection locked buffer for driving mixer and PA. The receiver front-end provides a conversion gain of 19 dB. The LNA achieves a power gain of 15 dB and noise figure of 5.4 dB, and the PA has an output power of 9 dBm. The phase noise of VCO is -90 dBc/Hz at 1-MHz offset. The total dc power dissipation of the transceiver is 142 mW and the size of the chip is only 1.2 × 1.4 mm^2.**

Index Terms—**CMOS integrated circuit, k-band, millimeter-wave, radar, transceiver, low-noise amplifier, power amplifier**

I. INTRODUCTION

The car radar sensor is known to be a most effective way to avoid critical traffic accidents and assist driving convenience. Compared to other radars used in aerospace and military systems, car radar sensors should have small volume and consume low power. More importantly, low cost implementation is essential to be equipped even in compact cars. A frequency modulated continuous-wave (FMCW) radar is a good candidate for adaptive cruise control (ACC), lane change assist (LCA) and Stop-and-Go system [1, 2]. Recent development of the long range radar system has moved to W-band around 77-GHz, but the cost issue does not seem to be easily solved due to high costs for IC fabrication, packaging and testing. Considering manufacturing costs, the radar sensors using 24-GHz ISM band can still be a viable alternative at the expense of the detection range. In addition, K-band radar transceiver can be used for various applications in security and industry. K-band radar transceiver circuits have been already reported using SiGe technologies [3, 4]. However, considering the level of integration, power consumption, manufacturing cost for mass production, the CMOS technology seems to be more competitive than other technologies for 24-GHz ISM band applications because successful design results have been reported using matured 0.13 μm technology [5, 6]. Though the 0.13 μm CMOS technology shows the maximum operating frequency around 80-GHz, it is still challenging to design a low power transceiver for 24-GHz applications to meet the gain and power specifications. Therefore, this work utilizes gain boosting technique in the receiver design and adopts injection locked buffer as a PA driver, which enables the low power operation and chip size reduction.

This paper is organized as follows. Section II presents the transceiver architecture and its building blocks. Section III shows the experimental results. Finally, Section IV concludes this work.

II. TRANSCEIVER DESIGN

The transceiver architecture is shown in Fig. 1, which includes receiver, transmitter, voltage controlled oscillator, and integer-N phase-locked loop (PLL). The reference clock (f_{ref}) is generated by an external direct digital frequency synthesizer (DDFS) to create a

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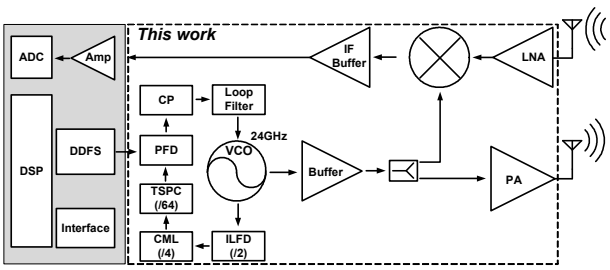


Fig. 1. FMCW radar transceiver architecture.

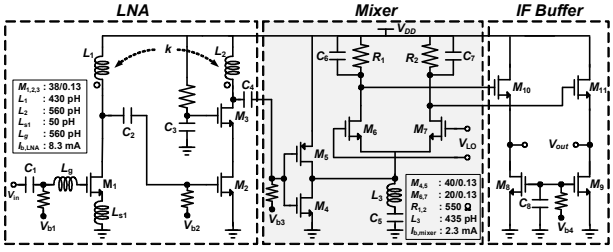


Fig. 2. Schematic of receiver.

frequency modulation signal. The PLL loop bandwidth is set to 1 MHz to improve the output chirp linearity of the PLL and suppress the spurs [7].

1. Receiver

Fig. 2 shows the schematic of the receiver which includes LNA for amplification of the received signal from the antenna with low noise and mixer for frequency down-conversion. The LNA consists of two stages. The first stage adopts the common source (CS) configuration to improve noise figure and the second stage uses a cascode structure. Since the single FET only shows the MAG below 9-dB, it is not easy to attain the LNA gain of two stage over 15-dB without excess power consumption due to the loss of matching networks. To boost the gain, the design introduces a new and simple positive feedback method utilizing proximate magnetic coupling between two load inductors L_1 and L_2 as shown in Fig. 2. The phase change in the cascode stage has an important role to determine the gain and resonant frequency of the magnetic feedback. The phase change should be less than – 90° to achieve the desired feedback effects and it inherently causes by RC delay. The magnetic coupling can be achieved simply by the close placement of two inductors without shield guards as shown in the part of LNA in Fig. 3 which in turn reduces the chip size. The required distance between two

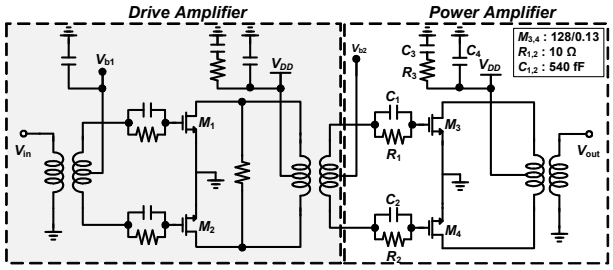


Fig. 3. Schematic of DA and PA.

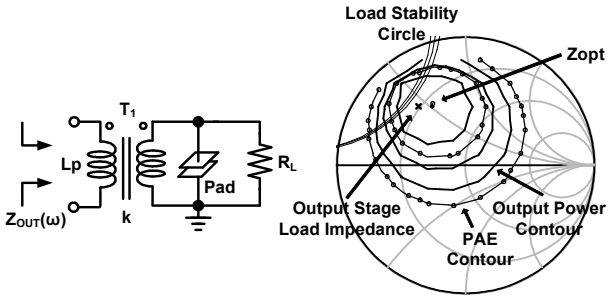


Fig. 4. (a) Equivalent circuit of the PA output and (b) load-pull simulation result.

inductors is determined using full-wave electro-magnetic simulation. It is observed that the operating frequency can be enhanced compared to the design without feedback and the gain is increased by 3 dB as confirmed in Fig. 4(a) without the increase of power consumption and any additional circuitry. After the LNA, a single balanced mixer is used to reduce the loading of LO port and simplify the layout. In radar systems, LO to IF feed-through can be easily eliminated by using bypass capacitors C_6 and C_7 because the IF (beat) frequency in the FMCW radar system is usually below 1 MHz and much lower than the LO frequency. The current bleeding technique using the PMOS M_5 reduces the flicker noise, which also plays a role of transconductance cell to enhance the conversion gain. The inductor L_3 is used to neutralize the parasitic source and drain capacitances at the common-node of the switching stage and to reduce the indirect flicker noise [8]. Therefore, it improves the conversion gain and reduces the noise contribution by the switching stage.

2. Transmitter

The transmitter is composed of the PA for increasing the power of a signal. The maximum allowable power

limit and the corresponding measurement procedures for 24-GHz radar systems are defined in the ETSI standard EN 302 288-1 [9]. Within ISM band, the peak equivalent isotropic radiated power (EIRP) is limited to 20 dBm, which includes the gain of the transmitting antenna (G_{TX}) and the actual transmitting power (P_{TX}) as follows [10],

$$P_{EIRP}(dBm) = P_{TX}(dBm) + G_{TX}(dBm) \quad (1)$$

Therefore, a PA with 10 dBm output power is sufficient to achieve the required maximum radar range.

The designed differential PA is shown in Fig. 3. It includes a drive amplifier (DA) for individual test. But, the PA integrated in the transceiver is directly driven by the injection buffer as explained in II-3 instead of the DA, which reduces the power consumption and chip area. A common-source (CS) amplifier is used as a unit power cell. Due to the low supply voltage, CS structure is more advantageous than cascode stage for higher efficiency and better linearity. The output and the inter-stage matching networks utilize a transformer to achieve power matching and ESD protection. The transformer and output pad capacitance consist the matching circuitry to transform 50 Ω load to the optimum load impedance that maximizes output power, efficiency and ensures stability. Fig. 4 presents the equivalent circuit of the PA output and the load-pull simulation result. The transformer is designed using full-wave electromagnetic simulator.

Stability is a prime consideration in PA design. A stabilization network composed of shunt resistor and capacitor is added at the gate of each transistor. To ensure common mode stability at low frequencies, an additional R-C network is used at the center-tap of the transformer.

3. VCO, Injection-Locked Buffer, and Power Divider

Fig. 5 shows the VCO and injection-locked buffer. The VCO is designed to oscillate at 24-GHz and its output is fed to the buffer and the first divider in the PLL directly. The buffer should provide a large voltage swing for driving mixer and PA. Since the mixer and PA show large capacitive loading, the buffer should be designed with a sufficiently large transistor which consumes large power. However, the transistor size of the buffer is limited by the VCO resonance frequency and tuning

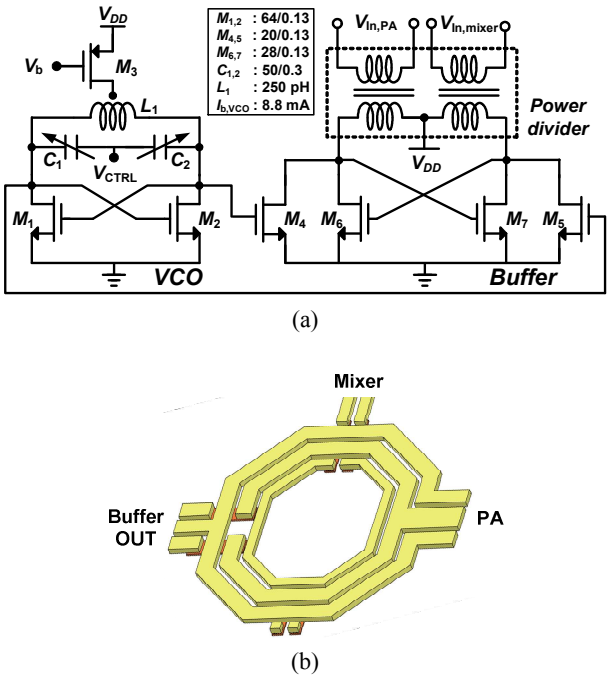


Fig. 5. (a) Schematic of VCO and injection-locked buffer and (b) the structure of the power divider.

range. As the oscillating frequency increases, the input capacitances of the buffer burden the VCO substantially. To reduce the buffer loading, multi-stage buffer amplifiers can be used with subsequent size and power scaling, but they increase power consumption and chip size. To overcome the above problem, this work adopts an injection-locked buffer. The injection-locked operation is an attractive technique to obtain a large voltage swing with low power consumption. Furthermore, it can reduce capacitive loading to the VCO. The injection amplifier is composed of M_4 and M_5 with moderate width of 20 μm. The additional cross-coupled pair composed of M_6 and M_7 increases gain and voltage swing. Therefore, the buffer can drive the mixer and PA with an enough voltage swing under low power consumption, even with the small sizes of M_4 and M_5. When the cross coupled pair is used, stability is a critical issue to avoid self-oscillation. However, it is not a problem in FMCW radar applications. If the self-oscillation frequency of the buffer can be pulled by the injection from the VCO, the radar can work properly. The frequency of the self-oscillating buffer can synchronize with the frequency of the injected signal from the VCO as explained in [11],

$$\left|\omega_{VCO}-\omega_0\right| < \Delta\omega_{lock} \tag{2}$$

$$\Delta\omega_{lock} = \frac{\omega_0}{2Q}\frac{A_{VCO}}{A} \tag{3}$$

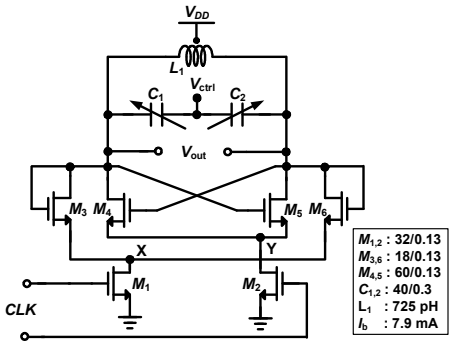
where ω_{VCO} and ω_0 are the frequencies of the VCO and the buffer, respectively. The symbol $\Delta\omega_{lock}$ represents half of the entire locking range. If the self-oscillating buffer satisfies conditions (2) and (3), its oscillation frequency follows the VCO frequency.

The load of the injection-locked buffer is implemented with the three-coil transformer as shown in Fig. 5(b). The transformer distributes the buffer power to the mixer and the PA. By using the transformer, the chip size can be reduced and the layout is much more simplified, since the transformer provides a simple bias network through the common-node and enables ac-coupling without capacitors. The top metal layer is used for the transformer layout to decrease the resistive loss.

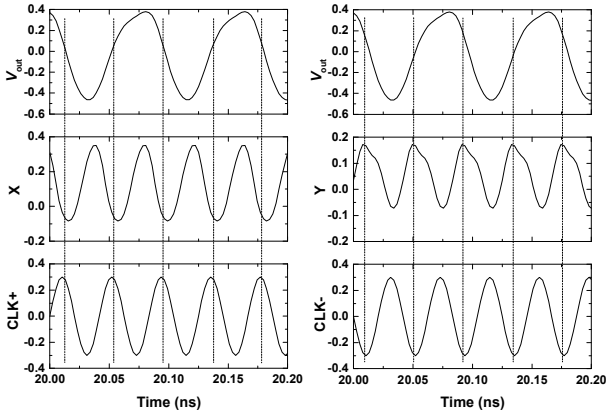
4. PLL

The integer-N PLL is used to precisely define the output frequency of the VCO. It consists of frequency dividers, phase frequency detector, charge pump and loop filter. The injection-locked frequency divider is used as the first divider stage. The schematic of the injection-locked frequency divider is shown in Fig. 6(a), and its operation is presented in Fig. 6(b). It has two injection mechanisms depending on the signal injection path. The injection signal is ac-coupled to the gate of M_1 and M_2. One injection path is through the transistor M_1. When the positive signal is injected into the transistor M_1, the voltage of the node X is decreased. As the injection voltage increases, the gate-source voltages of the transistors M_3 and M_6 become to exceed the threshold voltage. As a result, the diode-connected transistors M_3 and M_6 turn on and the differential outputs of the divider are connected with low impedance path. Therefore, the output is forced to zero and the zero-crossing of the divider output is synchronized with the VCO signal.

On the other hand, the other injection path is through the transistor M_2. In this case, the divider works like a conventional injection-locked divider. By the dual-injection scheme, the locking range can be enhanced. Additionally, the diode-connected transistors M_3 and M_6 make the locking range wider by degrading the quality factor of the tank. Thus, the divider has sufficient design margin to cover the entire VCO tuning range.



(a)



(b)

Fig. 6. (a) Schematic of 1st divider, and (b) its operation.

The second and third frequency dividers are based on master-slave D-type flip-flop using current-mode logic structure (CML) for high speed operation [12]. The other dividers are implemented with true-single-phase-clock (TSPC) divider considering its simple architecture, compact implementation, and small power consumption for moderate speed [13]. For complete PLL operation, the tri-state phase frequency detector with 50 MHz reference frequency and the second-order loop filter are adopted.

III. EXPERIMENTAL RESULTS

The transceiver chip is fabricated in 130 nm CMOS technology of Dongbu HiTek with 1-poly and 8-metal layers with the top metal thickness of 3.3 μm. The die microphotograph of the chip is shown in Fig. 7 and its size is 1.2×1.4 mm^2 including pads ESD protected.

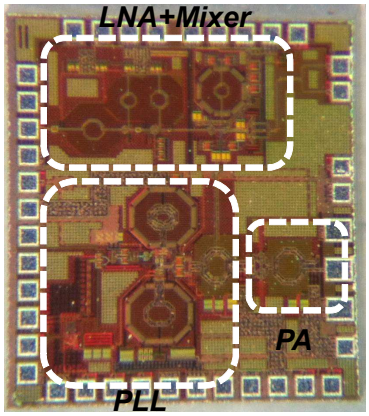
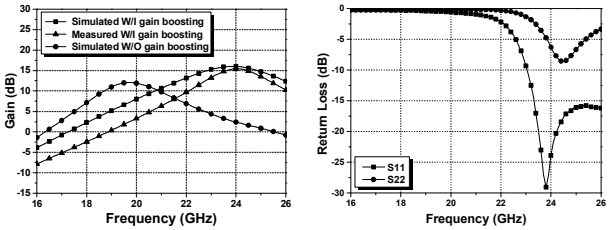
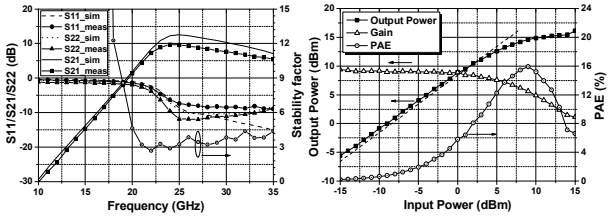


Fig. 7. Chip microphotograph.



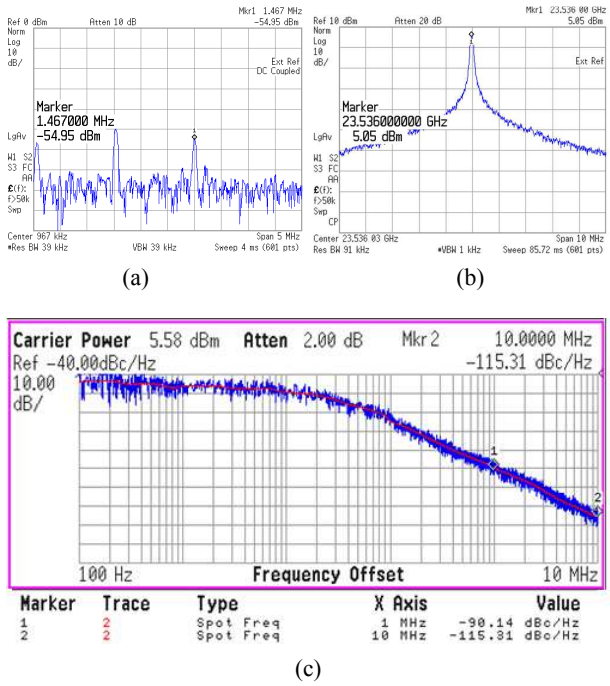
(a) (b)

Fig. 8. LNA simulated and measured results: (a) small-signal gain, and (b) input and output return losses.



(a) (b)

Fig. 9. PA simulated and measured results: (a) small-signal, and (b) large-signal.



(a) (b)

(c)

Fig. 10. Transceiver measurement results: (a) IF spectrum with RF input power of -74 dBm including cable loss, (b) PA output spectrum with cable loss of 4 dB, and (c) phase noise.

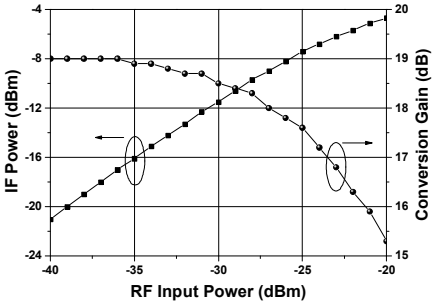


Fig. 11. Measured conversion gain and IF output power versus RF input power with IF frequency 1 MHz.

To verify the performance of each block, we designed and tested the LNA and PA individually. The chips are measured using on-wafer probing. The input and output return losses of LNA are shown in Fig. 8(b). The LNA has a peak gain of 15.42 dB with 5.4 dB noise figure at 24-GHz. The LNA without gain boosting shown in Fig. 8(a) is simulated with same size transistors, bias current and passive components, only except the coupling between inductors. The PA has a saturation power of 15 dBm with 16% peak PAE and the output P_1dB is 9.4 dBm.

The transceiver chip is mounted directly on the printed circuit board to supply the dc biases. RF signals such as LNA input and PA output are measured using wafer probing. Fig. 10 shows measurement results of the transceiver. The voltage conversion gain of the receiver is 19 dB and the transmitter output power is 9 dBm considering 4 dB cable loss at 24-GHz. The 1dB compression point of the LNA is -27 dBm. The frequency synthesizer has phase noise of -90 dBc/Hz at 1-MHz offset and -115 dBc/Hz at 10-MHz offset. Unfortunately, oscillation frequency of the VCO is slightly lower than the target frequency at ISM band. The frequency shift is possibly caused by the small size inductor for the VCO design because small size devices usually have low modeling accuracy due to de-embedding and measurement error.

The transceiver consumes a total power of 142 mW, of

Table 1. Performance summary and comparison of previous works

	This work	[3]	[5]	[6]
Process	130 nm CMOS	0.18 μm SiGe BiCMOS	130 nm CMOS	130 nm CMOS
Integration	Rx, Tx, PLL, 1-channel	Rx, Tx, PLL, Baseband, SPI, 15-bit DAC, 2-channel	Rx, PA driver, VCO, frequency divider, 1-channel	Rx
RX gain (LNA + Mixer)	19 dB	18 dB	12 dB	16.5 dB
RX Noise figure	5.4 dB (LNA)	10 dB	5.5 dB	5.3 dB
P_{1dB}	-27 dBm	- 15 dBm	-16.2 dBm	-26 dBm
Frequency	21.7 ~ 23.8 GHz	24 GHz	23.8-26.4 GHz	24 GHz
Phase noise	- 90 dBc/Hz @ 1 MHz - 115 dBc/Hz @ 10 MHz	- 82 dBc/Hz @ 100 kHz	-101 dBc/Hz @ 1 MHz	-
TX output power	+ 9 dBm	+ 7 dBm	-3 dBm	-
Power Consumption	142 mW	963 mW	88 mW	18 mW
Chip size	1.2 × 1.4 mm^2	5 × 5 mm^2 (QFN)	1.17 × 0.61 mm^2	1.4 × 0.5 mm^2

which 74 mW is dissipated in the injection-locked driver amplifier and the PA, 10 mW in LNA, 14 mW in the mixer and buffers, remaining power in the frequency synthesizer.

Table 1 summarizes the transceiver performance compared with the published K-band radar chipsets. The transceiver consumes less power and smaller chip size with compatible performance.

IV. CONCLUSIONS

A fully-integrated low power K-band radar transceiver is presented in this paper. The voltage conversion gain of the receiver is 19 dB, and the output power of the transmitter is 9 dBm. By adopting low power design, the total power consumption is significantly reduced. The transceiver will enable integrated low-cost FMCW radar system design.

ACKNOWLEDGMENTS

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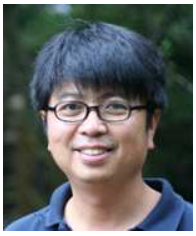

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