Comparative investigation of endurance and bias temperature instability characteristics in metal-Al_2O_3-nitride-oxide-semiconductor (MANOS) and semiconductor-oxide-nitride-oxide-semiconductor (SONOS) charge trap flash memory

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Abstract—**The program/erase (P/E) cyclic endurances including bias temperature instability (BTI) behaviors of Metal-Al_2O_3-Nitride-Oxide-Semiconductor (MANOS) memories are investigated in comparison with those of Semiconductor-Oxide-Nitride-Oxide-Semiconductor (SONOS) memories. In terms of BTI behaviors, the SONOS power-law exponent n is ~0.3 independent of the P/E cycle and the temperature in the case of programmed cell, and 0.36~0.66 sensitive to the temperature in case of erased cell. Physical mechanisms are observed with thermally activated h* diffusion-induced Si/SiO_2 interface trap (N_{IT}) curing and Poole-Frenkel emission of holes trapped in border trap in the bottom oxide (N_{OT}). In terms of the BTI behavior in MANOS memory cells, the power-law exponent is n=0.4~0.9 in the programmed cell and n=0.65~1.2 in the erased cell, which means that the power law is strong function of the number of P/E cycles, not of the temperature. Related mechanism is can be explained by the competition between the cycle-induced degradation of P/E efficiency and the temperature-controlled h* diffusion followed by N_{IT} passivation.**

Index Terms—**MANOS memory, SONOS memory, bias temperature instability, interface trap**

I. INTRODUCTION

Nitride-based charge trap flash (CTF) memories are under active research and development as promising solutions over conventional floating-gate flash (FGF) memories [1]. CTF memories have various advantages including low voltage operation, good retention, better scalability, and compatibility with complementary metal-oxide-semiconductor (CMOS) VLSI technologies [2]. Especially CTF memories with NAND-type flash cell arrays have been reported for the purpose of replacing the commercial mass data storage disks [3, 4] and their P/E operations are based on the Fowler-Nordheim (FN) tunneling [5-7]. As a major concern of the performance, the relatively low erase efficiency in CTF memories is generally believed to be due to the back tunneling of electrons from the gate to the nitride storage layer through the degraded top oxide (or blocking oxide). Very recently, in perspective of this viewpoint, a well-engineered tunnel barrier of NAND-type CTF memories using high-k dielectrics and metal gate (e.g. Metal-Al_2O_3-Nitride-Oxide-Semiconductor (MANOS) and/or

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TaN-Al_2O_3-Nitride-Oxide-Semiconductor (TANOS)) have been investigated improving the erase efficiency and performance, as reported in previous works [3, 8].

In cases of NAND-type CTF memories, in order to systematically benchmark the three-dimensional (3-D) cell transistors with various CTF memory stacks (SONOS, SANOS, MANOS, BE-SONOS [9], VARIOT [10], and TANOS), a comparative investigation is strongly required in perspective of the complicated reliability issues including the P/E cycling effect, the influences of carrier polarity (electron and hole), the bias temperature instability, and the FN stress time evolution. Especially, the unified understanding of P/E cyclic endurance under a readout condition has the industrial importance because it makes a significant role on the expectation of circuit design issues (readout margin, power consumption, area burden, and etc.). Motivated by these viewpoints, we reported the dynamic bias temperature instability (BTI) behaviors of P/E cycled cell in SONOS memories [11]. In this work, for unified understanding, the P/E cyclic endurances of MANOS memories are comprehensively investigated in comparison with those of SONOS memories. During the P/E cycling by the FN stress, both Si/SiO_2 interface trap (N_{IT}) and border trap in the bottom oxide (N_{OT}) are characterized in detail by analyzing the P/E cycle evolution of V_T, the subthreshold swing (SSW), the hysteresis during a readout condition, and the P/E efficiency. In addition, the dynamic BTI behaviors including the temperature-dependences of both the P/E stress time-evolution and the P/E cycle-evolution of V_T and/or SSW are characterized.

II. Device Fabrication and Measurement

The SONOS CTF memory devices were fabricated by a conventional CMOS process technology. The SONOS CTF memories with an extremely scaled gate ($L \times W=30 \times 30$ nm^2) were formed by the sidewall patterning technique [12]. The channel implantation was performed by BF^{2+} ions and B^+ ions on the boron-doped (4×10^{15} cm^{-3}, 100) fully depleted silicon-on-insulator (SOI) substrate (SOI thickness=50 nm). Then a 2.3 nm-thick bottom oxide was grown at 900°C. Subsequently, the 12 nm-thick Si_3N_4 film and a 4.5 nm-thick top oxide were deposited by low pressure chemical vapor deposition (LPCVD). After 30 nm poly-silicon gate patterning using the sidewall patterning technique, n^+ source/drain extension regions were formed with a low energy As^+ ion implantation. Finally, deep source/drain regions were formed by As^+ ion implantation and rapid thermal annealing.

In the case of MANOS CTF memory devices (capacitor), a 3 nm-thick bottom oxide layer was grown by thermal oxidation on the boron-doped (1×10^{17} cm^{-3}) p-type substrate. Then, a 6 nm-thick nitride layer was deposited by LPCVD. A 10 nm-thick Al_2O_3 top dielectric layer was deposited by using an atomic layer deposition at 500°C. Finally a 600 nm-thick Al gate (area=πr^2, r=200 μm) is deposited by e-beam evaporation and patterned on the ANO stack.

Although the condition for prepared samples is different from each other (SONOS transistor with ONO=4.5/12/2.3 nm, equivalent oxide thickness (EOT)=4.5/6.2/2.3 nm and MANOS capacitor with ANO=10/6/3 nm, EOT=4.3/3.1/3 nm), we expect that the validity of characterizing the P/E cyclic endurance and BTI behavior is effective except the detailed quantitative results. Hereinafter, the MANOS capacitor will be referred to as the MANOS cell or MANOS CTF device for convenience.

The P/E operation is performed by FN tunneling as follows: the gate voltage V_G=10/–10 V with the pulse width T_P/T_E=5/50 ms (SONOS) and V_G=11/–12 V with T_P/T_E= 200/500 ms (MANOS). While the flat band voltage V_{FB} is extracted by measuring the gated-diode current in SONOS CTF memory devices [13], V_{FB} in MANOS CTF memory devices is extracted from the flat band capacitance (C_{FB}) point of C-V curve described as-[14]

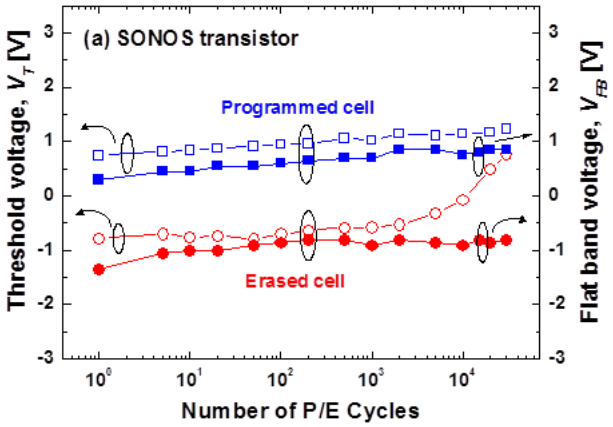
$$C_{FB} = \frac{C_{ANO}}{\left(1+\frac{136\sqrt{T/300}}{T_{ANO}\sqrt{N_A}}\right)} \quad (1)$$

where T_{ANO} is equivalent oxide thickness (=10.4 nm), N_A is substrate doping concentration (=1×10^{17} [cm^{-3}]), and T is the operation temperature respectively. The C-V curve is measured by Agilent 4284A LCR Meter and the P/E stress pulse is applied by Agilent 41501B Pulse Generator Expander connected with 4156C Precision Semiconductor Parameter Analyzer. Endurance tests were performed up to 30,000 P/E cycles and the

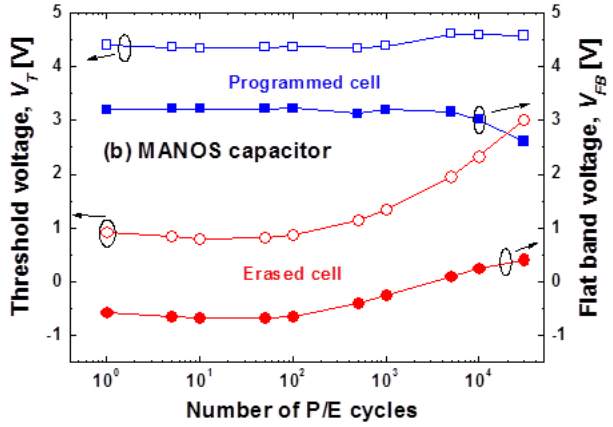
characterization was performed at T=300~400 K based on the hot chuck by using the temperature controller connected with PC.

III. RESULTS AND DISCUSSION

In the case of SONOS memory devices, while V_T of the programmed state (V_{TP}) is slightly increased, V_T of the erased state (V_{TE}) shows a severe roll-up as the number of P/E cycles increases as shown in Fig. 1(a). Since the variation of V_{FB} is not significant with P/E cycles, we conclude that the degradation of V_{TE} with P/E cycles mainly results from the increased N_{IT} rather than the back tunneling and/or the increased N_{OT}. In the case of MANOS memory devices, on the other hand, both V_{TP} and V_{TE} are degraded with P/E cycles. The P/E cycle evolution of V_{FB} shows that P/E efficiency decreases with P/E cycling due to increased N_{IT}.



(a)



(b)

Fig. 1. The P/E cycle evolution of both V_T and V_{FB} in (a) SONOS memory cell transistor, and (b) MANOS memory cell capacitor.

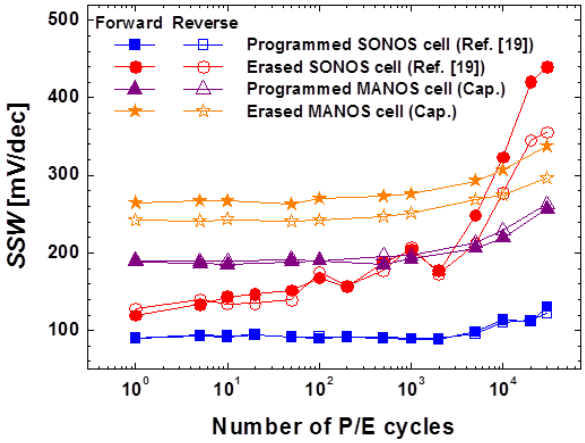


Fig. 2. The P/E cycle evolutions of SSW in SONOS memory cell (from I-V) and SSW in MANOS memory cell (from C-V).

In order to clarify the origin of P/E cycle evolution in Fig. 1, SSW with P/E cycling is shown in Fig. 2. The forward sweep is followed by the reverse sweep in measuring I-V (SONOS) and C-V (MANOS) curves.

In addition, under the readout condition of erased cell, the passivation of N_{IT} occurs during a forward sweep so that the SSW in reverse sweep is always lower than that in forward sweep. It is also worthy of noting that the difference of SSW between forward and reverse sweep is prominent only in the erased cell (in both cases of SONOS and MANOS), which is because that N_{IT}s in the programmed cell are fully passivated during program operation.

In Fig. 2, it should be understood that the P/E cycle-dependence of SSW is dominantly observed only in the SONOS erased cell. In the program condition of P/E cycled SONOS cells, injected holes by anode hole injection (AHI) are recombined with electrons trapped in the nitride layer and induce the damage in the top oxide. Then, in the erase condition, both the bottom oxide and the Si/SiO_2 interface are severely damaged by holes injected from the Si substrate. Which causes a large increase in both SSW and V_T with P/E cycles. On the other hand, in the P/E condition of P/E cycled MANOS cell, the higher hole tunnel barrier prevents holes from injecting through the AHI process. Therefore, the generation of N_{IT} and N_{OT} with P/E cycling in bottom and/or top oxide is less significant in MANOS cell than that in SONOS cell. Thus, the P/E cycle-dependence of SSW is the most distinct in the SONOS erased cell.

Our results properly agree with mechanisms in previous reports [15, 16] In the previous works, the generation and recovery of N_{IT} (as is the case in negative bias temperature instability (NBTI) in pMOSFETs) are modeled by the reaction-diffusion (R-D) theory for the released h* species away from Si/SiO_2 interface. This is also consistent with the polarity-dependent degradation mechanism [17].

The FN stress time dependence of ΔV_T, which eventually represents the P/E efficiency of memory cell, is shown in Fig. 3. Further, Fig. 4 illustrates the schematic energy band diagram of P/E cycled cells subjected to the FN P/E stress.

In the SONOS memory device, the power-law exponent n (=0.3) in the SONOS programmed cell is independent of the temperature in the 30k P/E cycled cell as well as in the fresh cell (Fig. 3(a)). This shows that the main conduction mechanism through the ONO dielectric layer in the programmed cell is only FN tunneling. The n in the SONOS erased cell is very sensitive to both the temperature and the number of cycles (Fig. 3(b)). This dependency indicates that the conduction mechanism in the erased cell is strongly correlated with not only the thermionic emission i.e., Poole-Frenkel (P-F) emission but also the amount of N_{IT}. These BTI characteristics of SONOS memory cells are analyzed as follows.

In cases of the program and the readout of programmed cell, the hole-trapping in the bottom oxide is alleviated due to the recombination in the nitride layer (Fig. 4(a)). On the other hand, both in the erase and in the readout of erased cell conditions, holes are injected from the Si substrate and the top gate, respectively. The significant parts of injected holes from the Si substrate in the erase operation and from the gate during the readout operation, respectively, are captured by bulk traps N_{OT} in the bottom oxide. If once the hole-trapping in bottom

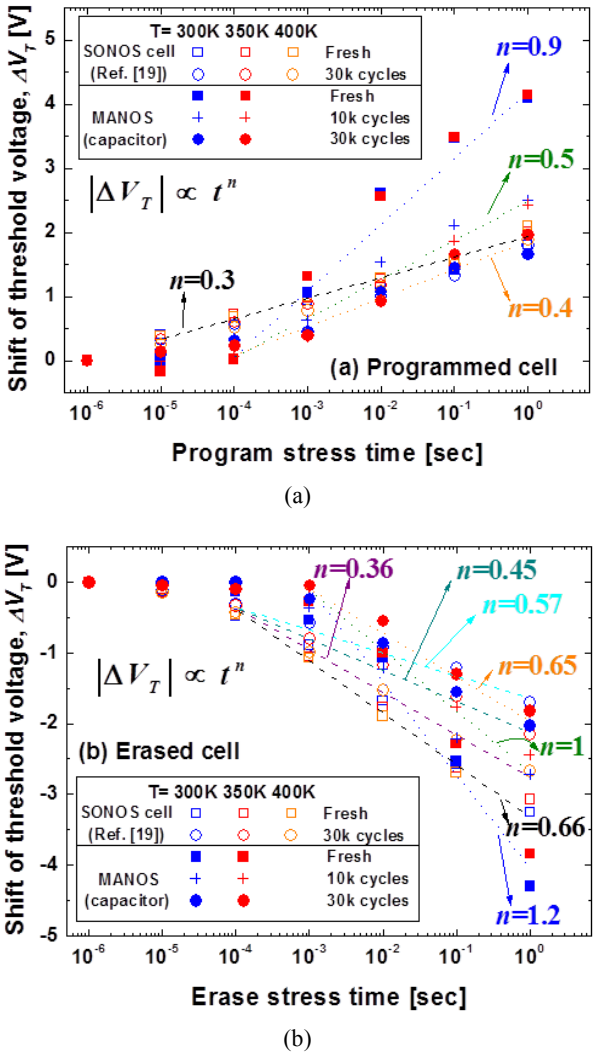


Fig. 3. Measured BTI behaviors of SONOS and MANOS CTF memory cells. (a) The program time-dependence, and (b) the erase time-dependence of V_T at various temperatures and P/E cycles

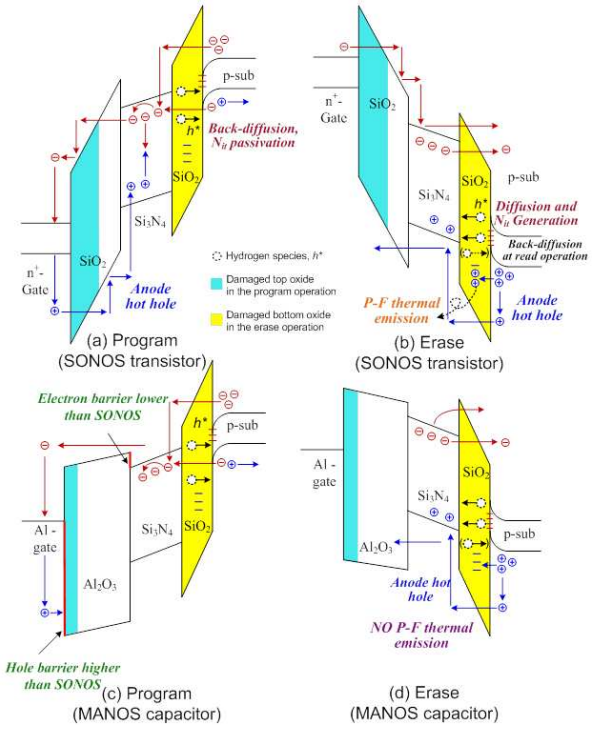


Fig. 4. Schematic energy band diagrams illustrating the BTI physical mechanism in the P/E cycled cell. (a) Program, and (b) erase conditions in SONOS memory cells, (c) Program, and (d) erase conditions in MANOS memory cells.

oxide during the readout of erased cell operation occurs and is accumulated in P/E cycled cell, AHI from Si substrate during the erase operation becomes more alleviated and consequently the erase efficiency more degraded. Therefore, the erase efficiency in fresh cell (n=0.66) is higher than that in cycled cell (n=0.57~0.36) as shown in Fig. 3(b), if and only if there exist the P/E cycle-induced traps (damages) both in the top and bottom oxide. These captured holes can be detrapped by the thermal P-F emission. While the erase stress time T_E evolution of V_{TE} shows a weak dependence on the temperature in the fresh erased cell, it is very sensitive to the temperature in the cycled erased cell. The detrapping of holes by the thermal P-F emission becomes more prominent as the temperature increases (Fig. 3(b)). Even if the higher temperature makes the erase more efficient in the cycled cell, it is not comparable to that in the fresh cell because the holes trapped in the bottom oxide still exist even at 400 K.

In addition, based on the reaction-diffusion (R-D) model in NBTI of pMOSFETs, the temperature-dependence becomes reinforced under the readout condition of SONOS erased cell in as much as the h* back-diffusion to Si/SiO_2 interface followed by the recovery of N_{IT} becomes more activated with the increased temperature. Furthermore, the increased N_{IT} with P/E cycles hurdles the efficient modulation of the energy band bending by V_{GS} and eventually the erase efficiency gets worse with P/E cycles. Hence, the erase efficiency in the fresh cell is always better than that in the cycled cell. For the role of holes in the stress condition, it has been recently shown that the generation of N_{IT} (ΔN_{IT}) during the hot carrier injection (HCI) stress has both contributions of broken ≡Si–H and ≡Si–O bonds in MOSFETs [17]. While the broken Si ≡ H bond-induced ΔN_{IT} shows a power-law time exponent n = 0.15~0.3 depending on the measurement setup, the ruptured ≡Si–O bond-induced ΔN_{IT} shows n>0.5 and is correlated with AHI.

In contrast to the NBTI stress, hot holes make significant roles in the ΔN_{IT} under HCI and/or FN stress [18]. Therefore, our cases agree with the cases of MOSFETs in the related literatures [16, 18, 19] because the observed n = 0.3 in the programmed cell is close to that of NBTI in pMOSFETs (known to be n ≈ 0.25) [20] , and n=0.36~0.66 in the erased cell with various stress and temperature conditions is consistent with the case of hot hole-induced rupture of ≡Si–O bond (n > 0.5). Comparing with the case of NBTI in pMOSFETs, two points are worthy of noting. The first one is higher n in SONOS erased cells under FN stress than that in pMOSFETs subjected to NBTI stress, which is evidently due to both the larger amount of N_{IT} and the AHI-induced holes. Another one is that the order of magnitude of FN stress time required to observe a significant ΔV_T (or ΔN_{IT}) is much shorter in SONOS erased cells than that in pMOSFETs. It is due to the charges trapped in the nitride storage layer and this high charge-trapping efficiency is also the motivation of SONOS memories.

In the MANOS memory devices, on the other hand, the power-law exponent n (=0.4~0.9) in the programmed cell is almost independent of the temperature in the 1~30k P/E cycled cell as well as in the fresh cell. However, the P/E cycle-dependence of n is clearly observed as shown in Fig. 3(a). This is a significant difference from the case of the programmed SONOS cell. It is because the degradation of the program efficiency due to the increased N_{IT} with P/E cycling rather than the h*-diffusion-induced N_{IT} passivation is more dominant mechanism controlling the programmed MANOS cell, which is consistent with Fig. 1(b). In the erased MANOS cell, moreover, the P/E cycling-dependence of n (=0.65~1.2) is more prominent than the temperature-dependence, vice versa in the erased SONOS cell. It means that the major role of temperature-dependence in the MANOS cell is the N_{IT} generation followed by the degradation of SSW rather than the P-F emission of trapped holes in the bottom oxide and/or more activated diffusion-reaction of h* than the case in the SONOS cell. Our results are consistent with the suppressed hole trapping of N_{OT} in the readout condition of the erased MANOS cell due to the high hole barrier at the gate/top oxide interface.

Fig. 5 shows the P/E time-dependence of SSW for the erased SONOS cell at various temperatures. In the case of the fresh cell, SSW becomes lower as the temperature decreases because SSW is monotonically proportional to the thermal energy as far as the N_{IT} remains constant (Fig. 5(a)). In addition, the difference of SSW between forward and reverse sweeps is enlarged with the increase of temperature only in the erased SONOS cell. It is attributed to enhancement of activated h* diffusion

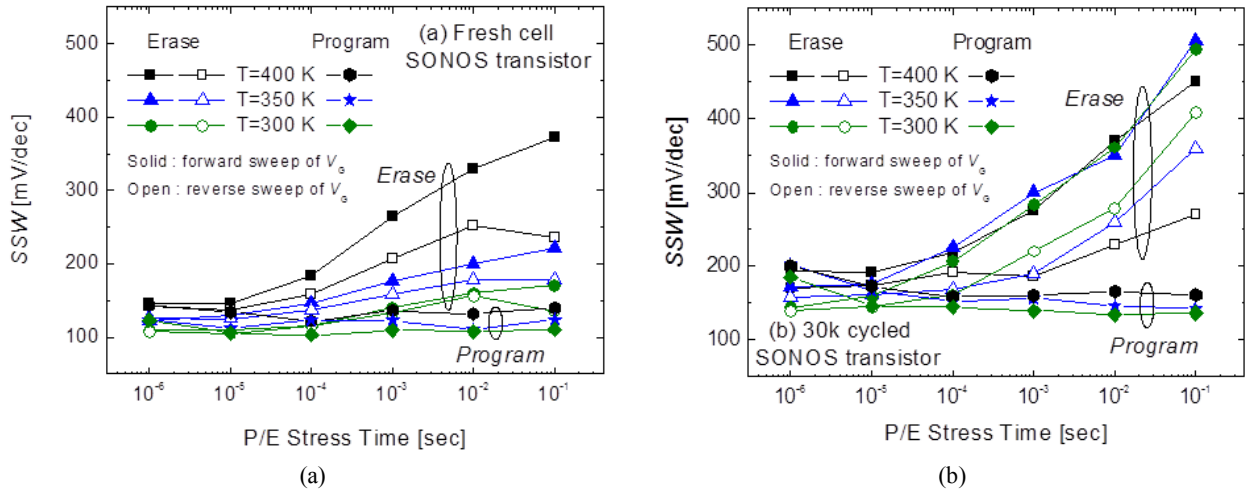


Fig. 5. The P/E-time dependence of SSW in the SONOS cell at various temperatures in (a) the fresh cell, and (b) the 30k cycled cell, respectively.

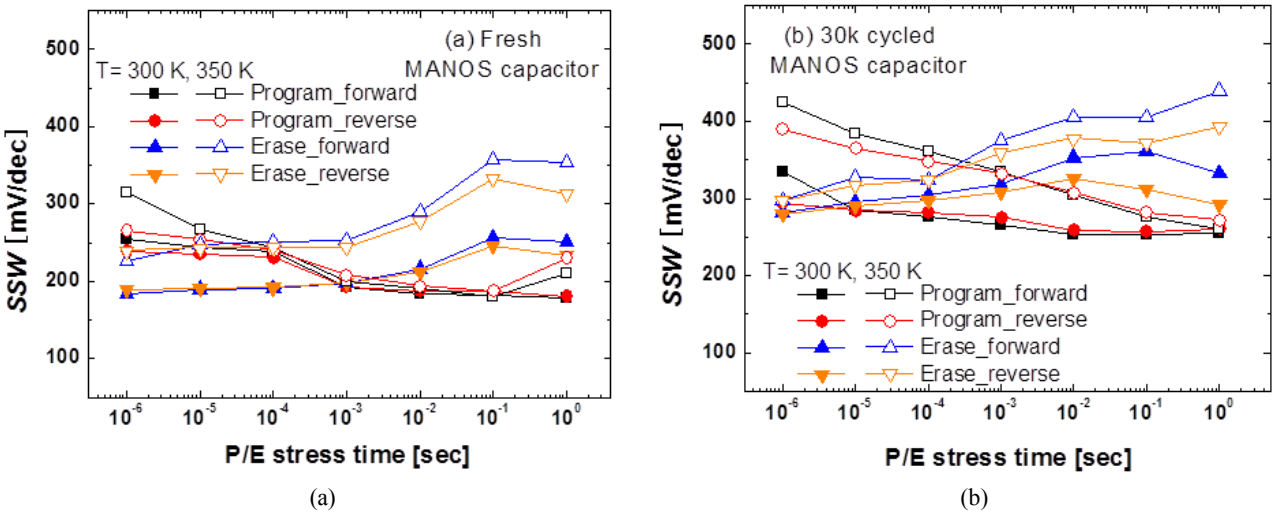


Fig. 6. The P/E-time dependence of SSW in the MANOS cell at various temperatures in (a) the fresh cell, and (b) the 30k cycled cell, respectively.

during the readout condition of the erased cell. In the case of the P/E cycled SONOS cell, on the contrary, SSW in the forward sweep becomes independent of the temperature because the temperature-dependence of the h* diffusion compensates that of SSW caused by the thermal energy (Fig. 5(b)). Furthermore, the SSW difference between forward and reverse sweeps increases with the temperature increase. This result is very reasonable because the passivation of N_{IT} caused by the h* back-diffusion to Si/SiO_2 interface becomes more activated with the temperature increase. The P/E time-dependent SSW of the MANOS erased cell at various temperatures is shown in Fig. 6, compared with the SONOS erased cell as shown in Fig. 5. As the P/E stress time evolves, SSW in the fresh MANOS cell decreases in the programmed cell, and increases in an erased cell (Fig. 6(a)). It is the evidence of the h* diffusion-induced N_{IT} curing in the MANOS program condition. Therefore, the temperature-dependence of SSW in the fresh programmed cell is negligible. However, in the P/E cycled programmed MANOS cell, the temperature-dependence becomes more prominent because the h* diffusion-induced N_{IT} curing process cannot compensate the thermal energy-dependent term in SSW (Fig. 6(b)).

IV. CONCLUSIONS

The P/E cyclic endurances including BTI behaviors of MANOS memories are comprehensively investigated in comparison with those of SONOS memories. BTI behaviors including the temperature-dependences of P/E stress time-evolution and the P/E cycle-evolution of V_T/SSW. Our results show that the role of the P/E cyclic endurances including BTI behaviors should be fully considered in the reliability modeling, the optimization of the P/E efficiency, and the lifetime projection of nitride-based CTF memories such as SONOS and MANOS devices for robust implementation. It is shown that the dominant mechanism of the BTI characteristics is a strong function of the structure in nitride-based CTF memory stacks (i.e. high-k or bandgap engineering). Especially, our unified understandings of the P/E cyclic endurances and their related reliability issues in CTF cells under a readout condition give a physical insight of making a significant role for the expectation of circuit design issues (readout margin, power consumption, area burden, and etc.).

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Sungwook Park photograph and biography not available at the time of publication.

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