http://dx.doi.org/10.5573/JSTS.2012.12.4.458 JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.12, NO.4, DECEMBER, 2012

Analytical Modeling and Simulation for Dual Metal Gate Stack Architecture (DMGSA) Cylindrical/Surrounded Gate MOSFET

Pujarini Ghosh*, Subhasis Haldar, R. S. Gupta***, and Mridula Gupta***

***Abstract*—A Dual metal gate stack cylindrical/ surrounded gate MOSFET (DMGSA CGT/SGT MOSFET) has been proposed and an analytical model has been developed to examine the impact of this structure in suppressing short channel effects and in enhancing the device performance. It is demonstrated that incorporation of gate stack along with dual metal gate architecture results in improvement in short channel immunity. It is also examined that for DMGSA CGT/SGT the minimum surface potential in the channel reduces, resulting increase in electron velocity and thereby improving the carrier transport efficiency. Furthermore, the device has been analyzed at different bias point for both single material gate stack architecture (SMGSA) and dual material gate stack architecture (DMGSA) and found that DMGSA has superior characteristics as compared to SMGSA devices. The analytical results obtained from the proposed model agree well with the simulated results obtained from 3D ATLAS Device simulator**.

***Index Terms*—Dual metal gate stack architecture (DMGSA), surrounded/cylindrical gate MOSFET (CGT/SGT), short channel effects (SCEs)**

Manuscript received Apr. 27, 2012; revised Jul. 26, 2012.
* Semiconductor Device Research Laboratory, Department of Electronic Science, University of Delhi, South Campus,
New Delhi , 110021, India.
Tel: 91-11-24115580; Fax: 91-11-24110606
E-mail: mridua@south.du.ac.in, puja510@gmail.com
** Department of Physics, Motilal Nehru College, University of Delhi, New Delhi, 110021 India.
*** Department of Electronic and Communication engineering, Maharaja Agrasen Institute of Technology, Rohini, Delhi 110085, India.

I. INTRODUCTION

Rapid downscaling of device dimensions, innovative device design and rapid advances in technology are some of the factors that have largely governed the evolution of CMOS technology at a remarkable rate over the past few decades. Due to which faster integrated circuits have been achieved which offer superior performance. However, the miniaturization of bulk MOSFET leads to short channel effects (SCEs) [1-3] such as drain induced barrier lowering, punch through, channel length modulation and reduction in current drivability. These issues become a serious challenge for further downscaling while maintaining a high quality of device performance. In order to overcome the scaling limitations and to increase the device performance various structures such as double gate [4], Pi gate [5], triple gate [6] or fin shaped gate [7], omega gate [8] and surrounded/ cylindrical gate have been proposed. Among this cylindrical/surrounded (CGT/SGT) gate MOSFET [9-14] offers higher packing density, steep subthreshold characteristics and higher current drive. Another remarkable feature of this structure is that the gate surrounds the silicon pillar completely and therefore controls the channel potential in a more effective manner resulting in increased short channel immunity. All these features make CGT/SGT a potential candidate to succeed the bulk MOSFET.

Recently various gate engineering structures have been studied and proposed to address the challenge of SCEs

and higher performance for deep submicrometer VLSI integration. Dual metal gate (DMG) architecture has also been investigated [15, 16] as one of the possible solution for reducing short channel effects present in deep sub micrometer devices. In this DMG design two different metal gate electrodes are used having different workfunctions. One near the source end (control gate) having workfunction more than the gate near the drain end (screen gate). Due to this work function difference, a potential step and an electric field peak in the channel is formed. Hence carrier transport efficiency is increased thereby suppressing the short channel effects.

Steady downscaling of device dimensions leads to reduction in voltage level as well as the gate oxide thickness. However, the level to which the gate oxide thickness can be scaled down is limited by direct tunneling which leads to an increase in the gate leakage current thus degrading the device performance. It also causes an increase in static power consumption, which can hamper the circuit operation [17]. In order to overcome the above limitations intensive stress has been made for the use of high K dielectrics as a gate insulator in lieu of SiO_2 to prevent direct tunneling leakage current. However, the studies illustrated that superseding SiO_2 with high K dielectrics reduces the device performance due to the increased fringing fields from the gate to the source/drain regions, which weakens the control of gate over the channel. The high K and Si system results in unacceptable level of bulk fixed charge, high interface trap density and low silicon interface carrier mobility [17]. Consequently, extremely thin layer of interfacial oxide is used as a coating to reduce the interface trap density thus increasing the device performance [18]. The gate stack architecture (GSA) was proposed in order to reduce the gate leakage and leads to an enhancement of average electric field in the channel, thereby improving carrier transport efficiency [19, 20].

In order to incorporate the advantages of the dual metal gate (DMG) and gate stack architecture (GSA), novel device architecture is proposed known as Dual Metal Gate Stack Architecture (DMGSA) CGT/SGT MOSFET.

In this work, 2-dimensional analytical model is presented to examine the impact of the structure on various device characteristics. It has been established that (DMGSA) CGT/SGT MOSFET enhances short channel immunity and improved transport efficiency as compared to DMG CGT/SGT MOSFET. The accuracy of the model was verified by comparing the analytical results with simulated data obtained using ATLAS 3-D device simulator [21].

II. ANALYTICAL MODEL

The Schematic diagram of DMGSA CGT/SGT MOSFET is shown in Fig. 1. As can be seen from the diagram the workfunction of the metal gate electrode near the source end (Φ_{m1}) at channel length L_1 is greater than the workfunction of the metal gate electrode near the drain end (Φ_{m2}) at channel length L_2, such that the total channel length L (=$L_1 + L_2$). Also it can be observed, that t_1 is the thickness of oxide layer and t_2 is the thickness of the dielectric (high-k) layer. Furthermore the quantum effects are not considered in the present analysis as the channel length and device diameter is not less than 30 nm and 10 nm respectively [22].

Assuming that the influence of the charge carriers and fixed charges in the channel is uniform and can be neglected, the potential distribution in the silicon pillar, before the onset of strong inversion, can be written as

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\phi(r,z)}{\partial r}\right)+\frac{\partial^2\phi(r,z)}{\partial z^2}=\frac{qN_A}{\varepsilon_{si}} \qquad (1)$$

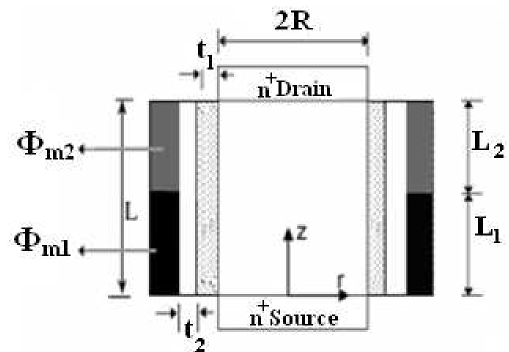

Fig. 1. Cross sectional view of DMGSA CGT/SGT MOSFET. Channel length, L=50 nm, Radius, R=10 nm, p type substrate doping $N_A=1 \times 10^{17}$ cm^{-3}, uniformly doped source/drain, $N_D=1 \times 10^{20}$ cm^{-3}, SiO_2 thickness t_1, High K Dielectric thickness t_2, workfunction of the metal gate electrode near the source end Φ_{m1}, workfunction of metal gate electrode near the drain end Φ_{m2}, dielectric permittivity of SiO_2 and high K dielectric ε_1 and ε_2 respectively.

where, N_A silicon film doping concentration $\phi(r,z)$ is the electrostatic potential in the silicon pillar.

The potential distribution in the silicon film is assumed to be a parabolic profile in the radial direction [23] and can be written as

$$\phi(r,z) = p_0 + p_1 r + p_2 r^2 \qquad (2)$$

where, p_0, p_1 and p_2 are the functions of z.

The Poisson‘s equation is solved using boundary conditions [24] to obtain the surface potential of the region.

In this device the metal gate electrode is made of two material of different workfunctions, the metal which is near the source end have workfunction, Φ_{m1} which is greater than the one having workfunction, Φ_{m2} near the drain end. On solving the Eq. (1) using the boundary conditions the surface potential for the two regions is obtained as

$$\frac{d^2\phi_{s1}(z)}{dz^2} - k^2\phi_{s1}(z) = \beta_1 \qquad (3)$$

for $0 \le z \le L_1$

$$\frac{d^2\phi_2(z)}{dz^2} - k^2\phi_{s2}(z) = \beta_2 \qquad (4)$$

for $L_1 \le z \le (L_1 + L_2)$

where, ϕ_{s1} and ϕ_{s2} are the surface potential under the gate near the source end and under the drain end respectively.

Where,

$$\beta = \frac{qN_A}{\varepsilon_{si}} - k^2(V_{gs} - V_{FB}) \qquad (5)$$

β_1 and β_2 are for the respective regions. V_{FB} = Flat Band Voltage

$$k^2 = \frac{2C_{ox}}{\varepsilon_{si} R} \qquad (6)$$

with
R = Radius of the Silicon Pillar

$$C_{ox} = \frac{\varepsilon_{ox}}{\left[R \ln\left(1 + \frac{t_{oxeff}}{R}\right)\right]} \qquad (7)$$

$$t_{oxeff} = t_1 + \frac{\varepsilon_1}{\varepsilon_2} t_2 \qquad (8)$$

t_{oxeff} is the effective silicon oxide thickness t_1 is the thickness of the SiO_2 (ε_1) layer and t_2 is the thickness of the high-k layer (ε_2).

On solving Eq (3) and (4) the following solution for the surface potential for each section is obtained as

$$\phi_{s1(z)} = A\exp(kz) + B\exp(-kz) - \frac{\beta_1}{k^2} \qquad (9)$$

for $0 \le z \le L_1$

$$\phi_{s2(z)} = C\exp(kz) + D\exp(-kz) - \frac{\beta_2}{k^2} \qquad (10)$$

for $L_1 \le z \le (L_1 + L_2)$

where,

$$A = \delta\left[2C_2 + C_3\left(\eta\eta_1^{-1} + \eta^{-1}\eta_1\right) - 2\eta^{-1}C_1\right] \qquad (11)$$

$$B = \delta\left[2C_1\eta - 2C_2 - C_3\left(\eta\eta_1^{-1} + \eta^{-1}\eta_1\right)\right] \qquad (12)$$

$$C = \delta\left[2C_2 - 2C_1\eta^{-1} + C_3\left(\eta^{-1}\eta_1^{-1} + \eta^{-1}\eta_1\right)\right] \qquad (13)$$

$$D = \delta\left[2C_1\eta - 2C_2 - C_3\left(\eta\eta_1 + \eta\eta_1^{-1}\right)\right] \qquad (14)$$

where,

$$\eta = \exp(k(L_1 + L_2)) \qquad (15)$$

$$\eta_1 = \exp(k(L_1)) \qquad (16)$$

$$\delta = \left[2(\eta - \eta^{-1})\right]^{-1} \qquad (17)$$

$$C_1 = \frac{\beta_1}{k^2} \qquad (18)$$

$$C_2 = \left(\frac{\beta_2}{k^2}\right) + V_{bi} + V_{ds} \qquad (19)$$

$$C_3 = \frac{(\beta_1 - \beta_2)}{k^2} \qquad (20)$$

The electric field distribution in the high metal workfunction and low metal workfunction region can be obtained by differentiating $\phi_{s1}(z)$ and $\phi_{s2}(z)$ respectively.

1. Minimum Surface Potential

The position at minimum of surface potential, $Z_{\min}$ is obtained by differentiating (9) with z and equating the result to zero, as

$$Z_{\min} = \frac{1}{2k} \ln\left[\frac{B}{A}\right] \tag{21}$$

Minimum surface potential, $\phi_{s\min}$ is then obtained from (9) as,

$$\phi_{s\min}(Z_{\min}) = 2\sqrt{AB} - \frac{\beta_1}{k^2} \tag{22}$$

2. Subthreshold Slope

Subthreshold slope, S is defined as

$$S = \frac{KT}{q} \log_{10}\left[\frac{1}{\frac{\partial(\phi_{s\min}(Z_{\min})}{\partial V_{gs}}}\right] \tag{23}$$

Using eq^n (22) in eq^n (23) subthreshold slope, S can be obtained as

$$S = \frac{KT}{q} \ln 10 \left[\frac{1}{\frac{1}{\sqrt{AB}}\left\{B\left(\eta\left[2\delta^{-1} - 2\right]\right) + A\left(\eta\left[2 - 2\delta\right]\right)\right\} + 1}\right] \tag{24}$$

III. RESULTS AND DISSCUSSION

The present analysis is carried out for a channel length, L=50 nm, device radius, R=10 nm, uniformly doped source/drain, N_D with doping density of 1 x 10^{20} cm^{-3}, p type substrate doping, N_A with a doping density of 10^{17} cm^{-3}, SiO_2 thickness, t_1=1 nm, High K dielectric thickness, t_2=4 nm, dielectric constant of SiO_2, ε_1=3.9, dielectric constant of High K dielectric, ε_2=20 the metal gate work function at the source end (Φ_{m1}) is 4.8 eV (Au) and metal gate work function at the drain end (Φ_{m2}) is 4.4 eV (Ti).

Fig. 2 shows the variation of surface potential along the channel for DMGSA CGT/SGT MOSFET and SMGSA CGT/SGT MOSFET devices at V_{gs}=0.2 V and V_{ds}=0.1 V. It can be seen that DMGSA and DMG CGT/SGT MOSFET exhibit a step function in the surface potential along the channel as compared to SMGSA and SMG CGT/SGT MOSFET. This step profile at the junction of two gate metal electrodes screens the region near the source end from the variations in the drain voltage and the increase in drain voltage is dropped across the drain region. Hence leads to reduction in drain induced barrier lowering (DIBL).

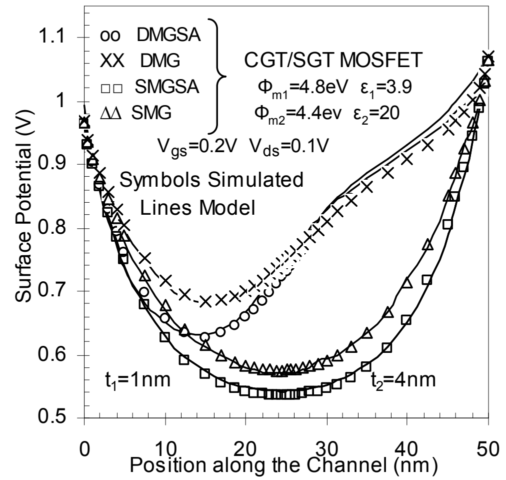

Fig. 2. Surface potential as a function of position along the channel, for DMGSA, DMG, SMGSA and SMG CGT/SGT MOSFET, at L=50 nm, N_A=1 x 10^{17} cm^{-3}, N_D=1 x 10^{20} cm^{-3}, V_{ds}=0.1 V and V_{gs}=0.2 V. Symbols show simulated data extracted from 3D ATLAS Device Simulator.

It is also found that with the increase in dielectric constant (ε_2 from 3.9 to 20) for DMGSA and SMGSA devices, the magnitude of minimum surface potential decreases which implies that the gate controllability is greatly enhanced by incorporating gate stack architecture. This further suppresses the short channel effects. The close agreement of the analytical results with simulated results validates the model.

Fig. 3 shows the variation of surface potential of DMGSA CGT/SGT MOSFET along the channel for different values of the dielectric constant of the upper oxide, ε_2. It is evident that as ε_2 increases the magnitude of minimum surface potential decreases for a change of ε_2 from 7 to 20, which implies that the gate controllability is greatly enhanced by using the stack architecture. Thus incorporation of DMG and stack architecture (for DMGSA) helps in suppressing the short channel effects and also leads to a considerable improvement in gate

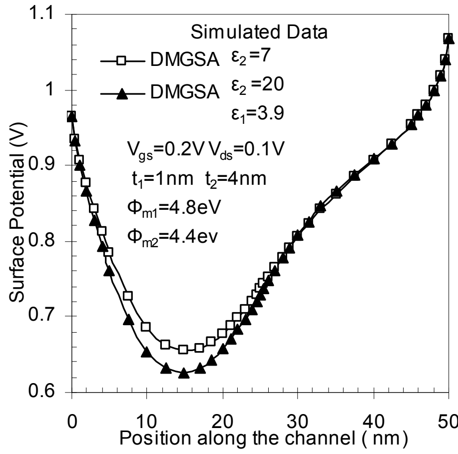

Fig. 3. Surface potential along the channel for different high K dielectric (ε_2) at V_{gs}=0.2 V, V_{ds}=0.1 V. At L=50 nm for DMGSA device.

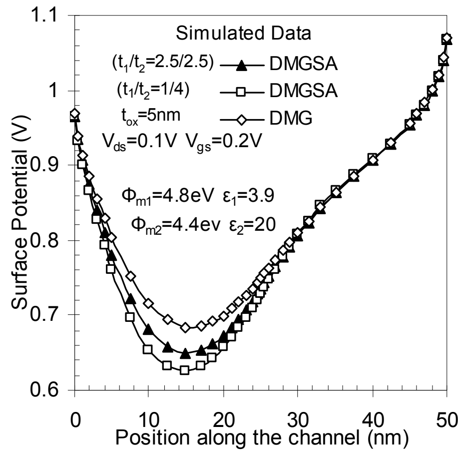

Fig. 4. Surface Potential along the channel for different values of t_1/t_2 ratio. At L=50 nm, V_{gs}=0.2 V and V_{ds}=0.1 V.

controllability. Even though ε_2 increases three times, its effect on oxide capacitance C_{ox} is very low as evident from (7) and (8). Thus the variation of surface potential with ε_2 will also be small.

Fig. 4 shows the variation of surface potential of DMGSA CGT/SGT MOSFET along the channel for different t_1/t_2 ratios. As evident from the Fig. 4 as well as from the Table 1, the surface potential decreases with the increase in thickness of high K dielectric material. The substantial decrease in surface potential with high K dielectric material in comparison to gate without high K dielectric material is also evident from the Fig. 4 and Table 1. So, use of high K dielectric material with higher thickness with respect to SiO_2 leads to better gate controllability.

In Fig. 5 the comparison of electric field distribution

Table 1.

	Surface Potential (V)		
	t_1:t_2 (DMGSA)		t_{ox} (nm) DMG
L (nm)	2.5:2.5	1:4	5
10	0.681783	0.65468	0.716464
14.94	0.650189	0.626464	0.684598
19.96	0.673014	0.656953	0.699775
25	0.735416	0.728769	0.749767
30.04	0.807001	0.807598	0.810798

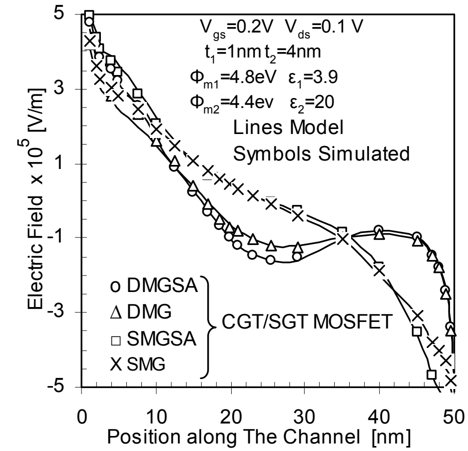

Fig. 5. Electric Field as a function of position along the channel, for DMGSA and SMGSA CGT/SGT MOSFET, at V_{ds}=0.1 V and V_{gs}=0.2 V. Symbols show simulated data extracted from 3D ATLAS Device Simulator.

along the channel has been shown for DMGSA, SMGSA, DMG and SMG CGT/SGT MOSFET at V_{ds}=0.1 V and V_{gs}=0.2 V. The analytical results are found to be in good agreement with the simulated data. From the figure it is observed that a peak in electric field is created for DMGSA and DMG as compared to SMGSA and SMG structures. This peak in electric field improves carrier transport efficiency there by suppressing SCEs. This electric field peak is created in the channel due to the lower gate electrode workfunction near the drain end. This leads to substantial reduction in electric field in case of DMGSA and DMG devices. The reduction in electric field at the drain end can be interpreted as a reduction in hot carrier effects, lower impact ionization and higher breakdown voltage. On incorporating stack architecture there is no big difference in electric field in DMGSA with DMG and SMGSA with SMG devices as observed from the figure. This is because electric field is derivative of surface potential, and from Fig. 2. it is observed that both the surface potential graph has same pattern which results in equal electric field. On keenly

observing the DMGSA and DMG devices there is a slight decrease in electric field near drain end for DMGSA. Same observation can be obtained between SMGSA and SMG devices.

Fig. 6 bar diagram shows the variation of subthreshold slope with different channel length for DMGSA, SMGSA, DMG and SMG CGT/SGT MOSFET. Due to the incorporation of dual metal architecture and gate stack design results in reduction of subthreshold slope for DMGSA as compared to DMG and SMG devices, implying better short channel immunity. However not much difference is seen for the case of SMGSA and DMGSA devices.

Fig. 7 shows the variation of minimum surface potential as a function of channel length at different radius R=10 nm, 20 nm and 30 nm. for DMGSA and DMG devices. It is demonstrated that for channel length above L=70 nm there is not much difference in the values of minimum surface potential for the three radii. However lower the value of channel length there is a considerable difference in the minimum surface potential for different R value. Furthermore there is a large decrease in minimum surface potential in DMGSA device as compared to DMG at R=10 nm, this is only due to the incorporation of gate stack architecture, which results in increase in device efficiency. The analytical results are found to be in good agreement with the simulated data.

In Fig. 8 the variation of subthreshold slope as a function of dielectric constant of the upper gate dielectric has been shown for DMGSA CGT/SGT MOSFET. The dielectric constant of the lower gate dielectric has been fixed at ε_1=3.9. It can be seen that subthreshold slope decreases with an increase in the dielectric constant of the upper dielectric layer. This is because with an increase in dielectric constant of the upper oxide, ε_2, the effective potential at the surface increases leading to a reduction in subthreshold slope. This clearly indicates that short channel effects are suppressed considerably by incorporating dual metal gate engineering and gate stack architecture in the CGT/SGT MOSFET.

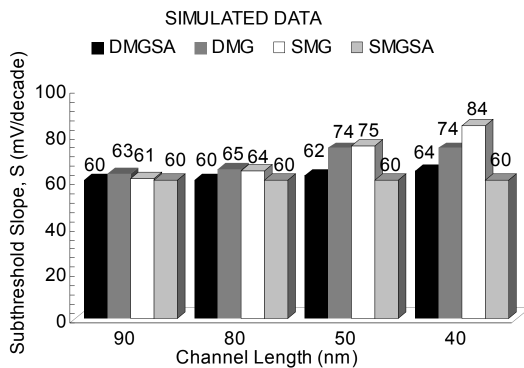

Fig. 6. Subthreshold Slope with respect to channel length for DMGSA, SMGSA, DMG and SMG CGT/SGT MOSFET. At V_{gs}=0.2 V, V_{ds}=0.1 V, R=15 nm, N_A=10^{16} /cm^{-3} and N_D= 5 x 10^{19} /cm^{-3}.

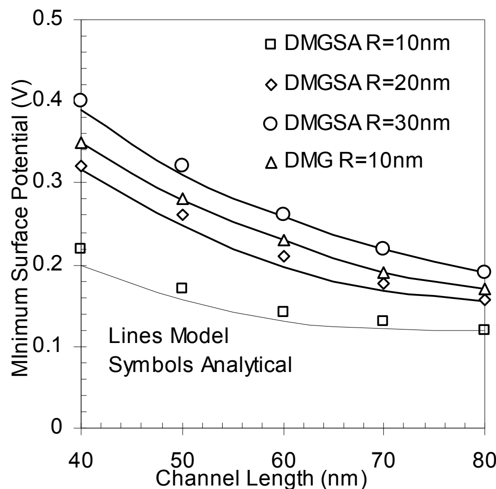

Fig. 7. Minimum surface Potential variation with respect to channel length for DMGSA and DMG devices. At V_{gs}=0.2 V, V_{ds}=0.1 V, R=15 nm, N_A=10^{16} /cm^{-3} and N_D=5 x 10^{19} /cm^{-3}.

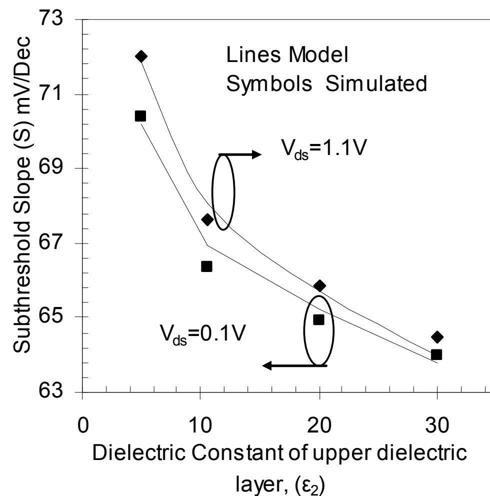

Fig. 8. Variation of subthreshold slope, S as a function of dielectric constant of upper dielectric layer for DMGSA CGT/SGT MOSFET. At V_{gs}=0.2 V, V_{ds}=0.1 V, R=15 nm, N_A=10^{17}/cm^{-3} and N_D=10^{20} cm^{-3}.

IV. CONCLUSIONS

A two dimensional analytical model for the novel device architecture DMGSA CGT/SGT MOSFET has been developed and its impact on the device characteristics has been discussed. The analytical results are compared with the simulated results obtained from ATLAS 3D device simulator and have been found in a good agreement. It has been analyzed that the DMGSA has a better screening from drain bias variation leading to a reduction in SCEs. A peak in the electric field profile results in reduction in hot carrier effect and impact ionization in DMGSA as compared to DMG and SMG devices. Further the reduction in subthreshold slope is direct consequence of gate stack architecture. Thus it has been demonstrated that incorporation of dual metal gate electrode design along with gate stack architecture leads to an improvement in short channel immunity and hot carrier reliability thereby ensures better carrier transport efficiency which results in better performance as compared to DMG and SMG designs.

ACKNOWLEDGMENT

Authors are grateful to University of Delhi and C.S.I.R for providing necessary financial assistance to carry out this research work.

REFERENCES

[1] J Tanaka, T Toyabe, S Ihara, S Kimura, H Noda, and K Itoh. “Simulation of sub-0.1-µm MOSFET’s with completely suppressed short-channel effect” *IEEE Electron Device Letters,*,Vol. 14, No. 8, pp. 396–399, 1993.

[2] P H Bricout and E Dubois. “Short-channel effect immunity and current capability of sub-0.1-micron MOSFET’s using a recessed channel” *IEEE Trans. Electron Devices,* Vol. 43, No. 8, pp. 1251–1255, 1996.

[3] K. K Young “Short channel effect in fully depleted SOI MOSFETs” *IEEE Trans. Electron Devices*, Vol. 36, No. 2, pp. 399-402, 1989.

[4] K Roy, H Mahmoodi, S Mukhopadhyay, H Ananthan, , H Bansal, and T Cakici. “Double-gate SOI devices for low-power and high-performance applications” *VLSI Design conference* 2006.

[5] Jong-Tae Park, Jean-Pierre Colinge, H Carlos, and Diaz “Pi-Gate SOI MOSFE” *IEEE Electron Device Letters*, Vol. 22, No. 8, pp. 405–406, 2011.

[6] Felice Crupi, Ben Kaczer, Robin Degraeve, Vaidy Subramanian, Srinivasan, Eddy Simoen Purushothaman, Abhisek Dixit, Malgorzata Jurczak, and Guido Groeseneken “Reliability Comparison of Triple-Gate Versus Planar SOI FETs” Vol. 53, No. 9, pp. 2351–2357, 2006.

[7] A Reinaldo. Vega and King Liu. Tsu-Jae “Three-Dimensional FinFET Source/Drain and Contact Design Optimization Study” *IEEE Trans. Electron Devices*; Vol. 56, No. 7, pp. 1483–1492, 2009.

[8] Tai-su Park, Euijoon Yoon, and Ho Lee Jong. “A 40 nm body-tied FinFET (OMEGA MOSFET) using bulk Si wafer” *International Symposium on Nanostructures and Mesoscopic Systems,* Vol. 19, No. 1-2, pp. 6–12, 2003

[9] A. Kranti, S. Haldar, and R. S Gupta. “An accurate 2D analytical model for short channel thin film fully depleted cylindrical/surrounding gate (CGT/SGT) MOSFET” *Microelectronics Journal*, Vol. 32, pp. 305–313, 2001.

[10] Pujarini Ghosh, S. Haldar, R. S Gupta, and M. Gupta. “An Analytical Drain Current Model for Dual Material Engineered Cylindrical/Surrounded Gate MOSFET” *Microelectronics Journal,*Vol. 43 pp. 17–24, 2012.

[11] Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R. S Gupta. “Impact of graded channel (GC) design in fully depleted cylindrical/surrounding gate MOSFET (FD CGT/SGT) for improved short channel immunity and hot carrier reliability” *Solid-State Electronics,* Vol. 51, pp. 398–404, 2007.

[12] H Takato, K Sunouchi, N Okabe, A Nitayama, K Hieda, F Horiguchi, et.al “Impact of surrounded gate transistor (SGT) for ultra-high- density LSI‘s” *IEEE Trans. Electron Devices* Vol. 38, No. 3, pp. 573–578, 1991.

[13] S Wtananabe, K Tsuchida, D Takashima, Y Oowaki, A Nitayama, K Hieda, et al. “A novel circuit technology with surrounded gate transistor (SGT’s) for ultra high density DRAM’s” *IEEE Journal of Solid State Circuit*. Vol. 30, No. 9, pp. 960–970, 1995.

[14] A Nitayami, H Takato, N Okabe, K Sunouchi, K

Hieda, F Horiguchi, et al. "Multi-Pillar surrounding gate transistor (M-SGT) for compact and high-speed circuits" *IEEE Trans. Electron Devices* Vol. 38, No. 3, pp. 579–583, 1991.

[15] W. Long, H. Kuo, J. M Ou, and K. K Chin, "Dual-material gate (DMG) field effect transistor", *IEEE Trans. Electron Devices*.1991;46, No. 5, pp. 865–870, 1991.

[16] Polishchuk, P Ranade, T. J King, and C Hu. "Dual work function metal gate CMOS technology using metal interdiffusion", *IEEE Electron Device Letters.*, Vol. 22, No. 9, pp. 444–446, 2001.

[17] B Cheng, M Cao, R Rao, A Inani, P. V Voorde, and W.M Greene, "The Impact of High K dielectris and metal gate electrods on sub-100nm MOSFET's", *IEEE Trans. Electron Devices.*, Vol. 46, No. 7, pp. 1537-1543, 1999.

[18] A Inani., R. V Rao, B Cheng, and J Woo. "Gate stack architecture analysis and channel engineering in deep sub-micron MOSFETs", "Japanese Journal of Applied Physics", Vol. 38, No. 4B, pp. 2266–2271,1999.

[19] M Saxena., S Haldar., M Gupta, and R. S Gupta. "Modeling and simulation of asymmetric gate stack (ASYMGAS)-MOSFET". *Solid State Electronics*, Vol. 47, No. 11, pp. 2131–2134, 2003.

[20] E. Fathi, A. Behnam, P Hashemi, B Esfandyarpour, and M. Fathipour "The influence of the stacked and the double material gate structures on the short channel effects in SOI MOSFETs", *IEICE Trans Electron E88-C*, Vol. 6, pp. 1122–1126, 2005.

[21] ATLAS 3D DEVICE Simulator, SILVACO International 2012.

[22] Y Naveh and K. K Likharev. "Modeling of 10nm scale ballistic MOSFETs." *IEEE Electron Device Letters.* Vol. 21, No. 5, pp. 242-244, 2000.

[23] K. K. Young, "Short-channel effect in fully depleted SOI-MOSFETs," *IEEE Trans. Electron Devices,* Vol. 36, No. 2, pp. 399–402, 1989.

[24] C. P. Auth and J. D. Plummer. "Scaling theory for cylindrical, fully depleted, surrounding-gate MOSFET's" *IEEE Electron Device Letters.* Vol. 39, No. 2, pp. 74–76, 1991.

Pujarini Ghosh was born in Assam, India, in 1985. She received the B.A Sc (H) Electronic Science from University of Delhi and M.Sc. Electronics from Jadavpur University in the year 2006 and 2008 respectively. Her doctoral Research involves the modeling design and simulation of gate material engineered Surrounded /Cylindrical Gate MOSFET for RF IC applications. She is currently working as University Teaching Assistant (UTA), University of Delhi. Currently she has authored 14 international journals and international conference proceedings. Her other areas of interest and activities cover VHDL and P Spice implementation.

Subhasis Haldar was born in India in 1967. He received the B. Sc (Hon.) and M. Sc degrees both in physics and the Ph.D Degree in electronics from University of Delhi. In 1988, 1990 and 1995 respectively. He joined the SDRL , Department of electronic Science, University of Delhi, South Campus in 1991 and developed analytical models of both MOSFET and MESFET devices. HE joined Moti Lal Nehru College, University of Delhi in 1993 as a lecturer and is now associate professor. Currently his area of interest is in miniaturization of devices, study and suppression of hot carrier effects considering LDD and FOLD structures, single and double gate MOSFET, Surrounded/ Cylindrical gate MOSFET and poly silicon. Currently he has 175 technical papers published in various journals and conference proceedings. Dr. Haldar was a member of ISRAMT'93, APMC 2004 and ISMOT 2009. He was joint secretary of APMC'96.

R. S. Gupta received B Sc. and M Sc. degrees from Agra University India in 1963 and 1966 respectively and the Ph.D degree in electronic engineering from the Institute of Technology, Banaras Hindu University, Varanasi, India, in 1970.

In 1971, he was with Ramjas College, University of Delhi, Delhi, India. In 1987, he was with the Department of Electronic Science, University of Delhi South Campus, New Delhi, India, as a Reader and later as a Professor from 1997 to 2008, later he was an Emeritus Scientist and with the Semiconductor Devices Research Laboratory. Currently is with Maharaja Agrasen Institute of Technology He heads several major research projects sponsored by the Ministry of Defence, the Department of Science and Technology, the Council of Science, and the Industrial Research and University Grants Commission. In 1988, he was a Visitor with the University of Sheffield, Sheffield, U.K., under the ALIS Link exchange program and also visited several U.S. and Spanish universities in 1995 and 1999, respectively. He also visited the Czech Republic in August 2003; Korea in November 2003; RPI Troy, NY, in August 2004, and China in December 2005. He has authored or coauthored over 580 papers in various international and national journals and conference proceedings. He contributed the chapter entitled “MOSFET Modeling” in the Encyclopedia on RF and Microwave Engineering (Wiley, 2005). He has supervised 46 Ph.D. students. His current interests and activities cover modeling of SOI submicrometer MOSFETs and LDD MOSFETs, modeling and design of HEMTs, hot-carrier effects in MOSFETs, and modeling of GaAs MESFETs for high-performance microwave and millimeter-wave circuits and quantum effect devices. Dr. Gupta was an Executive Member of the IEEE Electron Devices (ED)/ Microwave Theory and Techniques (MTT) Chapter India Council. His name has also appeared in the Golden List of IEEE TRANSACTIONS ON ELECTRON DEVICES in December 1998, 2002, and 2004. He is a Fellow of the Institution of Electronics and Telecommunication Engineers (India), a Life Member of the Indian Chapter of the International Centre for Theoretical Physics (ICTP), and a Life Member of the Semiconductor Society of India. He was the Secretary of ISRAMT’93 and the 1996 Asia-Pacific Microwave Conference (APMC’96), and the Chairman of the Technical Programme Committee of APMC’96. He edited the proceedings of both of these international conferences. He was the Chairman of APMC’2004, held in New Delhi, India, in December 2004.

Mridula Gupta received the B.Sc. degree in physics, the M.Sc. degree in electronics, the M.Tech. degree in microwave electronics, and the Ph.D degree in optoelectronics from the University of Delhi, Delhi, India, in 1984, 1986, 1988, and 1998, respectively. Since 1989, she has been with the Department of Electronic Science, University of Delhi South Campus, New Delhi, India, where she was previously a Lecturer and is currently an Associate Professor and with the Semiconductor Devices Research Laboratory. She has authored or coauthored approximately 312 publications in international and national journals and conference proceedings. She has supervised 14 Ph.D. students. She contributed the chapter entitled “MOSFET Modeling” in the Encyclopedia on RF and Microwave Engineering (Wiley, 2005). Her current research interests include modeling and simulation of MOSFETs, MESFETs, and HEMTs for microwave-frequency applications. Dr. Gupta is a Fellow of the Institution of Electronics and Telecommunication Engineers (India) and a Life Member of the Semiconductor Society of India. She was the Secretary of the 2004 Asia–Pacific Microwave Conference, and was General Secretary of 12th ISMOT 2009 which were held in New Delhi, India.