Assessment of Ambipolar Behavior of a Tunnel FET and Influence of Structural Modifications

Rakhi Narang*, Manoj Saxena, R. S. Gupta***, and Mridula Gupta***

Abstract—**In the present work, comprehensive investigation of the ambipolar characteristics of two silicon (Si) tunnel field-effect transistor (TFET) architectures (i.e. p-i-n and p-n-p-n) has been carried out. The impact of architectural modifications such as heterogeneous gate (HG) dielectric, gate drain underlap (GDU) and asymmetric source/drain doping on the ambipolar behavior is quantified in terms of physical parameters proposed for ambipolarity characterization. Moreover, the impact on the miller capacitance is also taken into consideration since ambipolarity is directly related to reliable logic circuit operation and miller capacitance is related to circuit performance.**

Index Terms—**Ambipolar, gate drain underlap (GDU), heterogate (HG), p-i-n, p-n-p-n, tunnel FET**

I. INTRODUCTION

In order to utilize the advantage of tunnel FET as a low subthreshold swing device [1, 2] as demonstrated recently for complementary n-type and p-type TFET [3, 4] as well and a possible candidate for low power digital circuit applications, its major impediements i.e. ambipolar behavior [5], high miller capacitance [6] and low ON current [7] should be overcome. Ambipolarity means conduction in two directions (i.e. both for positive gate voltage and negative gate voltage). It is caused due to the transfer of tunnel junction from source side to the drain side when the gate voltage $V_{gs} < 0$ for an n-type TFET operation. The basic requirement for an ideal switch in digital circuits is to work in only one direction, but if it also starts conducting in other direction this can create a problem in complementary logic circuit applications and thus limits the utility of the device for digital circuit design. However, if ambipolar conduction is completely suppressed or minimized over large negative voltage ranges (for n-type TFET operation), then the circuit operation can be reliable. The TFET based circuits can work well till the leakage current ($I_{off} = I_{ds}$ @ V_{gs}=0 V) and the ambipolar current ($I_{amb}=I_{ds}$ @ $V_{gs} < 0$ V) are below the ITRS level defined for a particular technology node in order to have minimum static leakage power and reliable circuit operation. Since the ambipolar characteristic is an inherent property of TFET architecture, different structural modifications are investigated which can suppress this behavior. These architectural modifications also affect the ON current and miller capacitance of the device. In this work, we have tried to propose and discuss the parameters which can quantify the ambipolar behavior of Si-based TFET and helps to choose a suitable architecture. The ambipolarity is characterized in two forms: graphically for generalized understanding and by formulating the parameters for device design issues. Two most extensively discussed TFET architectures are studied viz. conventional p-i-n and p-n-p-n TFET. Using these two basic architectures, the impact of various architectural modifications such as heterogeneous gate (HG) dielectric (with high-k material at the source side and low-k at the drain end) [8], gate

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drain underlap (GDU) [5, 9], and lower drain doping [10] on the ambipolarity of both p-i-n and p-n-p-n is then quantified. The above mentioned architectural variations results in high barrier width at the drain end which stops the tunneling leakage between the drain/channel junction and thus helps in suppression of ambipolar behavior. Since both the ambipolar and miller capacitance have direct impact on the performance of TFET based logic circuitry, thus these two characteristics should be studied together and not as independent properties in order to compare the trade-offs. The reference structures are the p-i-n and p-n-p-n [11] TFET with symmetric source/drain doping, completely aligned gate with source/drain and a high-k gate dielectric material. Some recent reports have studied the ambipolar characteristics and investigated in particular the gate-drain underlap architecture. The advantage of hetero-junction TFET has also been reported to prevent the ambipolar conduction [12]. In this work we study a HG architecture (which was proposed as one of the alternative to achieve high I_{on} as well as suppression of ambipolar behavior [8]) along with GDU and asymmetric source/drain doping. The optimization of length of low-k and high-k dielectric is also done in order to achieve low ambipolar conduction as well as a lower miller capacitance. Thus, different kind of architectural modifications reported till now for performance enhancement and specifically to overcome the ambipolar behavior are scrutinized, quantified and compared with each other together in this work in order to choose the best architecture for reliable complementary circuit performance point of view. This comprehensive theoretical investigation will give designers an insight into the ambipolar behavior related with different architectures and the ambipolar parameter will give quantification and graphical representation of the severity of ambipolarity.

II. Device Architecture Description and Simulation

The device structure considered in this study and the various structural modifications are shown in Fig. 1 and Table 1. The device parameters are as follows: Source/Drain doping i.e. $N_a=N_d=10^{20}$ cm^{-3} (Symm) for symmetric structure and $N_d=5 \times 10^{18}$ cm^{-3} (Asymm) for asymmetric structure, Channel length, L=45 nm, channel

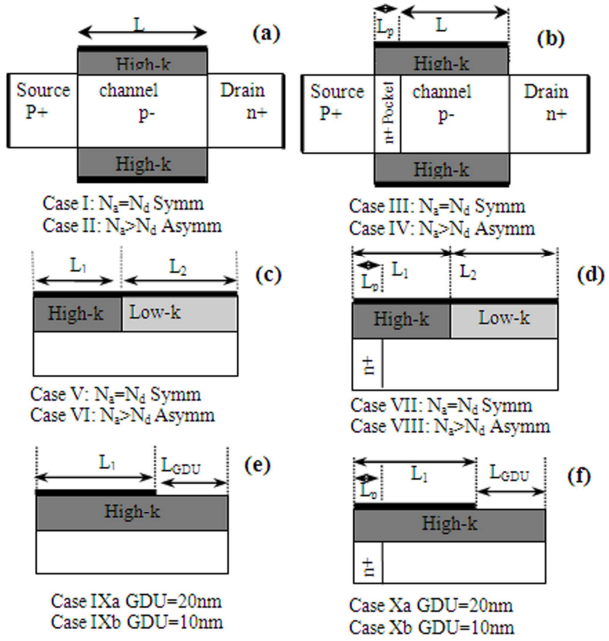

Fig. 1. Schematic of the different structural modifications of p-i-n and p-n-p-n TFET.

Table 1. Structural specifications for the cases shown in Fig. 1

Case	Device	Doping	GDU (nm)
I	p-i-n	Symmetric	0
II	p-i-n	Asymmetric	0
III	p-n-p-n	Symmetric	0
IV	p-n-p-n	Asymmetric	0
V	HG p-i-n	Symmetric	0
VI	HG p-i-n	Asymmetric	0
VII	HG p-n-p-n	Symmetric	0
VIII	HG p-n-p-n	Asymmetric	0
IXa	p-i-n	Symmetric	20
IXb	p-i-n	Symmetric	10
Xa	p-n-p-n	Symmetric	20
Xb	p-n-p-n	Symmetric	10

thickness t_{si}=10 nm, gate oxide thickness t_{ox}=3 nm, pocket width for p-n-p-n structure L_P=3 nm, pocket doping (n-type)=5 x 10^{19} cm^{-3}, permittivity of high-k $\varepsilon=21\varepsilon_0$ (HfO_2) and low-k=$3.9\varepsilon_0$ (SiO_2). Since the experimental data for all the possible architectures studied in this work are not available, so the non-local band to band tunneling model [13] used for simulation (which basically accounts for the current conduction mechanism in tunneling based devices) is calibrated with the experimentally measured results of a Si NW tunnel FET [14] by tuning the effective electron and hole masses. Various physical models activated along with non-local tunneling model are band gap narrowing (BGN),

concentration and field dependent mobility, Hurkx recombination model, and generation recombination model. The impact of HG structure, lower drain doping and gate drain underlap on the energy band diagram in the off state (V_{gs}=0 V, V_{ds}=1 V) and ambipolar state (V_{gs}=-0.5V, V_{ds}=1 V) are shown in Fig. 2. The barrier width at the drain end decreases for V_{gs}=-0.5 V and is minimum in case of p-i-n TFET, hence p-i-n TFET suffers from severe ambipolar conduction. The structural change increases the barrier width at the drain side and thus helps in avoiding the ambipolar conduction. The impact of these modifications will be studied in detail in next section where the behavior will be quantified and their impact will be studied. In this section, all the structures considered in this study with their advantages and disadvantages are discussed briefly. The problems associated with a lower drain doping and gate drain underlap structure is the non-scalability of drain region [1] and thus reduced chip packing density. Another disadvantage associated with asymmetric drain doping is an additional process step in the fabrication procedure. The gate drain underlap structure even with low drain doping requires a drain spacer of minimum length in order to suppress ambipolarity effectively and thus limits

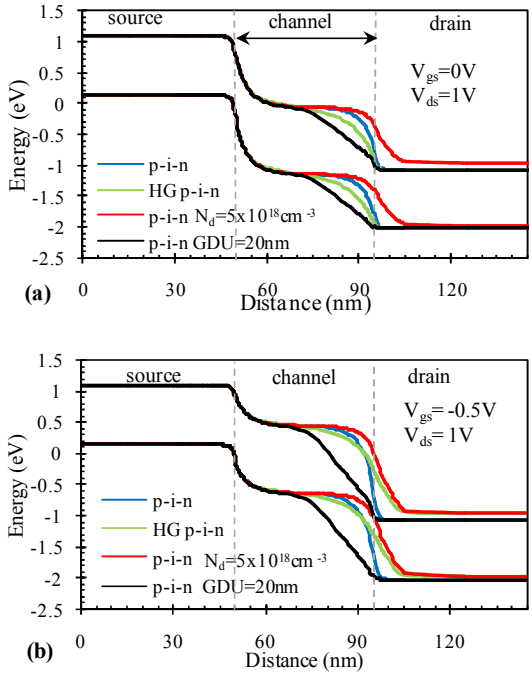

Fig. 2. Energy band diagram in the (a) off (V_{gs}=0, V_{ds}=1 V), and (b) ambipolar state (V_{gs}=-0.5 V, V_{ds}=1 V) for different structures.

the device scalability and even brought into question the utility of a planar architecture [15]. While the HG structure does not pose a non-scalability problem, the only requirement would be the optimization of high-k and low-k oxide length. Moreover, the fabrication of planar HG TFET can be obtained by the Ar-IBEE (Argon ion-bombardment-enhanced etching) process of low-k SiO_2 and then deposition of high-k dielectric i.e. HfO_2 adopting the technique mentioned for making asymmetric gate oxide thickness four terminal FinFET structure [16]. The process steps suggested in [16] can be adopted to fabricate a vertical double gate heterogeneous gate dielectric TFET as well. This kind of asymmetric gate dielectric profile has also been reported for lateral diffusion MOSFET [17] where a thin dielectric is grown on the source side to achieve high electric field and a thicker gate oxide on the drain side to reduce it, which is quite similar in its effect with the heterogeneous gate dielectric.

III. Formulation of Ambipolar Characteristic Parameter

An earlier work reported for ambipolarity characterization utilizes a long channel reference structure to quantify the factor [18, 19]. But, in our formulation, to compare different architectures the I_{off} is fixed at a certain level (i.e. 0.1 pA/μm) and then the factors are quantified. Before the quantification of ambipolar behavior through physical parameters, different cases of ambipolar current characteristics have been explained through graphical representation and then the parameters are formulated. There are two physical parameters considered to characterize the off-state conduction. The characteristic parameter are chosen on the basis of what should be the ideal behavior (no conduction at all as in the case of a MOSFET, device remains off in the negative V_{gs} regime) and then how the characteristic deviate from it. This can be understood with the help of graphical representation shown in Fig. 3. The different cases are classified in terms of geometrical figures (rectangle, trapezoid and triangle). Fig. 3(a) shows the best case where I_{amb} is completely suppressed over the complete negative V_{gs} range, when θ_2=180˚ and this happens to be the ideal case. Fig. 3(b) shows the case inferior to (a) represented by a trapezoid, wherein the I_{amb}

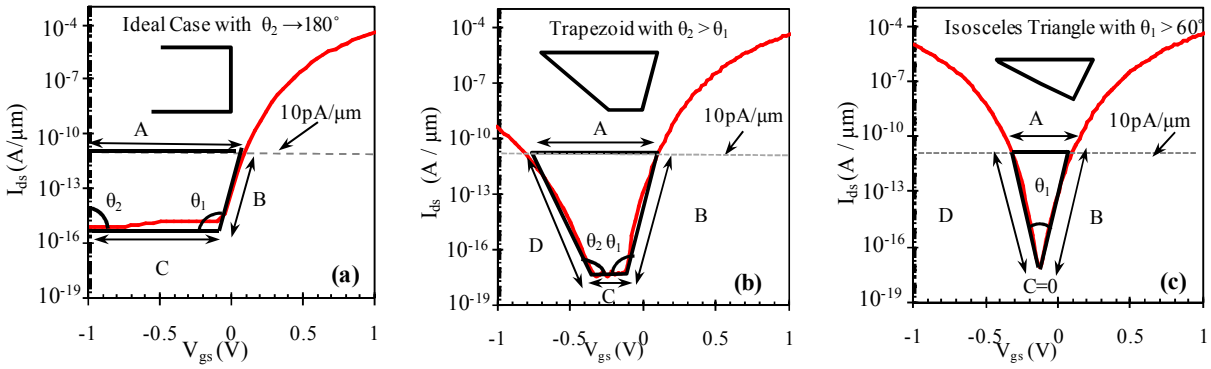

Fig. 3. (a), (b) and (c) Graphical Representation for three different cases of ambipolar characteristics and their analogy with geometrical shapes for quantification.

remains below the level of 10 pA/μm for a voltage range represented by side A. This type of trend can become much better if the θ_2 becomes much higher than θ_1, since in that case I_{amb} will be lower than 10 pA/μm for a large negative voltage range which is desirable. Fig. 3(c) depicts the worst case with severe ambipolar behavior wherein the trapezoid has reduced to a triangle due to side C becoming zero and I_{amb} starts increasing. This case can become a little better if the θ_1 of the triangle becomes greater than 60° or in other words, the triangle becomes isosceles and gives I_{amb} lower than 10 pA/μm for a large negative V_{gs}. Based on the above explanation, two parameters can be defined which quantitatively describes the ambipolar behavior. First parameter quantifies the range of negative gate voltage (V_{gs}) till which the ambipolar current is well below the ITRS limit of 10 pA/μm for low standby power (LSTP) applications and is termed as V_{Tamb}. Another parameter defined to characterize the rise and fall of the current in the negative gate bias region, which quantifies how fast the device goes into the complete off state and the ambipolar current again rises. This parameter is similar to what is defined as subthreshold swing (S) in case of MOSFET which is a measure of how fast the device goes from OFF to ON state, which in this case can be termed as ambipolar slope (as shown in Fig. 4(a)) representing how fast the device attains the off-state (given by $SS_{amb(1-0)}$) and comes out of off state (given by $SS_{amb(0-1)}$) in ambipolar region.

$$S = \frac{dV_{gs}}{d\log(I_{ds})}$$

From Fig. 4(a) and the graphical representation shown in the form of trapezoid in Fig. 3(b), it can be derived that the slope of the side B ($SS_{amb(1-0)}$) should be as steep as possible such that device instantly goes in the OFF state and the slope of the side D ($SS_{amb(0-1)}$) should be as large as possible in order to have lower I_{amb} for a large range of negative gate voltages and thus better suppression. In case of TFET it is possible to achieve subthreshold slopes lower than 60 mV/dec (limit for conventional MOSFET), thus the ambipolar slope could also be below this value as shown in the results. The quantitative analysis based on these two factors, to characterize the severity of ambipolar characteristics for various architectures studied in this work are discussed in *Section V*.

IV. Impact of Structural Modifications

The ambipolar behavior for p-i-n and p-n-p-n is almost similar (as also reported in experimental demonstrations [20]) because the difference in both the structure lies at

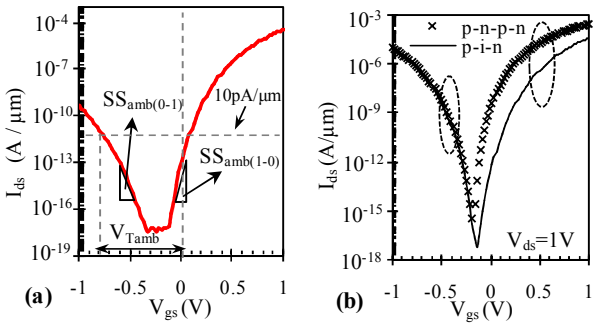

Fig. 4. (a) Ambipolar factors description, (b) Comparison of I_{ds}-V_{gs} characteristics of p-i-n and p-n-p-n TFET for similar gate metal workfunction, showing the similarity in ambipolar behavior and difference in the ON state.

source end and not at the drain end. The I_{ds}-V_{gs} characteristics (Fig. 4(b)) is shifted and this difference is due to the different threshold voltage of two devices (lower threshold for p-n-p-n) due to increased electric field for p-n-p-n. Fig. 4(b) is for the non-optimized case where all the parameters are similar for p-i-n and p-n-p-n TFET. This has been done to show the difference in the drain current characteristics of p-i-n and p-n-p-n TFET structure. For all other cases (unless it is mentioned), the devices are optimized to have similar off current (I_{ds} @ V_{gs}=0 V) to be equal to 0.1 pA/μm to study the ambipolar behavior accurately.

1. Optimization of High-k and Low-k Length for HG Architecture

As discussed in [8], the length of low-k and high-k gate dielectric can be optimized so as to obtain a high I_{on}, small SS and low I_{amb}. In this study, we also take into consideration the impact of different length of high-k and low-k dielectric on the ambipolar behavior as well as the gate capacitance (specifically the gate drain capacitance) component which basically determines the switching speed of the device. The length of high-k dielectric on the source side is varied from a lowest value of L_1=5 nm to a maximum of L_1=35 nm for a gate length of 45 nm. The impact on I_{ds}-V_{gs} characteristics is depicted in Fig. 5(a). For the extreme case of L_1=5 nm and L_2=40 nm, the I_{on} is reduced, although I_{off} is also low, but the ambipolar behavior is similar to rest of the cases.

Meanwhile, if L_1 is increased to its highest value of 35 nm, the ambipolar characteristic degrades and the gate capacitance and gate-drain capacitance increases monotonically (at high V_{gs}) with increase in length of high-k (L_1). Thus, the optimum value of L_1 is taken as 10 nm in order to achieve high I_{on}, low I_{amb} and low C_{gg} and C_{gd}. Similar is the case with optimization of L_1 and L_2 for HG p-n-p-n structure (Fig. 5(b)). Although in case of p-n-p-n TFET, the variation of L_1 and L_2 does not bring a very drastic change in the I_{ds}-V_{gs} characteristics in comparison to a HG p-i-n TFET, but the impact on C_{gg} and C_{gd} is appreciable. So, in case of HG p-n-p-n TFET the optimum value of L_1 is also considered as 10 nm. Thus, variation of the ratio of L_1 and L_2 also results in varying capacitance characteristics of TFET (Fig. 6) and thus the switching characteristics of the device.

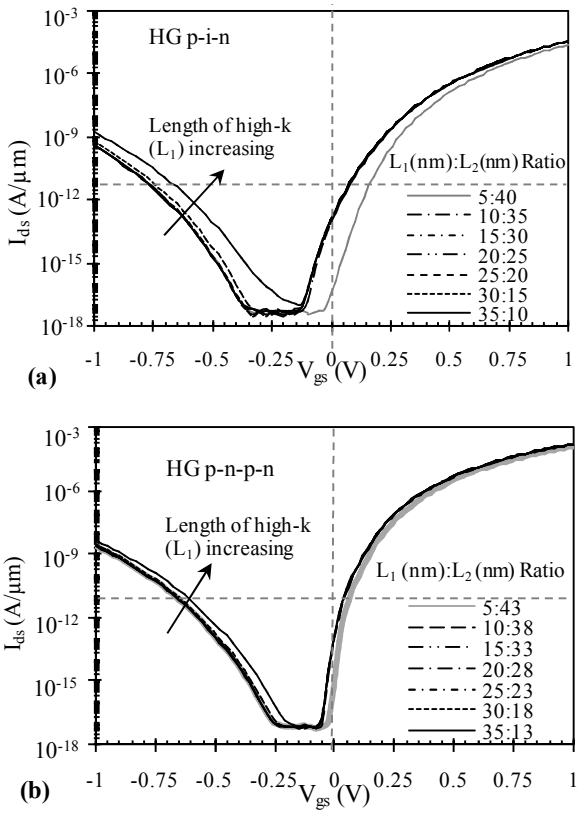

Fig. 5. Optimization of high-k (L_1) and low-k (L_2) length with L_1 varying from 5 nm to 35 nm for (a) HG p-i-n TFET, (b) HG p-n-p-n TFET. V_{ds}=1 V.

Table 2. Capacitance components (at V_{gs}=V_{ds}=1 V) and switching delay for all the cases depicted in Fig. 1

	C_{gg} (fF/μm)	C_{gd} (fF/μm)	τ (ps)
Case I	1.34	1.23	35.17
Case II	1.52	1.29	40.64
Case III	0.768	0.56	4.34
Case IV	1.66	1.12	10
Case V	0.41	0.311	11.14
Case VI	0.45	0.324	12.4
Case VII	0.348	0.152	2.04
Case VIII	0.492	0.27	3.04
Case IX a	0.725	0.59	17.81
Case IX b	0.997	0.873	24.44
Case X a	0.727	0.42	4.13
Case X b	0.668	0.457	3.77

As mentioned above that the HG helps in reducing the gate capacitance, Table 2 shows the reduction in the gate capacitance of a HG TFET over TFET and the impact of asymmetric drain doping on the capacitance voltage characteristics.

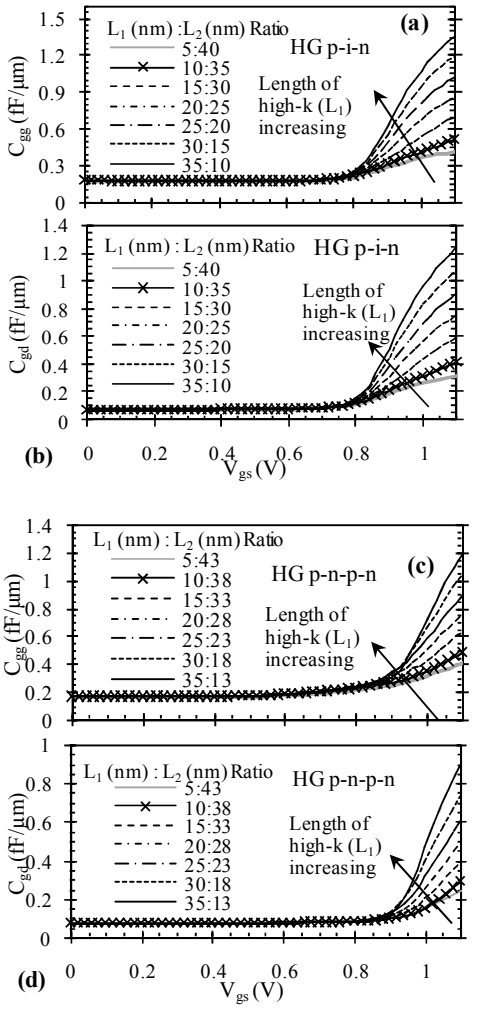

Fig. 6. Capacitance components for different L_1, L_2 combinations for (a), (b) HG p-i-n (c), (d) HG p-n-p-n TFET. V_{ds} = 1 V.

2. Impact of Asymmetric Source/Drain Doping and Gate Drain Underlap

The asymmetric source/drain doping drastically reduces the ambipolarity as shown in Fig. 7. Moreover, (as also discussed in earlier studies) p-n-p-n TFET exhibits lower sub-threshold swing, the slope $SS_{amb(1-0)}$ is lower in case of p-n-p-n TFET in comparison to p-i-n. For both p-i-n and p-n-p-n TFET, I_{amb} remains lower than 10 pA/μm till -1V V_{gs}.

In comparison to a single gate dielectric TFET, Heterogeneous Gate dielectric suppresses the ambipolar conduction and the suppression can be further improved if the drain is doped asymmetrically as shown in Fig. 7. Thus for a hetero-gate structure with L_1, L_2 optimized and asymmetric drain doping, the ambipolar conduction

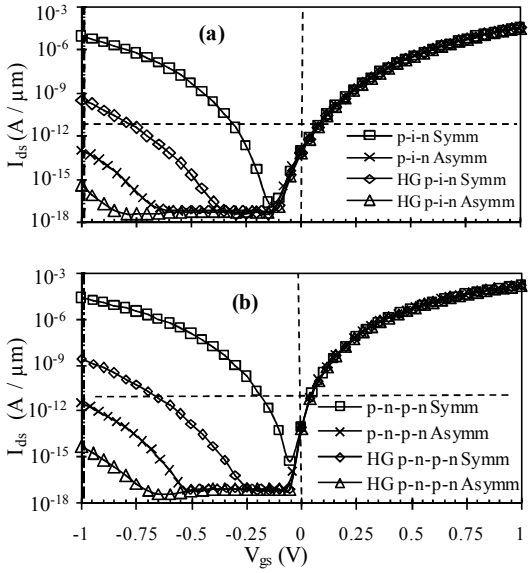

Fig. 7. Impact of lower drain doping on the ambipolar behavior of (a) p-i-n, and (b) p-n-p-n TFET. V_{ds}=1 V.

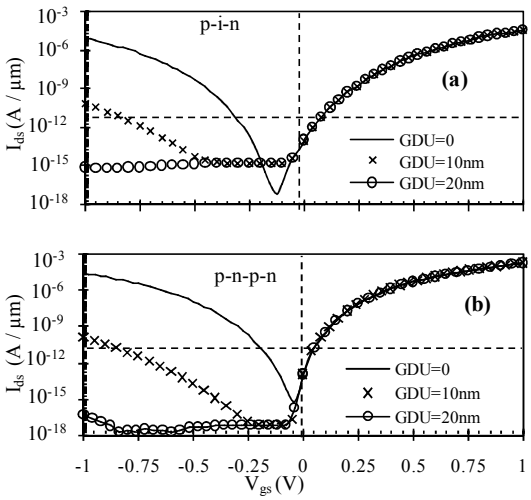

Fig. 8. Impact of varying gate drain underlap on the ambipolar conduction on (a) p-i-n TFET, (b) p-n-p-n TFET. V_{ds}=1 V.

can be suppressed completely. Although the ambipolar behavior gets suppressed but the capacitance component increases for a lower drain doping structures, so the gate delay ($\tau = C_{gg} V_{dd}/I_{on}$) [9, 21] will increase (Table 2). While a lower drain doping for HG-TFET architecture increases C_{gg} and C_{gd} (Table 2), but the values are much lower in comparison to a single high-k dielectric p-i-n and p-n-p-n TFET. The gate drain underlap technique is also effective in suppressing the ambipolar conduction. As shown in Fig. 8 that for a better suppression, a longer underlap length and drain spacer is required which limits the scalability for such kind of architectures as also

reported by Hraziia et. al [14] and for shorter drain spacers the lower drain doping also fails to suppress the ambipolar conduction.

Under this condition it is beneficial to consider a HG architecture with asymmetric drain doping in order to suppress the ambipolar conduction and also achieving a lowest value of gate capacitance as the values obtained for a p-i-n, p-n-p-n TFET with GDU architecture are still higher than a HG p-i-n and p-n-p-n TFET structure (Table 2). Thus, there is trade-off between a larger GDU with high gate capacitance but lower ambipolar conduction and non-scalability issues, or HG TFET with lower drain doping to have lower ambipolar conduction as well as lowest gate capacitance and hence low gate delay or fast switching time. The minimum GDU (10 nm) also suffers from ambipolar conduction and has even higher C_{gg} (Table 2).

V. Combinational Circuit Operation and Impact of Ambipolarity

The architectural modifications primarily increases the design window which is taken as the negative gate voltage range over which I_{amb} remains below 10 pA/µm also defined in this work as V_{Tamb} as shown in Table 3. The cases (II, IV, VI, IX (a) and X (a)) for which V_{Tamb} is not mentioned in Table 3 are the ones in which I_{amb} remains below 10 pA/µm even till V_{gs}=-3V. Thus, wider the design window the circuit operation is reliable and static power dissipation does not exceed the limit. Earlier work discusses conceptually static power dissipation enhancement in the pull-down network and spurious flipping of the output from high to low for a NAND circuit [19]. We explain the concept of design window (V_{Tamb}) and relevance of SS_{amb} and the reliability of circuit operation for an ambipolar device qualitatively (i.e without performing circuit simulation due to lack of compact analytical model available for TFET [22, 23]) using a two input Complementary TFET NAND circuit diagram as shown in Fig. 9. The main idea is to understand how ambipolarity can deteriorate performance of circuits based on TFETs and comparison of the prospective designs that can curb it. Fig. 9(a) and (b) shows the respective polarities of terminal voltages when the input is A=0, B=0 and A=0, B=1. For these input combination the V_{gs} value for n-TFET 1 is negative.

Table 3. Ambipolar parameters V_{Tamb}, SS_{amb} and α_{amb} for cases depicted in Fig. 1

	V_{Tamb} (V)	$SS_{amb\,(1\text{-}0)}$ (mV/dec)	$SS_{amb\,(0\text{-}1)}$ (mV/dec)	$\alpha_{amb} = SS_{amb\,(0\text{-}1)} / SS_{amb(1\text{-}0)}$
Case I	-0.32	30.4	25.2	0.83
Case II	--	33.2	100	3.01
Case III	-0.21	22.2	31.4	1.41
Case IV	--	14.4	102	7.08
Case V	-0.795	30.3	57.5	1.9
Case VI	--	29.8	81.1	2.72
Case VII	-0.66	18.1	73.4	4.05
Case VIII	-2.35	14.4	100	6.94
Case IX a	--	55.7	--	--
Case IX b	-0.87	58.0	103	1.77
Case X a	--	14.4	124	8.61
Case X b	-0.825	17.9	83.8	4.68

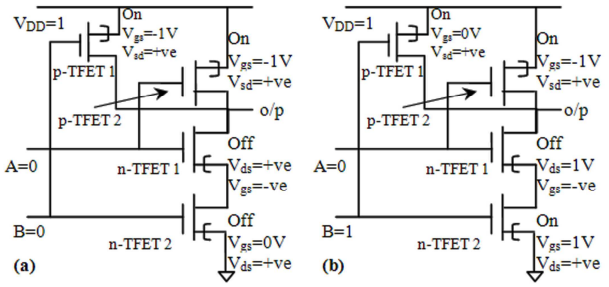

Fig. 9. (a), (b) Two input NAND gate operation for different input combination and the respective terminal voltage polarities.

In fact for A=0, B=0, a very high negative V_{gs} value appears across n-TFET 1, which leads to ambipolar current flow through it and ultimately results in increase of static leakage power dissipation and if I_{amb} is high, n-TFET 1 can start conducting.

For A=0, B=1, also a negative V_{gs} value appears across n-TFET 1 which creates an ambipolar state. If the V_{Tamb} value would be higher than the V_{gs} appearing across n-TFET 1 for input condition 1 and 2 and I_{amb} is below the level of 10 pA/µm then the circuit will work reliably and will not dissipate a high leakage power.

Thus, high V_{Tamb} value will provide a wide design window in the –ve V_{gs} range and better ambipolarity suppression, thus depending on the V_{DD} and device specifications (I_{on}, I_{amb}, I_{off}, V_{th}) it will be easy to determine which device architecture will be suitable depending on its V_{Tamb} and SS_{amb} values. To summarize the essence of this work and in order to compare all the structures together to provide a design guideline for the best architecture a quantitative comparison is made in

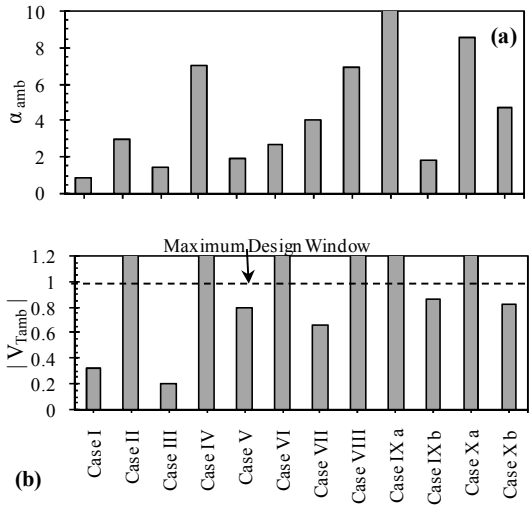

Fig. 10. Ambipolar parameters (a) α_{amb}, and (b) V_{Tamb} for various architectures. The cases for which the bar is crossing the axis limits exhibits the ideal behavior.

Table 3 and Figs. 10(a), (b). As discussed earlier in section III that $SS_{amb(0\text{-}1)}$ should be as high as possible and $SS_{amb(1\text{-}0)}$ should be as low as possible, so the factor α_{amb} should have maximum possible value in order to have a better ambipolar suppression. In addition to α_{amb}, V_{Tamb} should be as high as possible, the ideal case being, V_{Tamb} should not appear in the range of design window voltage as shown in Fig. 10(b) for case II, IV, VI, VIII, IX a and X a. From all of the structures discussed, the HG TFET with low drain doping and TFET with large GDU (=20 nm) provides the maximum design window in negative gate voltage range (Table 3) and hence they will exhibit a reliable complementary circuit operation and will not pose the problem of increased static leakage power dissipation due to increasing I_{amb}.

V. CONCLUSIONS

The study presents a comprehensive investigation of a variety of architectural modifications on the ambipolar conduction of p-i-n and p-n-p-n TFET through quantitative and qualitative analysis. The quantitative parameters defined to characterize the ambipolarity are calculated and compared for all the architectures. In addition to ambipolar conduction suppression, another important factor for circuit performance i.e. Miller capacitance (C_{gd}) is also analyzed and the trade-offs to achieve a fast and reliable logic operation are discussed. Although a large gate drain underlap, and low drain doping are effective in suppressing the ambipolarity but they exhibit a high miller capacitance and also suffers from device scalability limitation, whereas a HG structure with low drain doping completely suppresses the ambipolarity, does not faces scalability issues, and the optimization of high-k and low-k length also helps in minimizing the miller capacitance.

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