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Impact of Interface Charges on the Transient Characteristics of 4H-SiC DMOSFETs

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Abstract – In this paper, we study the transient characteristics of 4H-SiC DMOSFETs with different interface charges to improve the turn-on rising time. A physics-based two-dimensional mixed device and circuit simulator was used to understand the relationship between the switching characteristics and the physical device structures. As the SiO_2/SiC interface charge increases, the current density is reduced and the switching time is increased, which is due primarily to the lowered channel mobility. The result of the switching performance is shown as a function of the gate-to-source capacitance and the channel resistance. The results show that the switching performance of the 4H-SiC DMOSFET is sensitive to the channel resistance that is affected by the interface charge variations, which suggests that it is essential to reduce the interface charge densities in order to improve the switching speed in 4H-SiC DMOSFETs.

Keywords: 4H-SiC, DMOSFET, Mixed-mode, Transient, Interface charge

1. Introduction

Silicon carbide (SiC) is a well-known wide-bandgap (3.26 eV) semiconductor material, which is suitable for high-temperature, high-frequency, and high-power applications [1]. Due to their superior physical properties, such as high thermal conductivity, high critical field (2.2×10^6 V/cm), and high bulk electron mobility (~900 cm^2/Vs) of the 4H-SiC polytype, SiC MOSFETs can operate at junction temperatures well above 200°C with higher figures of merits than Si-based devices [2]. However, despite the major advancements in SiC process technology during the last decade, the realization of SiC MOSFETs is still hindered due largely to the low inversion channel mobility. The problem caused by the high interface state density at the metal-oxide-semiconductor (MOS) interface of SiO_2/SiC is the same as that of the early silicon devices [3, 4]. On the other hand, one of the major differences between Si and SiC is the energy barrier height between the semiconductor and dielectrics, thus the tunneling current density through the oxide is higher in SiC than that in Si for the same surface electric field [5]. Increasing the SiO_2/SiC interface charges may lead to a decreased breakdown voltage and therefore the interface charges in SiC MOSFETs can significantly affect the transient characteristics as well as the static characteristics. Although various SiC DMOSFET structures have been reported so far for optimizing performances [6], the effect of the interface states on the switching performance of SiC DMOSFETs has not been extensively examined. In this paper, we report on the effect of interface charge density (D_{it}) distributions on the transient characteristics of the SiC DMOSFET devices.

2. Resistive load switching

In order to optimize the key design parameters for SiC DMOSFETs and to understand the relationship of the switching characteristics, a physics-based two-dimensional (2-D) mixed mode device and circuit simulator by Atlas, Silvaco Inc. was used. At first, 2-D numerical simulations were performed to optimize a 4H-SiC DMOSFET for blocking up to 1200 V with minimum loss by adjusting the structure parameters [7] of DMOSFETs, such as the JFET region, the current spreading layer (CSL), the N-epi layer as well as the channel length (L_{CH}), and the gate oxide thickness, as shown in Fig. 1. To investigate transient characteristics of the devices, mixed-mode simulation was then performed, where the solution of the basic transport equations for the 2-D device structures was directly embedded into the solution procedure for the circuit equations. The circuit in Fig. 2 was used to investigate the switching characteristics of the 4H-SiC DMOSFETs under a resistive load. The circuit was designed to provide a current path from the supply voltage V_{DC}=100 V and a bus capacitor C_{DC}=1 μF to the resistive load R_{DC}=250 kΩ and 4H-SiC DMOSFETs [8, 9].

Relatively low inductance power resistors were employed for R_D, and the on-state current values were

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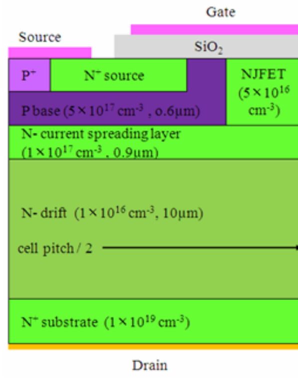

Fig. 1. Cross-sectional view of the 4H-SiC DMOSFET cell.

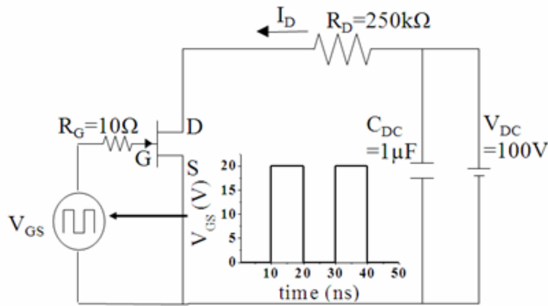

Fig. 2. Simulated resistive load switching circuit including a 4H-SiC DMOSFET.

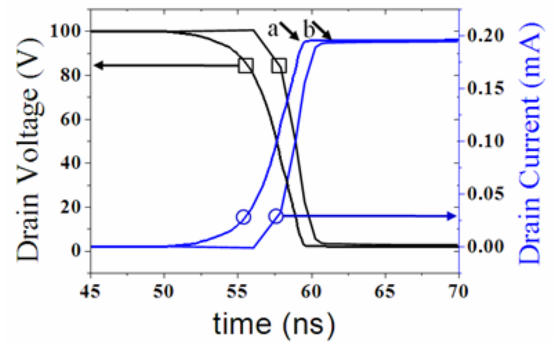

Fig. 3. Mixed-mode simulation results of the turn-on characteristics for DMOSFETs with different interface charges: (a) D_{it}=1×10^{11} C/cm^2; (b) D_{it}=1×10^{12} C/cm^2.

calculated accordingly. A resistive load circuit was used with the pulse bias applied to the gate-to-source voltage (V_{GS}) from 0 V to 20 V. The transient characteristics were obtained by the on and off switching of the device by applying the pulse bias V_{GS}.

3. Results and Discussion

3.1 The switching characteristics of 4H-SiC MOSFETs

Fig. 3 shows the resistive load turn-on waveforms including the 4H-SiC DMOSFETs drain voltage and current characteristics for different interface charge (D_{it}) conditions. The interface charges were linearly increased from 1×10^{11} C/cm^2 to 1×10^{12} C/cm^2. The switching times were calculated by the current waveforms of the turn-on rising time (t_r) when the device was turned on [10].

The results show that t_r is affected by the interface charge density. With a D_{it} of 1×10^{11} C/cm^2, a t_r of ~8 ns was extracted, while a t_r of ~11 ns was calculated at a D_{it} of 1×10^{12} C/cm^2. So, the turn-on response is slower for devices with higher interface charges.

3.2 RC delay time

The effect of interface charges on the device transient characteristics was investigated. The intrinsic parasitic components, such as capacitance and resistance, may affect the switching behavior of the device, and the gate-to-source capacitance (C_{GS}) together with the specific on-resistance ($R_{on,sp}$) dominates the switching speed [11, 12]. Therefore, the switching characteristics are related to changes in RC delay time (τ_{RC}) through C_{GS} and $R_{on,sp}$.

The RC delay time can be given by $\tau_{RC}=C_{GS}\times R_{on,sp}$, where C_{GS} is obtained from the C_{GS} versus V_{GS} characteristics with a gate bias of 10 V, and $R_{on,sp}$ is extracted from the drain current (I_D) versus drain voltage (V_D) characteristics in the Ohmic region. With a D_{it} of 1×10^{11} C/cm^2, $R_{on,sp}$ and C_{GS} are 5.5 mΩ/cm^2 and 0.306 fF/µm^2, respectively, which results in a RC delay time of 16.8 ps (see Table 1).

Table 1. RC delay time for DMOSFETs with different density of interface charges: (a) D_{it} = 1×10^{11} C/cm^2; (b) D_{it} = 5×10^{11} C/cm^2; (c) D_{it} = 1×10^{12} C/cm^2.

D_{it} (C/cm^2)	$R_{on,sp}$ (mΩ·cm^2)	C_{GS} (fF/µm^2)	τ_{RC} (ps)
1 × 10^{11}	5.5	0.306	16.8
5 × 10^{11}	5.7	0.329	18.6
1 × 10^{12}	5.8	0.345	20.0

The RC delay time of 20.0 ps can be obtained at a D_{it} of 1×10^{12} C/cm^2 because of the increase of 30% in $R_{on,sp}$ and the increase of 4% in C_{GS}. By increasing the interface charges, both the turn-on rising time and RC delay time are also increased as shown in Fig. 4. This is primarily due to the fact that the lowered channel mobility at high interface charges resulted in an increase in the $R_{on,sp}$. Since the $R_{on,sp}$ is dominated by the channel resistance, the interface charges have an effect on the intrinsic parasitic components, such as C_{GS} and $R_{on,sp}$ and thus change the switching performance.

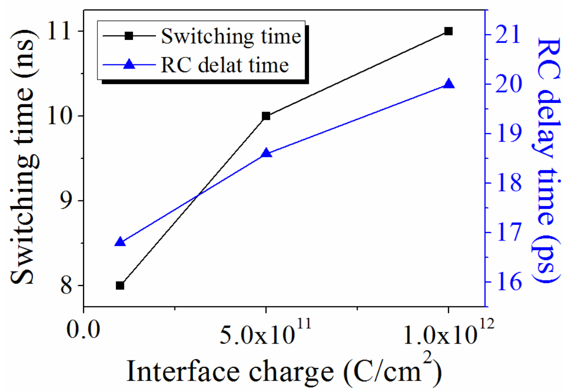

Fig. 4. Relationship between RC delay time and switching time as a function of interface charge.

3.3 Current density in the channel region

As the interface charge increases, the free-electron concentration in the inversion layer decreased and the trapped charge increased [5]. In addition, the field-effect mobility was reduced by the presence of interface-trapped charges, since the trapped charges act as scattering sites that reduce the mobility and current density as shown in Fig. 5. The lowered current density with high interface charges can result in increased carrier trapping, recombination centers, or scattering sites at an interface of the SiO_2/SiC.

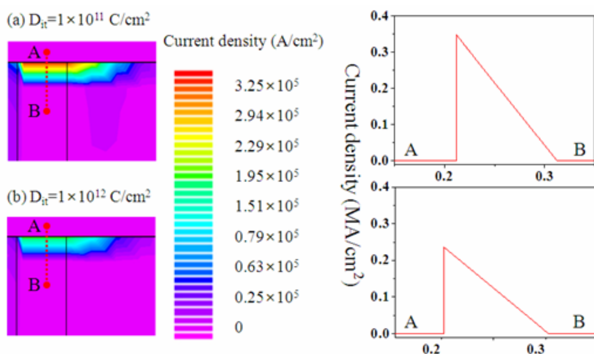

Fig. 5. Comparison of current density distribution profiles in the channel region: (a) D_{it}=1×10^{11} C/cm^2; (b) D_{it}=1×10^{12} C/cm^2.

4. Conclusion

This paper presents the transient characteristics of 4H-SiC DMOSFETs at different interface charges. Numerical simulations for both the static and switching characteristics were performed to analyze the effect on the device switching performances. As the interface charges linearly increased, the turn-on response of the device became slower and the intrinsic parasitic components increased. The device exhibited turn-on rise times of 8 ns and 11 ns for different D_{it} values of 1×10^{11} C/cm^2 and 1×10^{12} C/cm^2, respectively.

Additionally, the current density was reduced due to the presence of interface-trapped charges. It was found that the switching characteristics are related to changes in the RC delay time through the gate-to-source capacitance and the specific on-resistance. The switching performance of the 4H-SiC DMOSFET was very sensitive to channel resistance variation induced by different interface charges. In order to further improve the switching speed in 4H-SiC DMOSFETs, it is essential to reduce interface charges, which may act as carrier trapping, recombination centers, or scattering sites.

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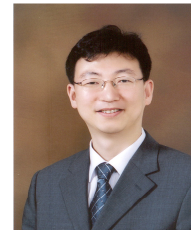

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