



A 1.8 V 40-MS/sec 10-bit 0.18- μ m CMOS Pipelined ADC using a Bootstrapped Switch with Constant Resistance

Ji-Hun Eo, Sang-Hun Kim, Mungyu Kim, and Young-Chan Jang*, *Member, KIICE*

Department of Electronic Engineering, Kumoh National Institute of Technology, Gumi 730-701, Korea

Abstract

A 40-MS/sec 10-bit pipelined analog to digital converter (ADC) with a 1.2 V_{pp} differential input signal is proposed. The implemented pipelined ADC consists of eight stages of 1.5 bit/stage, one stage of 2 bit/stage, a digital error correction block, band-gap reference circuit & reference driver, and clock generator. The 1.5 bit/stage consists of a sub-ADC, digital to analog (DAC), and gain stage, and the 2.0 bit/stage consists of only a 2-bit sub-ADC. A bootstrapped switch with a constant resistance is proposed to improve the linearity of the input switch. It reduces the maximum V_{GS} variation of the conventional bootstrapped switch by 67%. The proposed bootstrapped switch is used in the first 1.5 bit/stage instead of a sample-and-hold amplifier (SHA). This results in the reduction of the hardware and power consumption. It also increases the input bandwidth and dynamic performance. A reference voltage for the ADC is driven by using an on-chip reference driver without an external reference. A digital error correction with a redundancy is also used to compensate for analog noise such as an input offset voltage of a comparator and a gain error of a gain stage. The proposed pipelined ADC is implemented by using a 0.18- μ m 1-poly 5-metal CMOS process with a 1.8 V supply. The total area including a power decoupling capacitor and the power consumption are 0.95 mm² and 51.5 mW, respectively. The signal-to-noise and distortion ratio (SNDR) is 56.15 dB at the Nyquist frequency, resulting in an effective number of bits (ENOB) of 9.03 bits.

Index Terms: Pipelined, Analog to digital converter, Bootstrapped switch

I. INTRODUCTION

Over the past few decades, the designs for many pipelined analog-to-digital converters (ADCs) have been published for use in communication systems and image signal processing systems [1-3]. Recently, low power consumption and small area have become two of the most significant requirements for mobile systems. The pipelined ADCs in the literature [3] and [4] have reduced the power consumption and chip area by eliminating a sample-and-hold amplifier (SHA). To implement the pipelined ADC without an SHA, the design of the input sampling circuit is important to enhance the dynamic performance of an entire

ADC. Specifically, the switching clock between the multiplying digital-to-analog converter (MDAC) and the ADC in the first stage should be synchronized to produce an accurate sample of the input analog signal. Thus, an identical bootstrapped switch was used for the clock phases of both the MDAC and ADC [3].

In this work, a 1.8 V 40-MS/sec 10-bit pipelined ADC without an SHA is proposed to reduce hardware and power consumption. It uses a bootstrapped switch with a constant resistance to improve the linearity of the input sampling circuit [5]. Furthermore, it includes the on-chip reference driver, which generates the bias voltage of the entire analog block including the reference voltage for an ADC of each

Received 02 February 2012, Revised 17 February 2012, Accepted 27 February 2012

*Corresponding Author E-mail: ycjang@kumoh.ac.kr

Open Access <http://dx.doi.org/10.6109/jicce.2012.10.1.085>

print ISSN:2234-8255 online ISSN:2234-8883

© This is an Open Access article distributed under the terms of the Creative Commons Attribution Non-Commercial License (<http://creativecommons.org/licenses/by-nc/3.0/>) which permits unrestricted non-commercial use, distribution, and reproduction in any medium, provided the original work is properly cited.

Copyright © The Korea Institute of Information and Communication Engineering

stage. Section II describes the architecture and circuits of the proposed pipelined ADC. Section III examines its implementation and performance. In section IV, concluding remarks are presented.

II. PIPELINED ADC

A. Architecture

The proposed pipelined ADC consists of the analog block of nine stages and the digital block, which corrects the error noise generated in the analog block, as shown in Fig. 1. Each stage consists of an ADC, a DAC, and an amplifier with the voltage gain of two. However, the last stage includes only a 2-bit ADC.

Each stage resolves two bits with an ADC, subtracts this value from its input, and amplifies the resulting residue by a gain of two while it samples and holds the output of the previous stage. The stages are buffered by switched-capacitor gain blocks that provide a sample-and-hold between each stage, allowing concurrent processing. Each stage outputs the 2-bit digital code, and the 18-bit digital code from nine stages is supplied to the digital correction block. Then, the 10-bit binary digital code is finally generated by the digital correction block. Because the 18-bit digital code is sequentially generated for the sampled input analog signal, the digital correction block has a register composed of a D flip-flop to store the digital code supplied from each stage.

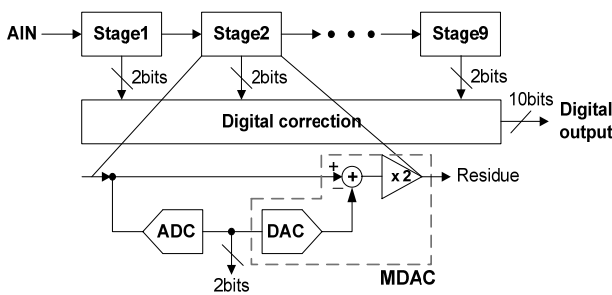


Fig. 1. Architecture of pipelined analog to digital converter (ADC) without sample-hold amplifier (SHA). DAC: digital to analog, MDAC: multiplying digital-to-analog converter, AIN: analog input.

The analog block composed of nine stages generates the 18-bit digital code including the redundancy bits to correct for analog noise errors such as the offset voltage of a comparator and operational amplifier and the variation in the reference voltage. Thus, the pipelined ADC can increase the accuracy by compensating for the analog noise through digital error correction. This architecture with digital correction relaxes the constraints on the comparator offset

voltage and direct current (DC) operational amplifier gain. Even if each stage generates the 2-bit digital code, this code effectively has the information of 1.5 bits. Actually each stage except the last one has three comparators for an ADC that has thresholds at $+V_{REF}/4$ and $-V_{REF}/4$ [1]. The input signal ranges from $-V_{REF}$ to $+V_{REF}$ (differential). The designed pipelined ADC has a differential input range of 1.2 Vpp with a 1.8 V supply. The voltage levels of $-V_{REF}$ and $+V_{REF}$ are 0.6 V and 1.2 V, respectively.

The proposed pipelined ADC uses the first 1.5 bit/stage including a bootstrapped switch with a constant resistance instead of a SHA. It results in the reduction of the hardware and power consumption. It also increases the input bandwidth and dynamic performance.

B. Input Sampling Circuit of First Stage

A SHA samples and holds the consistently transitional analog signal by using two periods of sample and hold. This results in the improvement of the dynamic performance in an ADC. Usually, an SHA consists of a holding capacitor, a sample switch, and an operational amplifier. Thus, this increases the power consumption and chip area, and limits the input bandwidth.

In this work, an SHA is removed to have the wide input bandwidth over the Nyquist frequency and to reduce the power consumption and chip area. Fig. 2 shows the input sampling circuit of the first stage.

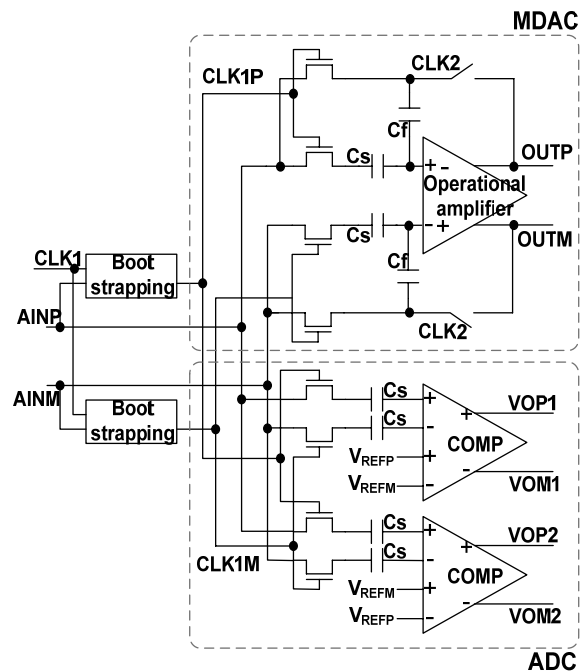


Fig. 2. Input sampling circuit of first stage. MDAC: multiplying digital-to-analog converter, ADC: analog to digital converter, AIN: analog input, CLK: clock, C: capacitor, V: voltage.

The input sampling circuit of the proposed pipelined ADC is implemented by synchronizing the clock phase between an ADC and an MDAC instead of using an SHA. While an MDAC and an ADC sample the analog input signal, the resistive and capacitive time constant of each path, which is determined by the product of the turn-on resistance of each analog switch and the load capacitance, should be maintained as constant. Thus, the identical bootstrapped switch is used for the clock phases of both the MDAC and ADC only in the first stage. This improves the dynamic performance by having a constant resistance even if the analog voltage level changes. Furthermore, the sampling capacitors (CS) of the MDAC and ADC have an identical value and are implemented by using a metal-insulator-metal (MIM) capacitor.

C. Bootstrapped Switch with Constant Resistance

In most highly accurate ADCs, a bootstrapped analog switch is used for sampling in sample-and-hold circuits. It provides constant on-resistance by maintaining the gate-source voltage (V_{GS}) of the sampling switches independent of the input signals. This results in the improvement of the precision and linearity of the sample-and-hold circuits. Fig. 3 shows the circuit diagram of the conventional bootstrapped switch using the capacitor (C_B) [1].

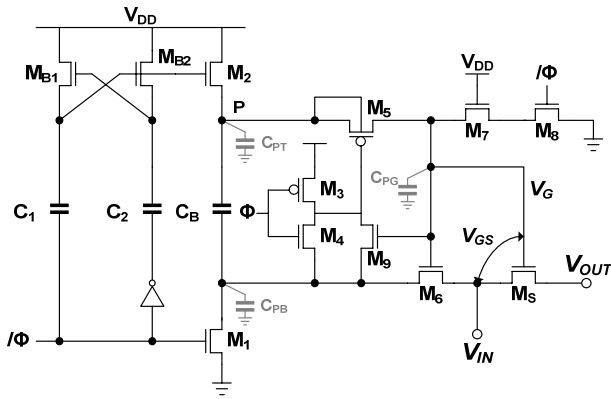


Fig. 3. Conventional bootstrapped switch for analog to digital converter (ADC) input stage.

M_5 operates as the sampling switch, turning on during phase Φ and off during $/\Phi$. When Φ is low, V_{DD} is applied across C_B by turning M_1 and M_2 on. M_6 and M_5 simultaneously turn off as the node voltage V_G is switched to ground. When Φ is high, the bottom plate of C_B is connected to V_{IN} , and the top plate of C_B and the V_G node are shifted to the voltage level of $V_{DD} + V_{IN}$ as M_5 and M_6 turn on. Thus the V_{GS} of M_5 is ideally determined by V_{DD} ,

which is independent of V_{IN} . However, this approach may lead to variations in V_{GS} due to the change of V_{IN} when the parasitic capacitors (C_{PT} , C_{PB} , and C_{PG}) shown in Fig. 1 cannot be ignored. Actually, C_{PG} may have a relatively large capacitance value due to the gate of the analog switch and route path while the capacitance values of C_{PT} and C_{PB} are small. The voltage levels of V_G and V_{GS} are determined by the charge sharing between C_B and C_{PG} , as shown in Eq. (1) and (2). Thus the maximum variation of V_{GS} when V_{IN} changes from ground to V_{DD} is expressed as Eq. (3).

$$V_G = \frac{C_B}{C_B + C_{PG}} (V_{DD} + V_{in}) \quad (1)$$

$$V_{GS} = V_G - V_S = \frac{C_B}{C_B + C_{PG}} V_{DD} - \frac{C_{PG}}{C_B + C_{PG}} V_{in} \quad (2)$$

$$\Delta V_{GS_MAX} = V_{GS(V_{in}=0V)} - V_{GS(V_{in}=V_{DD})} = \frac{C_{PG}}{C_B + C_{PG}} V_{DD} \quad (3)$$

As a result, the node voltage V_G is not determined by $V_{DD} + V_{IN}$, and the V_{GS} of M_5 is dependent on the input signal due to C_{PG} .

In the pipelined ADCs, the input-sampling switch (M_S) usually uses a large transistor to reduce the on-resistance of the input switch. This results in the increase of the capacitive load (C_{PG}) at the V_G node of the input-sampling switch. Thus, the value of V_{GS} has the variation of several tens of mV even if a bootstrapped switch is used.

A bootstrapped switch is used only for the differential analog input signal. Also, the pipelined ADC uses a multi-input-sampling switch instead of one separate sample-and-hold circuit, as shown in Fig. 2. When the gate voltage of a bootstrapped switch is shared as part of the multi-input-sampling switch, the capacitive load of the gate node of the bootstrapped switch increases.

Thus a gate node of a sampling transistor is not constantly boosted by amount of V_{DD} from the analog input signal, V_{IN} . Furthermore, the input-sampling switch (M_S) usually uses a large sized transistor to reduce the on-resistance of the input switch. This results in the increase of the capacitive load (C_{PG}) at the V_G node of the input-sampling switch. Thus, the value of V_{GS} has the variation of several tens of mV even if a bootstrapped switch is used.

The bootstrapped switch with a constant on-resistance is proposed in this work. To implement this bootstrapped switch, the initialization circuit of the bootstrapped switch is added into the conventional bootstrapped switch, as shown in Fig. 4. The added initialization circuit is composed of a transmission gate and a short pulse generator.

The transmission gate is inserted between the V_G and V_{IN} nodes of Fig. 4 and is controlled by the short pulse generator. Also, the Φ' signal generated in the short pulse generator is supplied for the gate node of M_3 and M_4 in Fig. 4. When Φ goes high (Φ goes low), the voltage of the P node changes from V_{DD} to $V_{DD}+V_{IN}$. Simultaneously, the V_G node is charged from ground to V_{IN} by the inserted transmission gate during a short period (t_{charge}). At this time, the P and V_G nodes are separated by turning M_5 off because the gate signal of M_3 and M_4 is delayed from the Φ signal. After the V_G node is charged to the voltage level of V_{IN} , the charge sharing between the P and V_G nodes is achieved as M_5 is turned on. The effect of C_{PG} is minimized by the above mentioned process. Thus the variation of V_{GS} (ΔV_{GS}) is reduced as the voltage level of V_{IN} changes. The short pulse generator supplies the control signals for the transmission gate (cont_n, cont_p) and the gate of M_3 and M_4 (Φ').

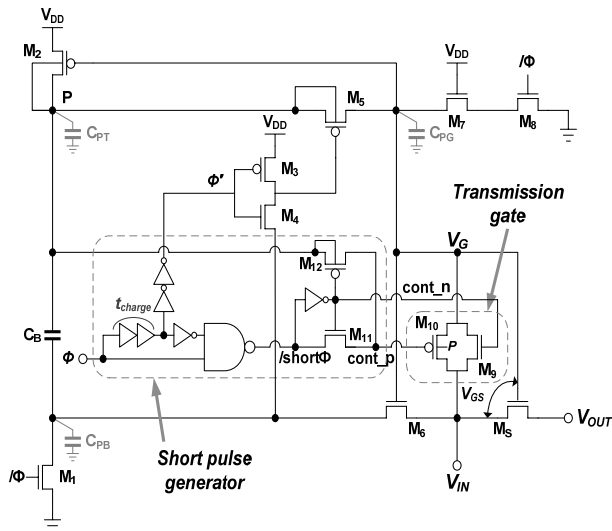


Fig. 4. Bootstrapped switch with constant resistance.

When Φ goes high, the cont_n and cont_p signals have the voltages of V_{DD} and ground, respectively, to turn the transmission gate on during the short period of t_{charge} , which is the time in which the V_G node reaches the voltage level of V_{IN} . Except the initial charging period for the V_G node, the cont_p signal follows the voltage of the P node to turn the PMOS transistor of the transmission gate off. Also, it is required to connect the bulk node of M_{10} to the P node because the voltage level of the V_G node can be changed from ground to $V_{DD}+V_{IN}$. Fig. 5 shows the timing diagram of the bootstrapped switch shown in Fig. 4.

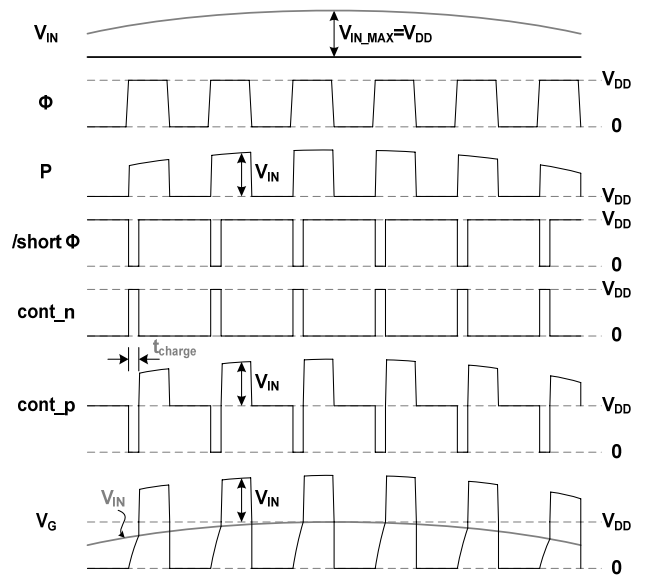


Fig. 5. Timing diagram of bootstrapped switch with constant resistance.

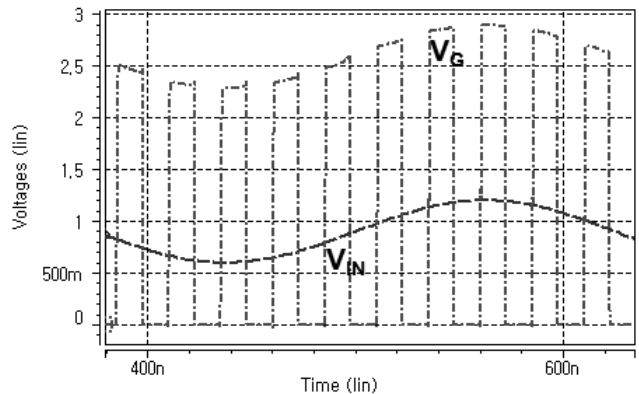
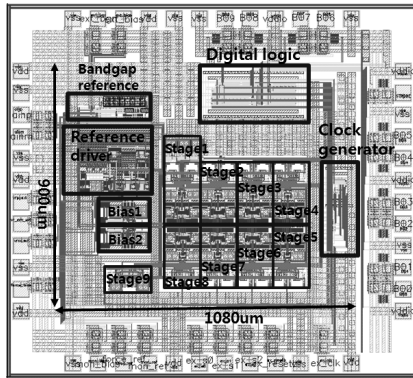


Fig. 6. Simulation result of bootstrapped switch with constant resistance.

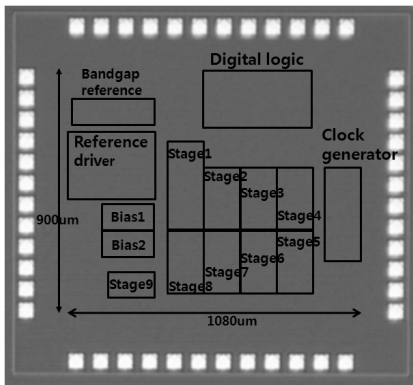
Fig. 6 shows the simulation results of the bootstrapped switch. The frequency of the input signal (V_{IN}) and clock (Φ) are 4 MHz and 40 MHz, respectively. The V_G node can confirm $V_{DD}+V_{IN}$ with a 1.8 V supply.

III. CHIP IMPLEMENTATION AND RESULT

The proposed 40-MS/sec 10-bit pipelined ADC was implemented by using a 0.18-um 1-poly 5-metal CMOS process with a 1.8 V supply. Fig. 7a and 7b show the layout of the designed pipelined ADC and the microphotograph of the implemented pipelined ADC.



(a)



(b)

Fig. 7. (a) Layout (b) Microphotograph.

The chip area, including the power decoupling capacitor, and power consumption were 0.95 mm^2 and 51.5 mW with a supply voltage of 1.8 V , respectively. Fig. 8 shows the fast fourier transform (FFT) result of the pipelined ADC. The SNDR of the pipelined ADC was 56.15 dB at the Nyquist frequency, resulting in an ENOB of 9.03 bits. Table 1 is performance summary of the proposed pipelined ADC.

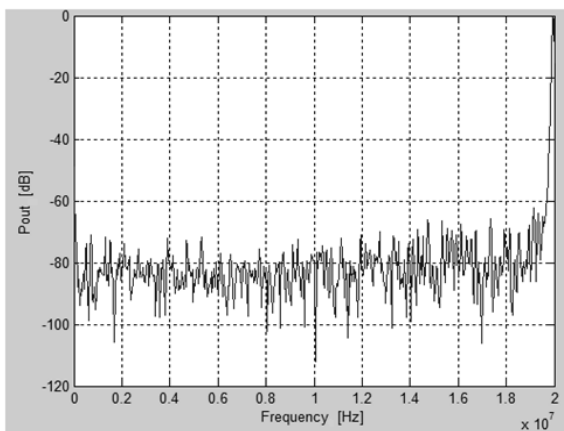


Fig. 8. Fast fourier transform result of pipelined analog to digital converter.

Table 1. Performance summary of designed pipelined analog to digital converter

Resolution	10-bit
Conversion rate	40-MS/sec
Process & supply	0.18- μm @1.8 V
Input range	1.2 Vpp
Signal-to-noise and distortion ratio	56.15 dB
Chip size	0.95 mm^2
Power consumption	51.5 mW

IV. CONCLUSIONS

A 40-MS/sec 10-bit pipelined ADC with 1.2 Vpp input range was implemented by using a $0.18\text{-}\mu\text{m}$ CMOS process with a 1.8 V supply. The implemented pipelined ADC consisted of an ADC, DAC, gain stage, and digital block. The proposed pipelined ADC increased the linearity by using the bootstrapped switch. The pipelined ADC using an on-chip reference driver instead of an external reference voltage was designed. The pipelined ADC has the SNDR of 56.15 dB and ENOB of 9.03 bits at the Nyquist frequency. The chip area including the power decoupling capacitor and power consumption are 0.95 mm^2 and 51.5 mW , respectively.

ACKNOWLEDGMENTS

This research was supported by the Research Fund, Kumoh National Institute of Technology.

REFERENCES

- [1] A. M. Abo and P. R. Gray, "A 1.5V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 599-606, 1999.
- [2] S. C. Lee, K. D. Kim, J. K. Kwon, J. Kim, and S. H. Lee, "A 10-bit 400-MS/s 160-mW 0.13- μm CMOS dual-channel pipeline ADC without channel mismatch calibration," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 7, pp. 1596-1605, 2006.
- [3] H. C. Choi, Y. J. Kim, M. H. Lee, Y. L. Kim, and S. H. Lee, "A 12b 50 MS/s 10.2 mA 0.18 μm CMOS Nyquist ADC with a fully differential class-AB switched OP-AMP," *Proceedings of the IEEE Symposium on VLSI Circuits*, Honolulu: Hawaii, pp. 220-221, 2008.
- [4] P. Huang, S. Hsien, V. Lu, P. Wan, S. C. Lee, W. Liu, B. W. Chen, Y. P. Lee, W. T. Chen, T. Y. Yang, G. K. Ma, and Y. Chiu, "SHA-less pipelined ADC converting 10th Nyquist band with in-situ clock-skew calibration," *Proceeding of the IEEE Custom Integrated Circuits Conference*, San Jose: CA, pp. 1-4, 2010.

- [5] S. H. Kim, Y. H. Lee, H. J. Chung, and Y. C. Jang, "A bootstrapped analog switch with constant on-resistance," *IEICE Transaction on Electronics*, vol. E94C, no. 6, pp. 1069-1071, 2011.



Ji-Hun Eo

was born in Gumi, Korea, in 1984. He received the B.S. and M.S. degree in electronic engineering from Kumoh National Institute of Technology, Gumi, Korea, in 2010 and 2012, respectively. His research interest includes the mixed-mode circuit design such as analog-to-digital conversion.



Sang-Hun Kim

was born in Gumi, Korea, in 1985. He received the B.S. and M.S. degree in electronic engineering from Kumoh National Institute of Technology, Gumi, Korea, in 2010 and 2012, respectively. Since 2012, he has been an analog IC designer at Magnachip, Cheongju, Korea. His research interest includes the high speed analog circuit design such as the analog-to-digital conversion of flash type.



Mungyu Kim

was born in Gumi, Korea, in 1985 and received the B.S. degree in electronic engineering from Kumoh National Institute of Technology, Gumi, Korea, in 2011. He is currently earning the M.S. degree in electronic engineering from Kumoh National Institute of Technology, Gumi, Korea. His research interest includes the analog integrated circuit design such as digital-to-analog conversion and temperature sensor.



Young-Chan Jang

was born in Daegu, Korea, in 1976. He received the B.S degree in electronic engineering from Kyungpook National University, Daegu, Korea, in 1999 and the M.S and Ph.D. degrees in electronic engineering from Pohang University of Science and Technology (POSTECH), Pohang, Korea, in 2001 and 2005, respectively. From 2005 to 2009, he was with the Memory Division, Samsung Electronics, Hwasung, Korea, working on high-speed interface circuit design and next-generation DRAM. Since 2009, he has been an Assistant Professor at Kumoh National Institute of Technology, Gumi, Gyungbuk, Korea. His current research area is high-performance mixed-mode circuit design for VLSI systems such as high-performance signaling, clock generation, and data conversion.