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직렬 및 병렬연결 멤리스터 회로의 전기적 특성 해석

(Analysis of Electrical Features of Serially and Parallelly connected Memristor Circuits)

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요 약

저항, 콘덴서, 및 인턱터와 함께 4의 회로 소자로 알려진 멤리스터가 개발되었으나, 아직 그 전기적 특성이 충분히 해석되지 않고 있다. 멤리스터들은 연결된 극성에 따라서 저항이 증가 혹은 감소하며, 직렬 혹은 병렬연결 형태에 따라서 그 동작 특성이 다양해진다. 본 연구에서는 HP의 TiO_2 멤리스터를 모델로 하여 다양한 직 병렬회로에 대한 전기적 특성을 분석하였다. 이를 위해서 사인파 입력신호에 대해서 나타나는 전압-전류 간의 히스테르시스 루프의 다양한 모양을 분석하였다. 본 멤리스터 연구결과는 멤리스터 소자에 대한 특성 이해와 논리 회로 및 뉴런 셀에의 응용회로들의 특성을 분석하는데 유용하게 사용될 수 있다.

Abstract

Memristor which is known as fourth basic circuit element has been developed recently but its electrical characteristics are not still fully understood. Memristor has the incremental and decremental feature of the resistance depending upon the connected polarities. Also, its operational behavior become diverse depending on its connection topologies. In this work, electrical characteristics of diverse types of serial and parallel connections are investigated using the HP TiO_2 model. The characteristics are analyzed with pinched hystersis loops on the V-I plane when sine input signal is applied. The results of the work would be utilized usefully for analyzing the characteristics of memristor element and applications to logic circuit and neuron cells.

Keywords : Memristor, series and parallel connections, incremental and decremental, pinched hysteresis loop.
멤리스터, 직병렬회로, 정방향 및 역방향의 극성, 핀치 히스테르시스 루프

Ⅰ. Introduction

A new ideal circuit element memristor relates the charge q and the magnetic flux ϕ in a circuit. It complements a resistor R, a capacitor C and an inductor L as the basic element of ideal electrical circuits.

The memristor was postulated as the fourth basic element of electrical circuits by Leon O. Chua in 1971 [1]. It is based on a non linear relationship between charge and flux. Chua and Kang extend the idea to memristive systems and devices in 1978[2].

After such an important discovery, however, there were no research work until HP discovered the memristor as a nano-component made of titanium dioxide in 2008[3]. It consists of a two layer thin film (size $D \sim 10nm$) of TiO_2, sandwiched between

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platinum contacts. One of the layers is doped with oxygen vacancies thus behaving as a semiconductor. Another layer which is undoped has an insulating property. The width w of the doped region is modulated depending on the amount of charge passing through the memristor. When current or voltage passes in a given direction, the boundary between the two regions moves in the same direction. The total memristance is a sum of the resistances of the doped and undoped regions. It exhibited pinched hysteresis loop in the current voltage plot.

Joglekar et. al. presented the memristor properties along with the ideal memristor-capacitor, memristor inductor and memristor-capacitor-inductor circuits in 2009[4]. They clarified the behaviour of two memristors in series. They labeled the polarity of a memristor by $\eta = \pm 1$, where $\eta = +1$ signifies that $w(t)$ increases with positive voltage or, in other words, the doped region in memristor is expanding. If the doped region, $w(t)$, is shrinking with positive voltage, then $\eta = -1$. In other words, reversing the voltage source terminals implies memristor polarity switching.

O. Kavehei et. al. reviews the memristor characteristics and provides mathematical and SPICE models for memristors in 2010[5]. They focused on device level property of memristors.

In this paper, the properties of a single memristor along with memristors in series and parallel connections with same and opposite polarity are presented. A current voltage characteristics for all the cases of memristor and the variations of overall memristance are analyzed at different frequencies.

In Section II, the basic principle and the mathematical model of the titanium dioxide memristor is introduced. The linear drift model of the TiO_2 transistor has been used for the simulation. In Section III, various connections of memristors including the series and parallel are discussed. It is followed by the Simulation results and conclusions in Sections IV and V respectively.

Ⅱ. Memristor as a circuit element and its model

The memristor theory stems from the electromagnetic behavior of material. The current and voltage relationship in memristor can be defined as,

$$v(t) = R(t)i(t) = \frac{d\phi}{dq}i(t) \tag{1}$$

Where $\phi(t)$ and $q(t)$ denote the flux and charge respectively, at time t.

It consists of a thin film with one layer of insulating TiO_2 and oxygen-poor TiO_{2-x} each, sandwiched between platinum contacts. The resistance of a doped TiO_2 region is significantly lower than the resistance of the undoped region. The boundary between the doped and undoped regions, and therefore the effective resistance of the thin film, depends on the position of these dopands. It, is in turn, is determined by their mobility μ_D and the electric field across the doped region. Fig. 1. shows a schematic of a memristor of size D modeled as two resistors in series, the doped region with size w and the undoped region with size $(D-w)$. The effective resistance of such a device is

$$M(w) = \frac{w}{D}R_{ON} + \left(1 - \frac{w}{D}\right)R_{OFF} \tag{2}$$

where, R_{ON} is the resistance of the memristor if it is completely doped and R_{OFF} is its resistance if it is undoped.

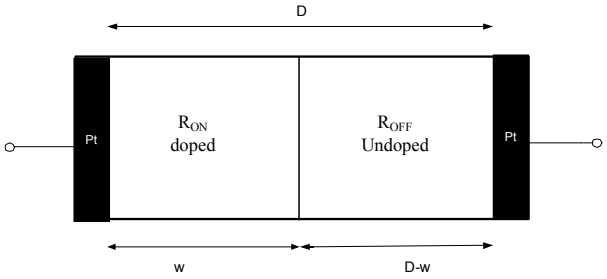


그림 1. 길이 D 인 TiO_2 멤리스터의 구조
Fig. 1. Configuration of TiO_2 Memristor with length D.

Using linear-drift model the boundary between the doped and undoped regions drifts at a constant speed given by,

$$\frac{dw}{dt} = v_D = \eta \frac{\mu_D R_{ON}}{D} i(t) \tag{3}$$

η is the parameter that characterizes the polarity of a memristor such that $\eta = \pm 1$, where $\eta = +1$ corresponds to the expansion of the doped region.

Integrating equation (2),

$$w(t) = w_0 + \eta \frac{\mu_D R_{ON}}{D} q(t)$$

$$\text{or, } w(t) = w_0 + \eta \frac{D q(t)}{Q_0} \tag{4}$$

where, w_0 is the initial size of the doped region and $Q_0 = D^2 / \mu_D R_{ON}$ is the charge required to pass through the memristor for the dopant boundary to move through distance D. Substituting equation (4) in equation (2), we get,

$$M(q) = R_0 - \eta \frac{\triangle R q}{Q_0} \tag{5}$$

where, $R_0 = R_{ON}(w_0 / D) + R_{OFF}(1 - w_0 / D)$ is the effective resistance at time $t = 0$.

Now voltage across the memristor is given by,

$$v(t) = iM(q) = \frac{dq}{dt}(R_0 - \eta \frac{\triangle R q(t)}{Q_0})$$

$$\text{or, } v(t) = \frac{d}{dt}(R_0 q - \eta \frac{\triangle R q^2}{2 Q_0}) \tag{6}$$

Solving equation (6),

$$q(t) = \frac{Q_0 R_0}{\triangle R}\left[1 - \sqrt{1 - \eta \frac{2 \triangle R}{Q_0 R_0^2} \phi(t)}\right] \tag{7}$$

Similarly,

$$i(t) = \frac{v(t)}{R_0} \frac{1}{\sqrt{1 - \eta \frac{2 \triangle R}{Q_0 R_0^2} \phi(t)}}$$

$$\text{or, } i(t) = \frac{v(t)}{M(q(t))} \tag{8}$$

where, $\phi(t) = \int_0^t v(t) dt$ is the magnetic flux associated with the voltage $v(t)$.

Ⅲ. Memristors in different connections

Like other passive circuits elements (R, L and C), Memristors can be connected in series and parallel, however the resulting equivalent memristance is different than that of the other circuit elements.

3.1 A single memristor

When a sinusoidal signal is applied to a decrement type of memristor as shown in Fig. 2(a), then the memristance is varying from a large value to a small value resistance. The range of the resistance values depends on the value of R_{ON} and R_{OFF}.

Similarly an incremental memristor when supplied with the sinusoidal voltage as shown in Fig. 2(b), such that the memristance is varying from a small value to a large value resistance for positive of sinusoidal voltage signal and vice versa.

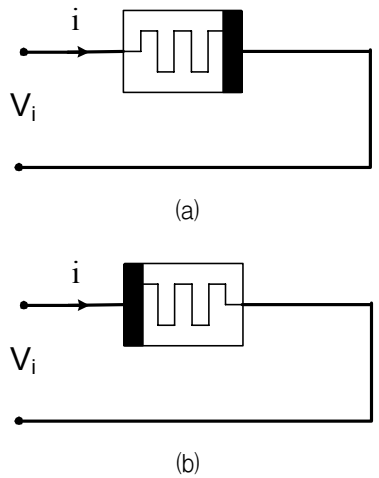


그림 2. 단일 멤리스터
(a) 저항 감소형 극성 (b) 저항 증가형 극성
Fig. 2. A single memristor (a) Decrement type memristor, (b) Incremental type of memristor.

3.2 Memristors in Series

When a voltage is applied at two serially connected decrement type memristors as shown in

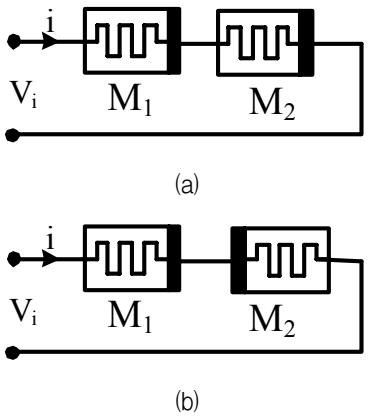


그림 3. 직렬 연결된 멤리스터 M_1 및 M_2
(a) 동일 극성인 경우 (b)역방향 극성인 경우
Fig. 3. Memristors M_1 and M_2 in series connections
(a) M_1 and M_2both are decrement type (b) M_1 is decrement type and M_2 is increment type.

Fig. 3(a), the input voltage is distributed to every memristor according to the voltage law so that the sum of each memristor voltage is equal to the input voltage like in ordinary resistors. In this case, the memristive effect is retained because the doped regions in both memristors shrink or expand simultaneously.

If the two memristors such that one is decrement type (M_1) and another is incremental (M_2) are connected in series as shown in Fig. 3(b), the memristance of M_1 decreases as the voltage increase whereas memristance M_2 increases while increasing the voltage. So the overall memristance will be suppressed that leads to the linear behavior like that of a resistance.

3.3 Memristors in parallel

In the case of parallel connection of two decrement type memristors as shown in Fig. 4(a), the same input voltage V_i must be applied at both input terminals of the parallel devices. Here, the voltage across both the memristors M_1 and M_2 are same so does the current.

Similarly if two memristors such that one is decremental (M_1) and other is incremental (M_2) are connected in parallel as shown in Fig. 4(b), though the voltage across both memristors M_1 and M_2 is

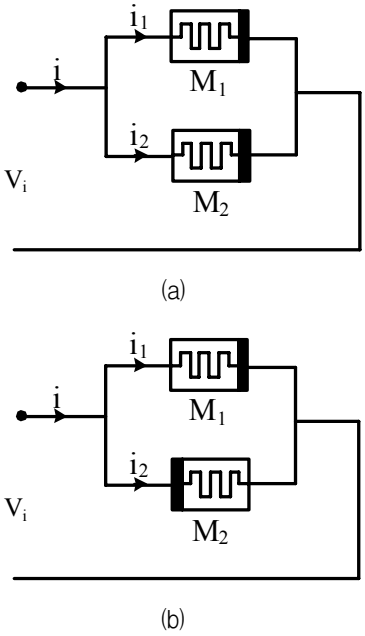


그림 4. 병렬연결된 멤리스터 M_1 및 M_2
(a) 동일 극성 연결회로,
(b) 역방향 극성 연결회로
Fig. 4. Memristors M_1 and M_2 in parallel connections.
(a) M_1 and M_2 both are decremental (b) M_1 is decremental and M_2 is incremental type.

same, the value of the current in each memristor is different. As the value of the resistance is different for M_1 and M_2 i.e. as the memristance M_1 decreases, the value of the memristance M_2 increases with increase in the supply voltage.

Ⅳ. Simulation Result

The simulations were perfomed assuming the data given by HP. The specifications for the simulation are $v(t) = V_m \sin\omega t$, $V_m = 1$, $R_{OFF} = 16K\Omega$, $R_{ON} = 100\Omega$, $D = 10nm$; $\mu_D = 10^{-14}$, $\omega_0 = 0.1 * D$ (decrement type) and $\omega_0 = 0.9 * D$ (Incremental). For a single memristor, the voltage and memristance characteristics w.r.t to time is shown in Fig. 5. The i-v characteristics of decrement type memristor for the sinusoidal input voltage are shown in Fig. 6(a). As the value of w increases, the pinched hysteresis loop becomes narrow and at high frequencies it becomes a straight line.

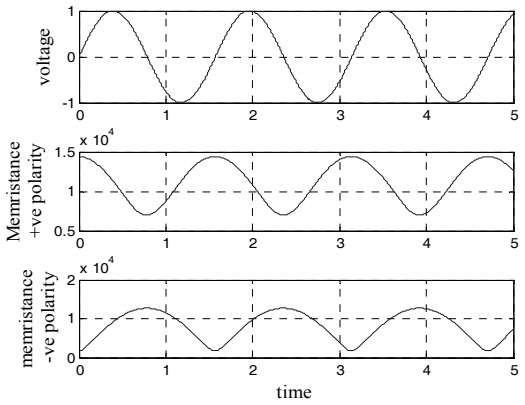
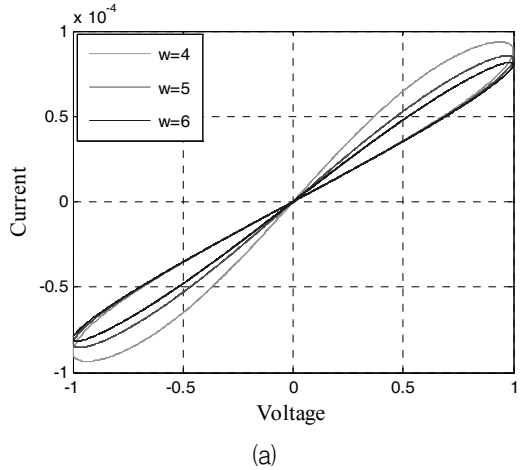
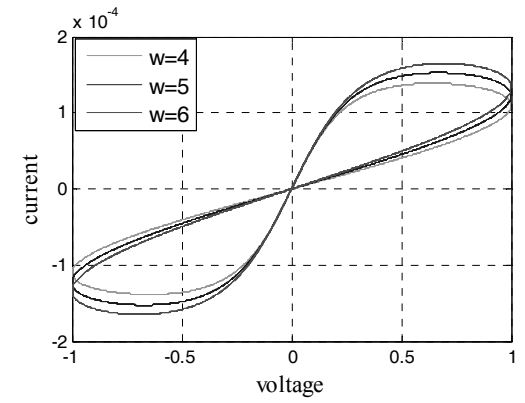


그림 5. 단일 멤리스터에 대해서, 동일 극성을 갖는 경우와 역방향 극성을 갖는 경우의 싸인 입력전압에 대한 멤리트턴스의 변화

Fig. 5. Voltage, memristance 1 (decrement type), memristance 2 (Incremental) vs. time for single memristor.



(a)



(b)

그림 6. 단일 멤리스터에 대해서, W 값 변화에 따른 전류-전압 관계 곡선 변화

Fig. 6. Current vs. voltage graph with different w for single memristor (a) decrement type (b) Incremental.

When an incremental memristor is supplied with the sinusoidal voltage, then the memristance w. r. t to time is shown in Fig. 5 at w=4 where the effective resistance is changing. Similarly, the current vs. voltage is plotted as shown in Fig. 6 (b), where a pinched hysteresis loop is obtained.

When an incremental memristor is supplied with the sinusoidal voltage, then the memristance w.r.t to time is shown in Fig. 5 at w=4 where the effective resistance is changing. Similarly, the current vs. voltage is plotted as shown in Fig. 6 (b), where a pinched hysteresis loop is obtained. The hysteresis loop is more flat at the same frequency than that of the decremental memristor. Although the loop shrinks as the frequency increases, increasing the frequency (from w = 4 to 6) has less effect on the slope of hysteresis loop compared to that of decrement type memristor with $\eta = 1$.

When two decrement type memristors M_1 and M_2, are connected in series as shown in Fig. 3(a), and supplied with the sinusoidal voltage then the voltage is divided between M_1 and M_2 and the doped region in both the memristors shrink and expand simultaneously. So the memristance of both memristors varies simultaneously. The memristance of M_1 and M_2 decreases with increase in the supply

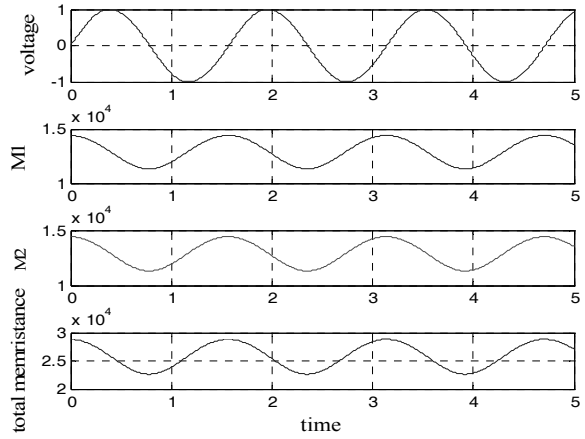


그림 7. 두 개의 멤리스터 (M_1 및 M_2)가 직렬연결된 회로에 sin 전압 파를 인가한 경우의 멤리스턴스

Fig. 7. Voltage, memristance M_1, M_2 and total memrsitance vs. time for two decrement type memristors in series at w=4.

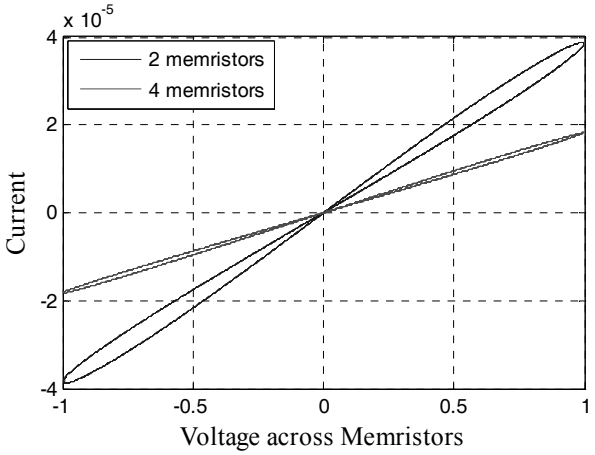


그림 8. 저항 감소방향으로 멤리스터 2 개 혹은 4개를 직렬로 연결할 때의 전류-전압그래프

Fig. 8. Current vs. voltage graph for 2 and 4 decrement type memristors in series.

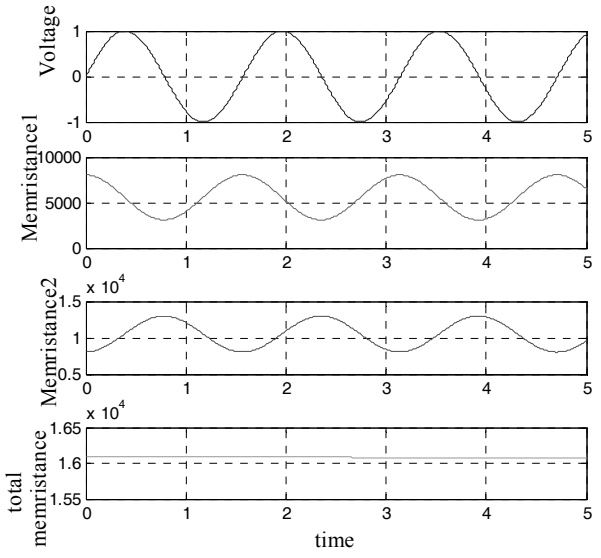


그림 9. 반대극성의 멤리스터 두 개를 직렬로 연결한 회로에서 입력전압, 첫 번째 멤리스턴스, 두 번째 멤리스턴스 및 멤리스턴스 합

Fig. 9. Voltage, memristance 1, memristance 2 and total memristance vs. time for 2 memristors M_1(decrement type) and M_2(Incremental) in series.

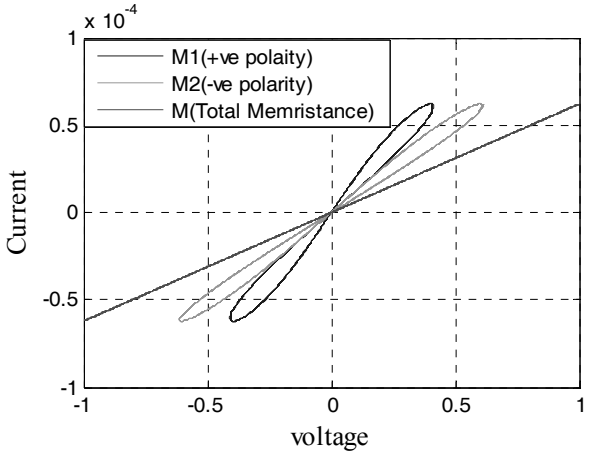


그림 10. 반대 극성의 멤리스터가 직렬로 연결된 회로에서의 전류-전압 그래프

Fig. 10. Current vs. voltage graph for memristance M_1, M_2 and overall memristance M for memristors M_1(decrement type) and M_2(incremental) in series.

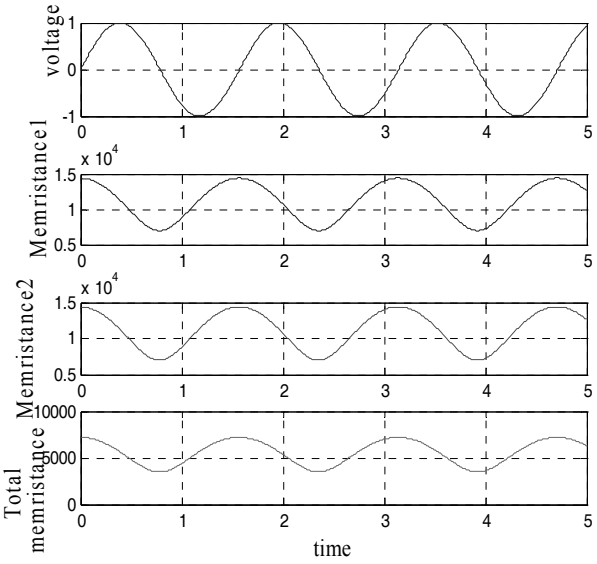


그림 11. 동일 극성의 멤리스터 두 개를 병렬로 연결한 회로에서 입력전압, 첫 번째 멤리스턴스, 두 번째 멤리스턴스 및 멤리스턴스 합

Fig. 11. Voltage, memristance1, memristance2, total memristance vs. time for two decrement type memristors in parallel.

voltage as shown in Fig. 7.

Here, for the same specifications, the pinched hysteresis loop at the same frequency is narrow as shown in Fig. 8 compared to that of the single memristor. When the frequency is increased, the hysteresis loop tends to be narrow thus becomes linear rapidly. If the number of memristors in series is increased, the pinched hysteresis loop becomes more and more linear compared to that of the single memristor. Fig. 8 shows pinched loop for 2 and 4 memristors in series.

If two memristors M_1 (decrement type) and M_2 (Incremental) are connected in series as shown in

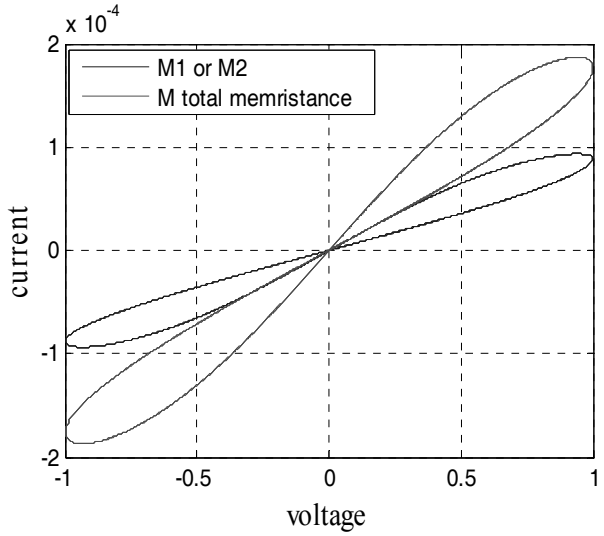


그림 12. 동일 극성의 두 멤리스터가 병렬연결된 회로에서의 전류-전압 그래프

Fig. 12. Current vs. voltage graph for two decrement type memristors M_1 and M_2 connected in parallel.

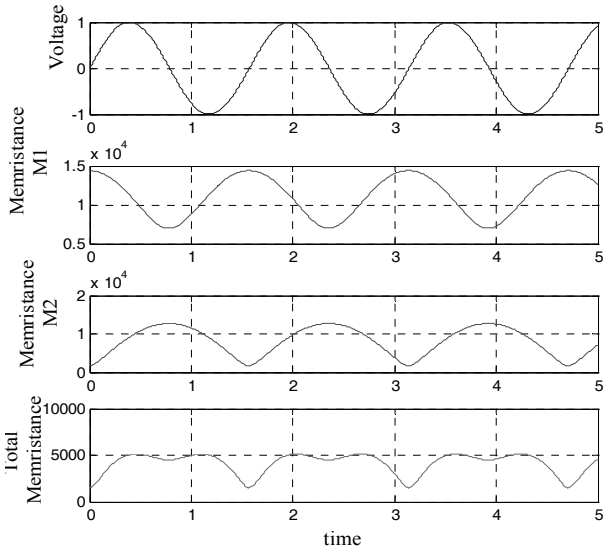


그림 13. 멤리스터 두 개를 병렬로 연결한 회로에서 입력전압, 첫 번째 멤리스턴스, 두 번째 멤리스턴스 및 멤리스턴스 합

Fig. 13. Voltage, Memristance1, Memristance2 and total memristance vs. time for memristors M_1(decrement type) and M_2(Incremental) in parallel.

Fig. 3(b), as the supply voltage increases, the value of memristance M_1 decreases whereas the memristance M_2 increases such that the net memristance becomes constant as shown in Fig. 9.

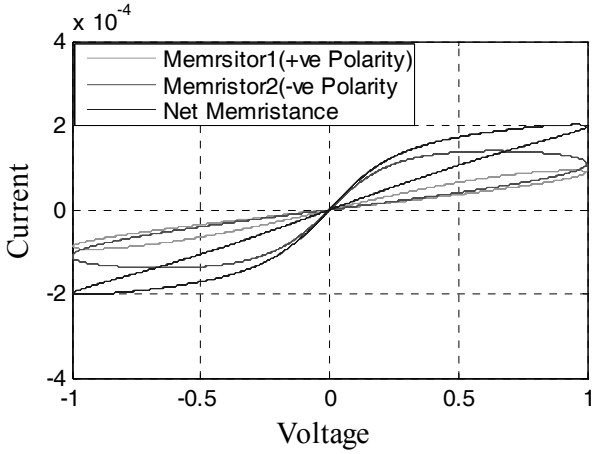


그림 14. 반대방향의 극성을 가진 멤리스터를 병렬로 연결한 경우, 전류-전압 그래프

Fig. 14. Current vs. voltage graph for memristors M_1(decrement type) and M_2(Incremental) connected in parallel at w=4.

As a result, the voltage drop across M_1 and M_2 is different. So the pinched hysteresis loop for each memristor is different as shown in Fig. 10.

If the two memristors M_1 and M_2, each decrement type, are connected in parallel then the memristance of M_1 and M_2 varies simultaneously as shown in Fig. 11. It is due to the fact that the voltage and current through both memristors are same. So, the hysteresis loop for each memristor is same for particular frequency as shown in Fig. 12.

Similarly for two memristors M_1(decrement type) and M_2(Incremental) connected in parallel as shown in Fig.4(b), the voltage across each memristor is same. However the current in each memristor is different.

So the memristance of M_1 decreases and the memristance of M_2 increases when the voltage is increased as shown in the Fig. 13. The current voltage characteristic plot is different for memristor M_1 and M_2 and hence the overall memristance is different at particular frequency as shown in Fig. 13. The pinched hysteresis loop for each memristor is different making the pinched loop narrow for overall circuit as shown in Fig.14.

V. Conclusion

Different configurations of memristor are analyzed. Computer Simulations were carried out for TiO_2 memristor model. The i-v characteristic of a single memristor showed that the variation of memristance is slow in a incremental memristor at the same frequency.

Similarly, when two memristors, each decrement type, are connected in series then the resulting pinched hysteresis loop tends to be narrow at the same frequency. Increasing the number of memristors, the pinched hysteresis loop becomes more and more linear. Thus overall series connection suppress the memristance either by increasing the number of memristors in series connection or the frequency. Since the size of memristors is quite smaller than the resistors, number of decremental memristors in series can be employed to make resistors. However one decrement and one incremental memristors in series are sufficient to provide the linear characteristics.

The two decremental memristors in parallel showed that the variation of memristance in each memristor is same and it is same as that of single decremental memristor. It reveals the fact that parallel connectivity doesn't affect the change in individual memristance. The net memristance range would be suppressed to some extent using a decrement type and an incremental memristors in parallel.

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