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Effects of some factors on the thermal-dissipation characteristics of high-power LED packages

Peng Fei Ji and Cheol-Hee Moon*

Green Display Device Lab, Department of Display Engineering, Hoseo University, Asan City, South Korea

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Decreasing the thermal resistance is the critical issue for high-brightness light-emitting diodes. In this paper, the effects of some design factors, such as chip size (24 and 35 mil), substrate material (AlN and high-temperature co-fired ceramic), and die-attach material (Ag epoxy and PbSn solder), on the thermal-dissipation characteristics were investigated. Using the thermal transient method, the temperature sensitivity parameter, R_{th} (thermal resistance), and junction temperature were estimated. The 35-mil chip showed better thermal dissipation, leading to lower thermal resistance and lower junction temperature, owing to its smaller heat source density compared with that of the 24-mil chip. By adopting an AlN substrate and a PbSn solder, which have higher thermal conductivity, the thermal resistance of the 24-mil chip can be decreased and can be made the same as that of the 35-mil chip.

Keywords: light-emitting diode; thermal dissipation; thermal resistance; junction temperature

1. Introduction

Light-emitting diodes (LEDs) as the replacement of incandescent lamps are widely applied in many areas, such as in signaling, illumination, narrow-band light sensors, and non-visible applications. With their advantages of high efficiency, long life span, flexible fabrication, and environment friendliness, LEDs are currently popular among the consumers. For the development of high-brightness LEDs, both high performance and high reliability are required [1]. To attain these, the dissipation of heat by the LED itself is one of the obvious challenges. Much of the power is converted into heat, which will raise the junction temperature of the LED chip, will reduce the power conversion efficiency, and will finally affect the LED reliability (e.g., lifetime and color shift). At the same time, high temperature and heat will produce mechanical stress in the LED package structure and may lead to a series of reliability problems. The heat generation from the p–n junction of the LED chip has been identified as being responsible for a number of failure mechanisms, such as delamination at the interface, resin crack, active-region degradation [2], phosphor degeneration [3], bonded-wire failure, and detachment. Therefore, thermal management is the top priority in improving LED reliability and performance.

The thermal management of LEDs improves the thermal performance of LEDs by optimizing the material or structure. In general, thermal management can be divided into internal and external thermal management. Internal thermal management handles the thermal resistance from the junction to the package case, while external thermal management handles the thermal resistance from the package case to the ambient. Internal thermal management should be done during the structure design process, and it plays a significant role. External thermal management includes the selection of the cooling mode, heat sink design, and the selection of a substrate, chip, and die-attach material [4,5]. The die-attach material, also called *thermal-interface material (TIM)*, connects the different parts by filling the contact interface between them as a thermal-management solution.

The common parameters that are used for evaluating the thermal performance of LEDs are junction temperature and thermal resistance. Junction temperature is the temperature of the active-region crystal lattice, which has a vital effect on the thermal characteristics of LEDs [6]. Thermal resistance is also an important performance parameter that indicates the obstruction of the heat flow from the p–n junction to the ambient during operation. Thermal resistance, whose symbol is R_{th}, can be calculated using the following:

$$R_{\mathrm{th}} = \frac{\Delta T_{\mathrm{J}}}{P} = \frac{\Delta T_{\mathrm{J}}}{I_{\mathrm{F}} V_{\mathrm{F}}}, \tag{1}$$

where ΔT_{J} is the junction temperature rise, P is a given power, I_{F} is a forward current, and V_F is a forward voltage on the LED [7].

There have been many technical reports that have used thermal resistance to analyze the thermal behavior of the

*Corresponding author. Email: chmoon@hoseo.edu

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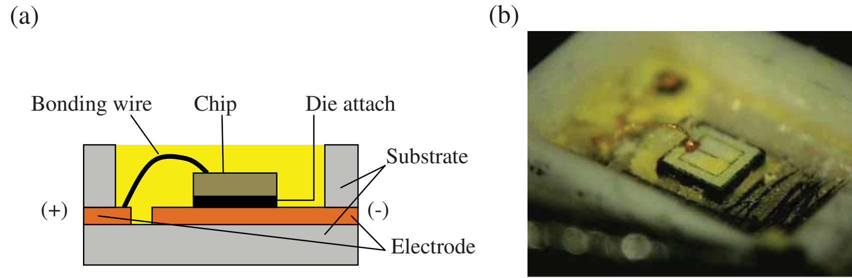

Figure 1. (a) Schematic structure and (b) photograph of the LED package that was used in the experiment in this study.

electronic packages for semiconductors or LEDs. Lalith Jayasinghe *et al*. investigated the influence of the changed current and ambient temperature on the thermal resistance of LEDs by estimating the junction temperature and measuring the board temperature [8]. Lianqiao Yang *et al*. investigated the effect of different thermal vias in ceramic packages on the thermal resistance of LEDs [9].

The junction temperature measurement methods can be divided into direct and indirect measurement methods. The direct measurement method measures the junction temperature with a thermocouple or an infra-red (IR) camera. As the junction temperature changes constantly, however, and as the measurement tool that is used has low precision, researchers often use the indirect measurement methods, such as the forward-voltage, peak-wavelength-shift, and high-energy-slope methods [6]. In the experiment in this study, the forward-voltage method was used. After measuring the junction temperature, the thermal resistance was tested. There are two methods for estimating the thermal resistance of an electronic package: the steady-state and transient methods. The steady-state method uses a thermocouple to determine the temperature change between the LED chip and the ambient (ΔT), with the LED chip on, which is divided by the input power to determine the thermal resistance using Equation (1). This method looks simple, but it is actually not easy to measure the temperature of an LED chip accurately, and it is impossible to obtain information on the thermal-resistance values for each layer. To investigate the thermal-dissipation behavior and the evolution of the temperature over each layer in the experiment in this study, the transient method, in which the junction temperature is monitored indirectly by measuring the change in the forward voltage when the LED chip is off, was used. The purpose of this experiment was to investigate the thermal-dissipation behavior of a high-power LED package. Of course, a large LED chip is needed, with the increase in input power applied on the LED chip. The use of a large LED chip will result in an increase in the price of the device and will be an obstacle to a compact design. Thus, in this paper, the thermal-dissipation characteristics of two different-sized chips, 24- and 35-mil chips, were compared to determine the restrictive conditions for increasing the chip size in connection with the die-attach and submount materials.

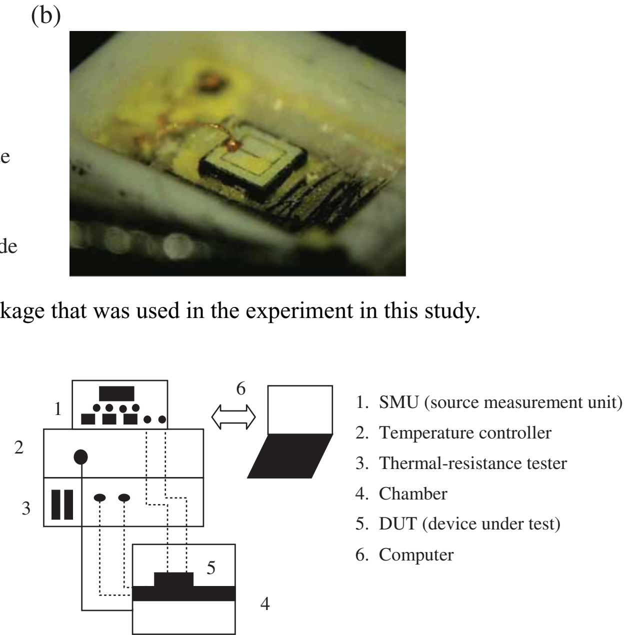

Figure 2. Configuration of the transient thermal measurement system.

2. Experiment

As can be seen in the schematic structure and photograph of an LED package in Figure 1, the LED package consists of a chip, a die attach, a bonding wire, an electrode, a package ceramic substrate, and an epoxy lens. Blue chips with 35 and 24-mil dimensions and with a vertical structure are mounted on a ceramic substrate, as shown in Figure 1(b). In this experiment, to investigate the influence of the chip size and substrate and die-attach materials separately, the other conditions (e.g., ambient temperature and input power) were set as constants.

As shown in Figure 2, the total LED package is located on the chamber. Below the cooling plate of the chamber is the ambient temperature sensor, which is utilized to test the ambient temperature (T_A) and helps the temperature controller to regulate the temperature in the chamber. As the ceramic substrate has good insulation, high thermal conductivity, and a low cost, it is widely applied as a submount in LED packages. Two kinds of ceramic substrates, AlN (aluminum nitride) and high-temperature co-fired ceramic (HTCC), were used as submounts in the experiment in this study. For the die-attach material, Ag epoxy (product name: Ablestik) and PbSn solder were compared as the experimental factors. The materials and thermal properties of the ceramic substrate and die attach that were used for this experiment are given in Table 1.

3. Determination of the thermal resistance

A thermal-resistance tester (Metasystem^{TM}) was used to measure the thermal resistance of the LED package.

Table 1. Material and thermal properties of the ceramic substrate and die attach.

Component	Material	Length × width	Thickness	k (W/m°C)	R_{th} (°C/W)	Specificheat (J/kg°C)
Ceramic substrate	AlN	5 × 5 mm^2	0.64 mm	180	0.1	740
	HTCC			17	1.5	795
Die attach	Ag epoxy (Ablestik^{TM})	610 × 610 µm (24-mil chip)	30 µm	2.5	32	
		880 × 880 µm (35-mil chip)			16.7	
	PbSn Solder	610 × 610 µm (24-mil chip)	30 µm	28	2.9	290
		880 × 880 µm (35-mil chip)			1.5	

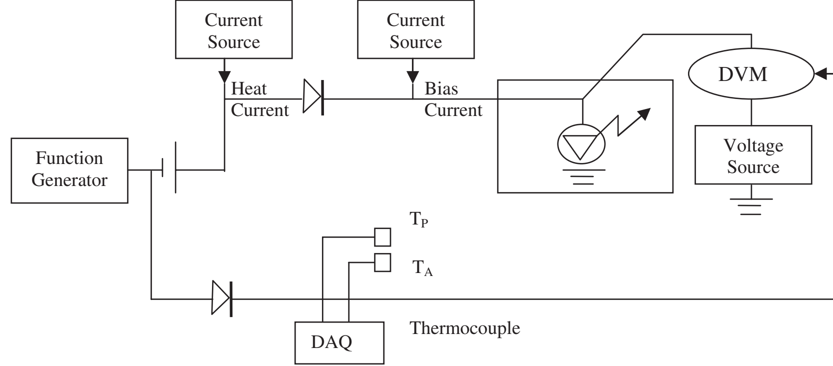

Figure 3. Determination of thermal resistance using the measurement system.

Metasystem^{TM} uses a three-step sequence to determine the thermal resistance, as described below.

3.1. *K-factor calibration*

In the first step in the determination of the thermal resistance of the LED package, the temperature sensitivity parameter (TSP) was measured, which is called the *K-factor.* As shown in Figure 3, the device under test was located in the chamber to be tested. The forward voltage of the LED diode was measured at different temperatures and was expressed as TSP. It has been reported that the relationship between the forward-voltage drop of a junction and the temperature of that junction is nearly linear, in which the K-factor is regarded as a constant [10]. Thus, in this experiment, the K-factors were calculated using Equation (2). For K-factor calibration, 1 mA bias current (I_{bias}) was used in three thermal-equilibrium environments, respectively, 25, 40, and 55°C:

$$K = \frac{\Delta T_J}{\Delta V_F}, \tag{2}$$

where ΔT_J is the change in the LED's junction temperature and ΔV_F is the change in the LED's forward voltage [11].

3.2. *Forward-voltage recording and junction temperature calculation*

In the second step, the forward-voltage transient data were recorded to determine the junction temperature change with the ambient temperature fixed at 25°. Figure 4 shows the applied current pulse and voltage change during the

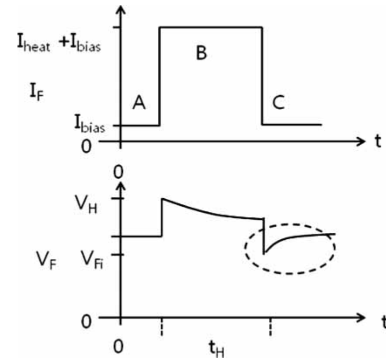

Figure 4. Applied current pulse and voltage change during the measurement of thermal resistance.

measurement of the thermal resistance. A bias current (I_{bias}) was applied during time A, as shown in Figure 4, and then the current level was quickly switched to a higher level ($I_{heat} + I_{bias}$) for time duration B until the steady state of the LED was obtained. Then, the driving current was replaced with the bias current, and the voltage transient data were recorded during the natural cooling (C in Figure 4). In this experiment, I_{bias} was 1 mA, and I_{heat}, 199 mA. As the K-factor is known from the first step, the junction temperature transient data can be obtained from the variation of the forward voltage in Figure 4, using the relationship between ΔT_J and ΔV_F in Equation (3).

3.3. *Differential structure function*

In the third step, the cooling curve was transformed into a Foster R–C network, which is called *network identification*

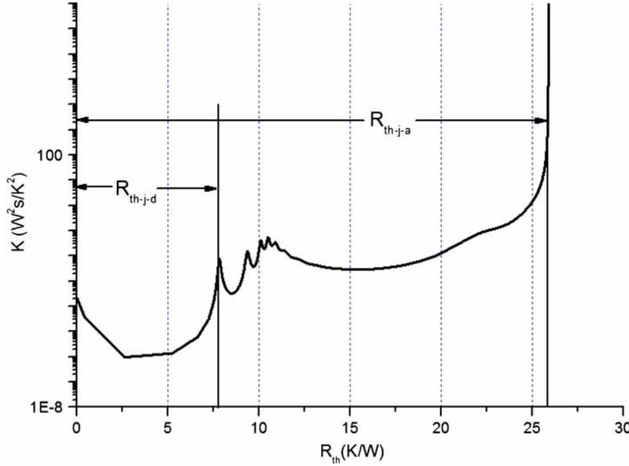

Figure 5. Differential structure function used for measuring the thermal resistance.

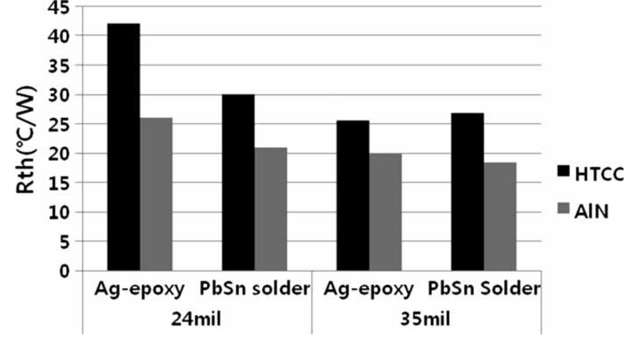

Figure 6. Comparison of the thermal-resistance ($R_{\mathrm{th,j\text{-}a}}$) values of the LED packages with different chip sizes and die-attach and ceramic-substrate materials.

by deconvolution. As the Foster network is theoretical, however, it was transformed into the Cauer network. The cumulative and differential structure functions are the graphical presentations of the Cauer R–C network [12–14]. The differential structure function is defined as the derivative of the cumulative thermal capacitance with respect to the thermal resistance:

$$K(R_\Sigma) = \frac{\mathrm{d}C_\Sigma}{\mathrm{d}R_\Sigma} = \frac{cA\mathrm{d}x}{\mathrm{d}x/\lambda A} = c\lambda A^2, \tag{3}$$

where A is the area of the heat conduction path, c is the specific heat of a material, and λ is the thermal-conductivity coefficient.

In Figure 5, the peaks in the differential structure function show good conducting materials, and the valleys represent the bad heat conductors. According to Equation (3), the differential structure function is a good tool for identifying either the geometry or material changes (or both) inside the package, as it is proportional to the square of the area of the heat conduction path and the product of the material parameters λ and c. Figure 5 shows the thermal resistance from the junction to the die attach ($R_{th,j-d}$) or the thermal resistance from the junction to the ambient ($R_{\mathrm{th,j\text{-}a}}$). For the investigation of the thermal-dissipation characteristics of the LED packages in this experiment, the $R_{\mathrm{th,j\text{-}a}}$ value was used.

4. Results and discussion

Figure 6 shows the data measured for thermal-resistance ($R_{\mathrm{th,j\text{-}a}}$), which is a line resistance between the junction and the ambient, for the LED packages with different chip sizes and die-attach and ceramic-substrate materials, which were chosen as experimental factors in this study. Actually, $R_{\mathrm{th,j\text{-}a}}$ is the sum of each resistance component, such as the LED chip, die attach, and ceramic substrate, which compose the LED package, because they are connected in series with one another in the direction of the heat dissipation toward the heat sink.

It can be seen in Figure 6 that for the 24-mil LED chip, the die-attach material and the ceramic substrate show differences in thermal-resistance values. For the 35-mil LED chip, however, the ceramic-substrate factor shows a meaningful difference in thermal-resistance values, but the die-attach factor does not. The thermal resistance of the bulk material is defined as

$$R_{\mathrm{th}} = \frac{L}{kA}, \tag{4}$$

where L is the thickness, k is the thermal conductivity, and A is the cross-sectional area of the component in the experiment in this study, as thermal dissipation occurs through the layers of the die attach and submount, outward from the package. Note that the conduction resistance of a medium in Equation (4) depends on the geometry and thermal property of the medium. With the disturbance of the interface resistance between different media, however, accurate evaluation cannot be achieved by investigating each medium separately. In the experiment, the total thermal resistance of the LED package, which includes the conduction resistance, interface resistance, etc., was evaluated to identify the factors that must be considered to improve the thermal-dissipation characteristics of LEDs. To understand this result, as shown in Table 1, the thermal resistance of each component was calculated using the dimensions and the thermal-conductivity values.

From the R_{th} calculation given in Table 1, it was shown that the difference in R_{th} is large (greater than 10 times) in the cases with different die-attach materials and ceramic substrates. The difference in R_{th} is only twice in the case of different chip sizes, depending on the area of the chip bottom. The measured $R_{\mathrm{th,j\text{-}a}}$ data, however, show larger differences depending on the chip size, but no difference was observed in the die attach in the case of the 35-mil chip size. This can be explained as follows. The main role of the die-attach material is to fill the gap between the LED chip and ceramic submount, and the thickness of the die

attach does not have any import because it is spread out by the applied pressure at an elevated temperature. Therefore, the effective thickness of the die attach is expected to be less than 30 μm, as indicated in Table 1. It is likely that the thermal resistance of the die attach depends more on the material than on the bonding condition. This is why there is no difference in $R_{th,j\text{-}a}$ with the die attach in the case of the 35-mil chip. For the 24-mil chip, however, there exist differences in $R_{th,j\text{-}a}$ with the experimental factors, as follows.

First, the $R_{th,j\text{-}a}$ value of the 24-mil chip is greater than that of the 35-mil chip for all the conditions. This can be easily explained by the fact that the bonding area of the 24-mil chip is only half of that of the 35-mil chip; as such, the die-attach material causes a difference in thermal resistance. The input power is almost the same when driving with the same current for the two kinds of LEDs. *Heat source density* is defined as

$$\frac{Q}{A} = \varphi, \tag{5}$$

where Q is the transferred heat energy, A is the cross-sectional area of the LED chip, and φ is the heat source density. From Equation (5), it can be seen that $\varphi(24)$ is greater than $\varphi(35)$. Thus, the effect of the thermal-dependent parameters related to thermal dissipation is greater in the case of the 24-mil chip than in the case of the 35-mil chip. As a result, the $R_{th,j\text{-}a}$ value of the 24-mil chip is greater than that of the 35-mil chip.

Second, it can be seen that the change in the $R_{th,j\text{-}a}$ value of the 24-mil chip is greater for different TIMs (Ag epoxy and PbSn solder). This can be explained as follows. Ag epoxy includes a great portion of epoxy, but PbSn solder contains only metal. It is generally accepted that the thermal conductivity of a metal slightly decreases (or increases in some cases) with the temperature, but the thermal conductivity of epoxy decreases on a greater scale with the temperature [15,16]. Therefore, it can be said that the $R_{th,j\text{-}a}$ value of the LED package with Ag epoxy is much greater than that of the LED package with PbSn solder due to the former's poor thermal conductivity at a higher temperature.

Third, the difference in $R_{th,j\text{-}a}$ between Ag epoxy and PbSn solder is greater in the case of the HTCC substrate than in the case of the AlN substrate. This can again be explained by the fact that the increase in package temperature, including junction temperature, was lower in the case of the AlN substrate due to its high thermal conductivity, as shown in Table 1.

Lastly, the inspiring result shown in Figure 6 is that the $R_{th,j\text{-}a}$ value of the 24-mil chip can be reduced and made the same as that of the 35-mil chip for the condition with an AlN submount and a PbSn solder. That is, using the good contact at the LED chip attachment and a good submount with high thermal conductivity, the thermal dissipation of the 24-mil chip can be enhanced and can be made the same as that of the 35-mil chip. This is meaningful because it shows that a compact design can be made by using a smaller chip.

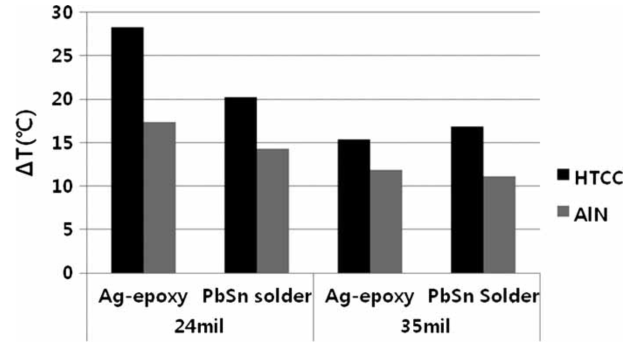

Figure 7. Comparison of the temperature rise values at the junction of the LED packages with different chip sizes and die-attach and ceramic-substrate materials.

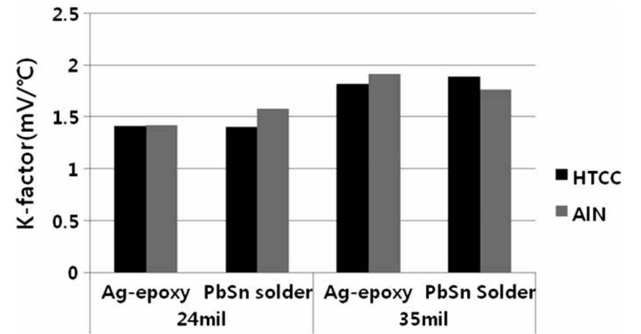

Figure 8. Comparison of the K-factor values of the LED packages with different chip sizes and die-attach and ceramic-substrate materials.

Figure 7 compares the temperature rise values at the junction of the LED packages with different chip sizes and die-attach and ceramic-substrate materials, showing the same tendency as that of $R_{th,j\text{-}a}$ in Figure 6. This can be explained by the fact that more heat is dissipated with the LED package system that has a lower $R_{th,j\text{-}a}$ value.

Figure 8 compares the K-factor values of the LED packages with different chip sizes and die-attach and ceramic-substrate materials. The 35-mil chip shows a higher K-factor than the 24-mil chip.

In the semiconductor basics, the I–V characteristic of the diode is defined as

$$I = I_0(e^{qV/kT} - 1), \tag{6}$$

where q is the elementary charge, V is the driving voltage, k is the boltzmann constant, T is the junction temperature, and I_0 is the reverse saturation current, defined as

$$I_0 = qA\left[\frac{D_p N_A}{L_p} + \frac{D_n N_D}{L_n}\right] e^{-qV_0/kT}, \tag{7}$$

where A is the cross-sectional area; D_p and D_n are the diffusion coefficients of the holes and electrons, respectively;

N_D and N_A are the donor and acceptor concentrations at the n- and p-sides, respectively; L_p andL_n are the hole and electron diffusion lengths, respectively; and V_0 is the contact potential. Equation (7) provides an explicit exponential dependence on the temperature and energy gap or contact potential. Owing to the same calibration temperature at 25° and the same fabrication material, it is considered that $I_0 \propto A$.

When $V > 0.1$, Equation (6) can be deduced as

$$I = I_0 e^{qV/kT}. \quad (8)$$

By differentiating Equation (7), the following equation can be obtained:

$$\frac{dV}{dT} = \ln\left(\frac{I}{I_0}\right)\frac{k}{q}. \quad (9)$$

As $I_0 \propto A$, it is regarded that

$$I_0 = A\alpha \quad (\alpha > 0). \quad (10)$$

When Equation (10) is inserted into Equation (9), the following equation can be obtained:

$$K = -\frac{dV}{dT} = -\ln\left(\frac{I}{I_0}\right)\frac{k}{q} = -\frac{k}{q}\ln I_F + \frac{k}{q}\ln A\alpha. \quad (11)$$

The fact that $A_1 = 35\,\text{mil}$ is greater than $A_2 = 24\,\text{mil}$ clearly explains the result.

5. Conclusion

To consider the feasibility of using a smaller LED chip for a compact design, the effects of some design factors, such as the dimensions of the chip and the substrate and die-attach materials of the high-power LED package, were investigated using the thermal transient method. The results are summarized as follows:

(1) The 35-mil chip showed better thermal dissipation, leading to lower thermal resistance and lower junction temperature, than the 24-mil chip. This can be explained by the smaller heat source density in the 35-mil chip than in the 24-mil chip.
(2) By using an AlN substrate, which has better thermal conductivity than an HTCC substrate, the thermal resistance of the 24-mil chip can be decreased. This can be explained by the fact that more heat is dissipated through a thermally high-conductive substrate, leading to a decrease in R_{th}.
(3) By using a PbSn solder as a die-attach material, the thermal resistance of the 24-mil chip can be decreased and made lower than that of Ag epoxy. Moreover, the amount of change in the thermal resistance with the different substrate materials (AlN and HTCC) was smaller in the case of the PbSn solder than in the case of Ag epoxy. It is likely that the thermal conductivity of the PbSn solder is less dependent on the temperature change than that of Ag epoxy, leading to a smaller change in the thermal resistance.
(4) It is encouraging that with the adoption of an AlN substrate and a PbSn solder, which have higher thermal conductivity, the thermal resistance of the 24-mil chip can be decreased and made the same as that of the 35-mil chip. This means that by using the good contact at the LED chip attachment, and a good submount with high thermal conductivity, the thermal dissipation of an LED chip can be enhanced, leading to a small chip and a compact design.

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