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Electrical stabilities of half-Corbino thin-film transistors with different gate geometries

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In this study, the bias-temperature stress and current-temperature stress induced by the electrical stabilities of half-Corbino hydrogenated-amorphous-silicon (a-Si:H) thin-film transistors (TFTs) with different gate electrode geometries fabricated on the same substrate were examined. The influence of the gate pattern on the threshold voltage shift of the half-Corbino a-Si:H TFTs is discussed in this paper. The results indicate that the half-Corbino a-Si:H TFT with a patterned gate electrode has enhanced power efficiency and improved aperture ratio when compared with the half-Corbino a-Si:H TFT with an unpatterned gate electrode and the same source/drain electrode geometry.

Keywords: half-Corbino; thin-film transistor; bias-temperature stress; current-temperature stress; gate geometry

1. Introduction

Interdigitated electrodes were first adapted in metal oxide semiconductor field effect transistors to achieve a high device-width-(W)-to-length-(L) ratio in a limited layout space [1,2]. To increase their ON-current characteristics, organic thin-film transistors (TFTs) were also made to employ these structures [3,4]. Comb-shaped electrodes have also been used to enhance the output power in field effect hydrogenated-amorphous-silicon (a-Si:H) solar cells [5]. In the a-Si:H TFT, one pair of interdigitated, the so-called 'fork-shaped' electrodes was introduced to reduce the gate-to-source capacitance and photo-leakage current, which reduce the high resolution and power efficiency of active-matrix liquid crystal displays (AM-LCDs) [6,7].

These authors previously reported the designs and electrical properties of fork-shaped and half-Corbino a-Si:H TFTs for use in active-matrix organic light-emitting diode (AMOLED) displays [8–10]. In this paper, the electrical stabilities of half-Corbino a-Si:H TFTs are reported. More specifically, the effects of the gate electrode pattern on the half-Corbino TFT output characteristics were first studied. The detailed studies of the bias-temperature stress (BTS) and the current-temperature stress (CTS) that induced the electrical instability of half-Corbino TFTs with different gate electrode patterns were also reported. Finally, the effects of the gate electrode pattern on the electrical properties of half-Corbino TFTs, which are important for AM-LCDs and AMOLED devices, were investigated.

2. Experiment

As shown in Figure 1, two different types of half-Corbino a-Si:H TFTs were fabricated on the same glass substrate with the five-photomask process used in the processing of AM-LCDs. The detailed process steps can be found in a previous publication [10]. Both half-Corbino TFTs have source and drain electrodes with the same dimensions and consisting of a rod-shaped inner electrode ($R_1 = 5\ \mu$m) and a U-shaped outer electrode ($R_2 = 15\ \mu$m), while the bottom gate electrode had a structural difference in the two types of TFTs: (a) the unpatterned gate electrode was large enough to cover the entire region of the outer and inner electrodes; and (b) the patterned gate electrode was only large enough to cover the device channel area with a 1 μm overlap between the outer and inner electrodes. To compare the output characteristics of the half-Corbino, a-Si:H TFTs with different gate electrode patterns for different drain bias conditions, the drain bias was swept from 0 to 20 V for a fixed gate bias (20 V), as in Figure 2. Next, the transfer characteristics of the half-Corbino a-Si:H TFTs with different gate electrodes were measured, after which the gate bias was swept from 25 to 0 V and was swept again from 0 to 25 V for various drain voltages, to extract their electrical parameters.

A series of BTS and CTS measurements on the two types of half-Corbino TFTs was performed, using a semiconductor parameter analyzer (HP 4145B), under accelerated stress conditions, by setting the stress temperature at 27 and 80°C [11]. The total stress time (t_{STR}) was 10,000 s, and the stress test was interrupted for only 1 min, to measure the transfer characteristics. Both the linear and saturation region transfer

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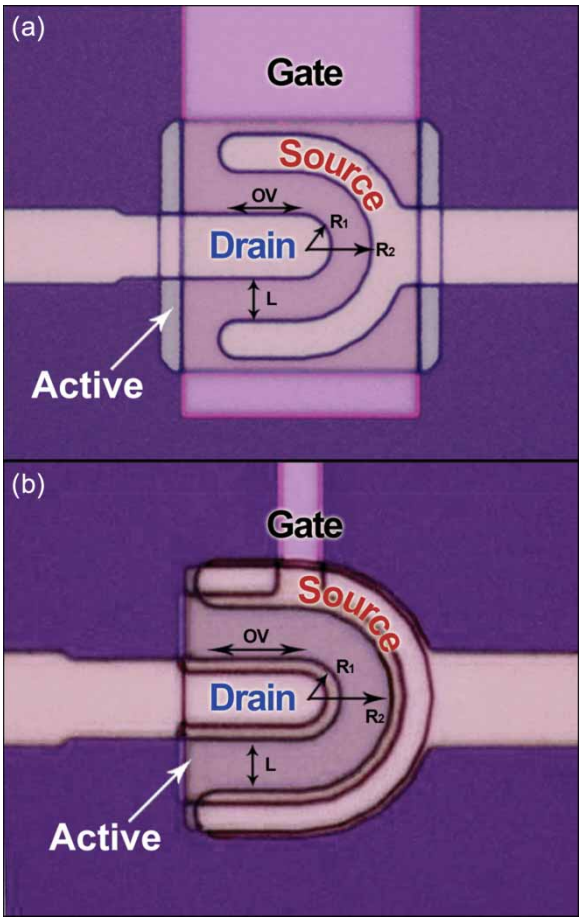

Figure 1. Top views of the half-Corbino a-Si:H TFTs with (a) unpatterned gate electrodes and (b) patterned gate electrodes, where the overlap (OV) is defined as 10 μm and the channel length (L) is defined as 10 μm.

curves of the half-Corbino TFTs were measured. Prior to the measurement, a 10 min stabilization time was allowed before the measurement to prevent thermal shock. During the BTS experiments, a constant gate bias ($V_{GS} = 40$ V) was continuously applied while a drain and a source were connected to the ground ($V_S = V_D = $ GND), as shown in Figure 3(a). During the CTS experiments, I_{STR} was continuously applied to the drain of the TFTs, and the gate was biased at 20 V, as shown in Figure 3(b). The source of the TFT was grounded while the stress current was set at 4 μA. The stress current reflects the current level that corresponds to the OLED luminance of 10,000 cd/m^2 for the emission efficiency of 12.5 cd/A and the 100 × 50 μm^2 pixel size [12]. The threshold voltages were extracted using the maximum slope method, which determines the threshold voltages as the extrapolation of the current curve with the maximum slope to zero current over the stress time. The threshold voltage shift can be expressed as follows:

$$\Delta V_{TH}(t) = V_{TH}(t = t_{STR}) - V_{TH}(t = 0). \quad (1)$$

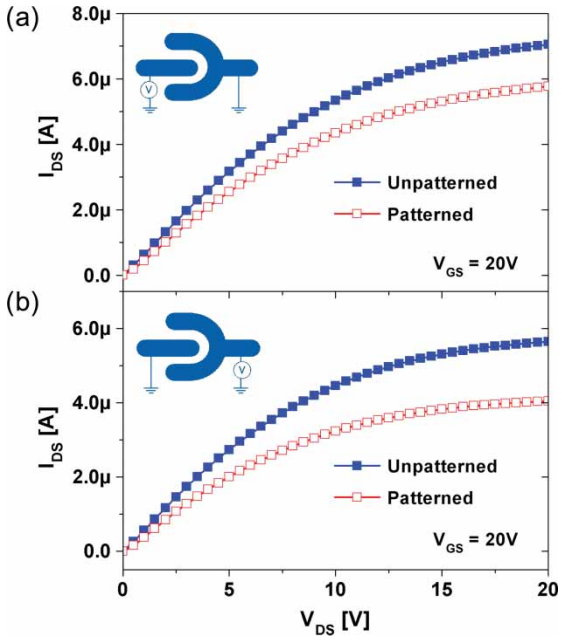

Figure 2. Comparison of the output characteristics of the unpatterned and patterned half-Corbino a-Si:H TFTs with $L = 10$ μm and OV = 10 μm. (a) A source bias was applied on the U-shaped electrode, and (b) a source bias was applied on the rod-shaped electrode.

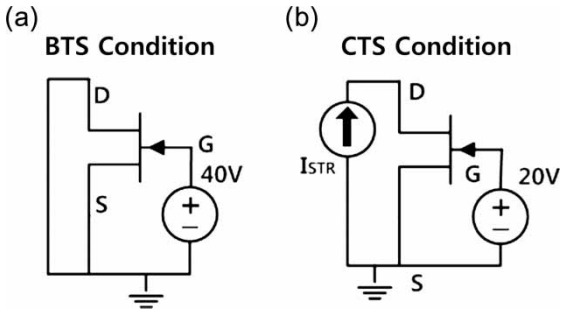

Figure 3. (a) BTS experimental setup for the gate bias stress condition ($V_{GS} = 40$ V), and (b) CTS experimental setup for the current stress condition ($I_{STR} = 4$ μA) used in this paper.

3. Experiment results and discussion

To compare the power efficiency of half-Corbino TFTs with unpatterned and patterned gate electrodes, the output characteristics of the two types of half-Corbino TFT were measured with the same bias conditions. Figure 2 shows the output current level of the unpatterned-gate-electrode half-Corbino TFT compared with that of the patterned-gate-electrode half-Corbino TFT. Drain voltage was applied on the inner rod-shaped drain electrode and was swept from 0 to 20 V. For the same gate voltage (20 V), as shown in the figure, the output current of the unpatterned-gate-electrode TFT (7.04 μA) was 1.22 times larger than that of the patterned-gate-electrode TFT (5.76 μA). Even for the other bias condition (drain on the U-shaped source

Table 1. Extracted parameters of the patterned- and unpatterned-gate-electrode half-Corbino TFTs for different source bias conditions (OV = 10 μm, L = 10 μm).

	Rod-shaped source		U-shaped source	
Bias condition	Unpatterned	Patterned	Unpatterned	Patterned
V_{TH} (V)	2.7	2.3	2.3	2.5
μ_{FE} (cm^2/V s)	0.53	0.36	0.51	0.40
SS (mV/decade)	432	434	407	457

on the rod-shaped electrode), the half-Corbino TFT still showed a higher output current (5.65 μA) compared with the fork-shaped TFT (4.05 μA). This difference in the output current levels of the half-Corbino TFTs with different gate electrodes is believed to have originated from the overlap area between the source and gate electrodes. As the overlap between the source and patterned gate electrodes is only 1 μm, it can be speculated that this overlap is not large enough compared with the required TFT characteristic length (L_T) [1], resulting in a reduced ON-current level and field effect mobility value. From the previously established observations that asymmetric electrode configuration results in asymmetric electrical properties depending on the bias condition [10], using the predefined geometric factors of the half-Corbino TFT, the electrical parameters of each a-Si:H TFT were extracted and are summarized for both bias conditions in Table 1.

Figure 4 shows the threshold voltage shift (ΔV_{TH}) of the two types of half-Corbino TFTs with the t_{STR}. In the BTS condition at an elevated temperature (80°C), the ΔV_{TH} values of the patterned- and unpatterned-gate-electrode half-Corbino TFTs when a drain bias was applied on the rod-shaped electrode, as in Figure 4(a), were 12.34 and 12.43 V at 10,000 s, respectively, while the ΔV_{TH} values of the patterned- and unpatterned-gate-electrode half-Corbino TFTs when a drain bias was applied on the U-shaped electrode, as in Figure 4(b), were 11.84 and 11.81 V at 10,000 s, respectively. The ΔV_{TH} values of the two types of half-Corbino TFTs were also measured under CTS conditions, as shown in Figure 5. Figure 5 shows the average ΔV_{TH} of the transistors, with error range bars for the same current stress condition: CTS condition I_{STR} = 4 μA. Under the CTS condition at the elevated temperature (80°C), the maximum ΔV_{TH} values of the patterned- and unpatterned-gate-electrode half-Corbino TFTs when a drain bias was applied on the rod-shaped electrode, as in Figure 5(a), were 3.84 and 3.85 V, respectively, while the maximum ΔV_{TH} values of the patterned- and unpatterned-gate-electrode half-Corbino TFTs when a drain bias was applied on the U-shaped electrode, as in Figure 5(b), were 4.09 and 4.17 V, respectively. From these measurements, it can be seen that the ΔV_{TH} values of the patterned-gate-electrode half-Corbino TFT are very similar within the measurement error range to those of the unpatterned-gate-electrode

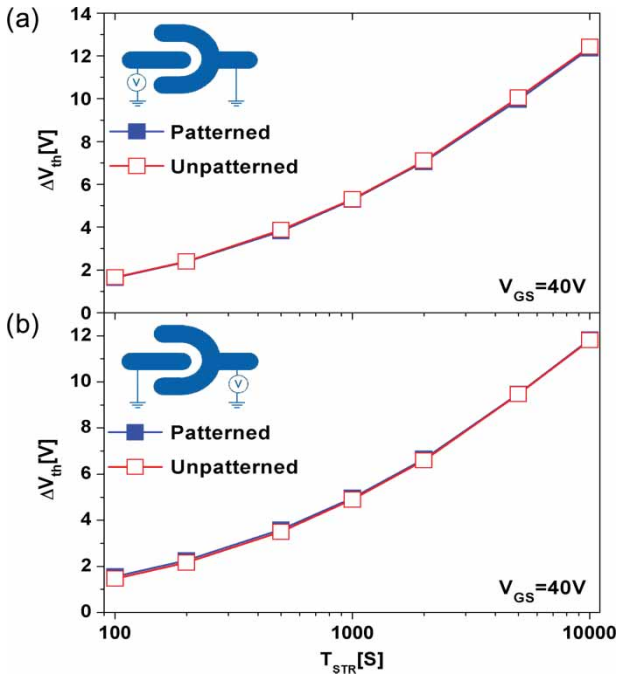

Figure 4. Threshold voltage shifts of the patterned and unpatterned half-Corbino a-Si:H TFTs as a function of stress time with the BTS condition: V_{GS} = 40 V. (a) A source bias was applied on the U-shaped electrode, and (b) a source bias was applied on the rod-shaped electrode.

half-Corbino TFT for both the BTS and CTS conditions. Therefore, it was shown that even though the two types of half-Corbino TFTs have different gate geometries, the threshold voltage variation of each transistor remains identical under both the BTS and CTS conditions, regardless of the gate electrode pattern in the half-Corbino a-Si:H TFT. Based on these experiment results, it can be said that the gate geometry does not affect the electrical instabilities, and that only the source/drain geometry influences the electrical stabilities of half-Corbino TFTs because such half-Corbino TFTs have the same geometry in the source and drain electrodes. In other words, the overlap area between the gate and source/drain electrodes does not have an impact on the electrical stability of the half-Corbino a-Si:H TFTs, but only on the ON-current levels, which are expected to be adjusted by changing the overlap width.

Like the fork-shaped a-Si:H TFT generally used in AM-LCDs [8], the half-Corbino TFT can be used as a switching TFT with a source bias on the rod-type electrode, thanks to its low gate-to-source capacitance (C_{GS}) and enhanced switching time due to its higher ON-current level compared with that of the fork-shaped TFT. In an AMOLED with a simple pixel circuit electrode, including at least two transistors, the dynamic power consumption is expressed by the following equation during the programming stage:

$$\text{Power}_{\text{program}} = fC_{\text{Total}}V_{\text{DS}}^2, \quad (2)$$

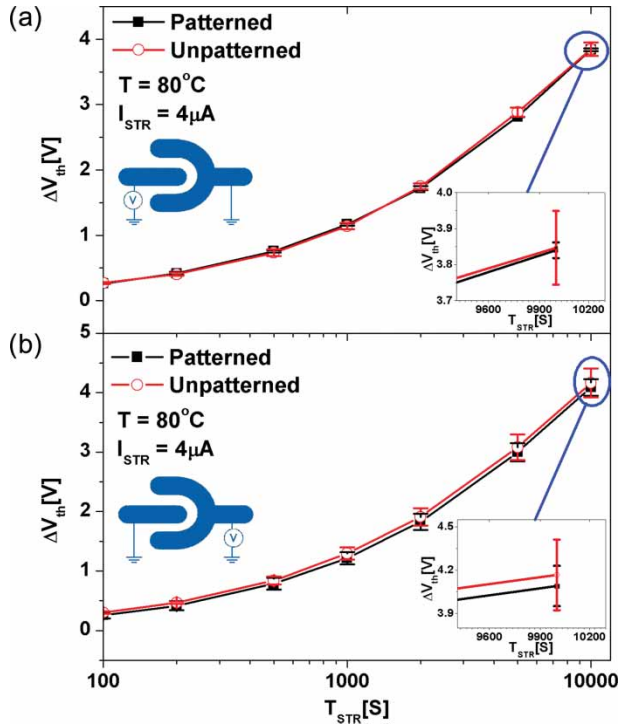

Figure 5. Threshold voltage shift of the patterned- and unpatterned-gate-electrode half-Corbino a-Si:H TFTs as a function of stress time with the CTS condition: $I_{STR} = 4\,\mu A$. (a) A source bias was applied on the U-shaped electrode, and (b) a source bias was applied on the rod-shaped electrode.

where f is the display driving frequency and C_{Total} is the sum of C_{GS}, C_{GD}, C_G, and C_{ST}. Here, C_G is the gate-to-channel capacitance and C_{ST} is the storage capacitance in the AMOLED. In general, the frame frequency and C_{ST} are fixed values in AMOLEDs. For the half-Corbino a-Si:H TFT with a patterned gate electrode, as the parasitic capacitance is reduced compared with a fork-shaped TFT or a half-Corbino TFT with an unpatterned gate electrode, the storage capacitor can be further reduced to maintain the same feed-through the voltage level, resulting in a lower total capacitance value of the switching TFT, while the electrical stability of the TFT remains as good as that of the half-Corbino TFT with an unpatterned gate electrode. Therefore, for a certain gray level (a fixed drain bias), the power consumption of each pixel can be linearly reduced, resulting in better power efficiency and an enhanced pixel aperture ratio due to the reduction of the storage capacitor.

4. Conclusion

In this study, the electrical stabilities of two types of half-Corbino a-Si:H TFTs were investigated under BTS and CTS conditions. It was found that even though the two types of half-Corbino TFTs have different gate electrode geometries, the threshold voltage variation of each transistor remains identical under both the BTS and CTS conditions, regardless of the gate electrode pattern in the half-Corbino a-Si:H TFT. By patterning the gate electrode of the half-Corbino TFT to minimize the parasitic capacitance, enhanced power efficiency and improved aperture ratio of the half-Corbino TFT could be achieved, which are promising characteristics for pixel circuit application in AMOLEDs and other flat-panel displays.

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