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Facilitation of the four-mask process by the double-layered Ti/Si barrier metal for oxide semiconductor TFTs

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The double-layered Ti/Si barrier metal is demonstrated for the source/drain Cu interconnections in oxide semiconductor thin-film transistors (TFTs). The transmission electromicroscopy and ion mass spectroscopy analyses revealed that the double-layered barrier structure suppresses the interfacial reaction and the interdiffusion at the interface after thermal annealing at 350°C. The underlying Si layer was found to be very useful for the etch stopper during wet etching for the Cu/Ti layers. The oxide TFTs with a double-layered Ti/Si barrier metal possess excellent TFT characteristics. It is concluded that the present barrier structure facilitates the back-channel-etch-type TFT process in the mass production line, where the four- or five-mask process is used.

Keywords: oxide TFT; barrier layer; back-channel-etch-type TFT; four-mask process

1. Introduction

Oxide semiconductor thin-film transistors (TFTs) have attracted much attention due to their advantages, such as their high electron mobility, good uniformity, and simple manufacturing process using sputtering [1]. As the etching selectivity between the oxide semiconductors and the source/drain (S/D) interconnections is not sufficient, etch-stop-layer (ESL)-type TFTs are conventionally being used as signal drivers. The TFTs that use oxide semiconductors are very sensitive to the surface conditions, such as adsorbed molecules and surface treatments [2–5]. Thus, the ESL is located on the topmost semiconductor layer and also acts as a protective layer.

The fabrication of ESL-type TFTs requires a six-mask process. On the other hand, the back-channel-etch (BCE)-type TFTs are widely used in amorphous Si, where only four or five masks are necessary for fabrication. The four- or five-mask process is more favorable than the six-mask process in terms of the production cost. Thus, the BCE-type TFTs will be extensively introduced herein for the next-generation oxide TFTs.

One of the challenging issues concerning the achievement of BCE-type TFTs is the development of a barrier layer. Generally, the barrier layer needs to satisfy the following conditions: (1) the interfacial reaction between the oxide semiconductor and the barrier layer should be minimized as it may cause composition and density fluctuation in the oxide semiconductor and barrier layers, and the S/D layer often peels off; (2) interdiffusion of the elements in both the oxide semiconductor and the barrier metal should not occur as it often increases the resistivity of the S/D interconnections, and as some elements (e.g. Cu and Mn) act as carrier killers in the oxide semiconductor [6,7]; (3) the contact resistivity between the oxide semiconductor and the barrier layer should be low to maintain good ohmic contact (high contact resistivity results in on-current reduction in the TFT operation); and (4) for the BCE TFTs, it is particularly important that the etching process not only maintains enough etching selectivity but also causes no surface damage to the semiconductor layer during the manufacturing process.

Due to their similarity with the a-Si TFT manufacturing process, Ti and Mo are widely used as barrier metals for the oxide semiconductor TFTs, but they do not have enough etching selectivity to the oxide active layer in the S/D wet-etching process. Furthermore, Ti often reacts with the oxide semiconductors at the interface, resulting in a reduction of the elements in the oxide semiconductors [8–10]. Thus, the barrier layer that meets the above-mentioned criteria is strongly desired. It is known that a layer consisting of Si can suppress the redox reaction to the oxide layer and is easily removed by additional dry etching using the same mask as that for the S/D layer. Therefore, it is expected that the double-layered Ti/Si barrier metal will be applicable to the BCE-type TFTs using Cu interconnections. In this paper, a double-layered Ti/Si barrier metal for the S/D Cu interconnections in the oxide semiconductor TFTs is proposed. The feasibility of the four- or five-mask process is examined.

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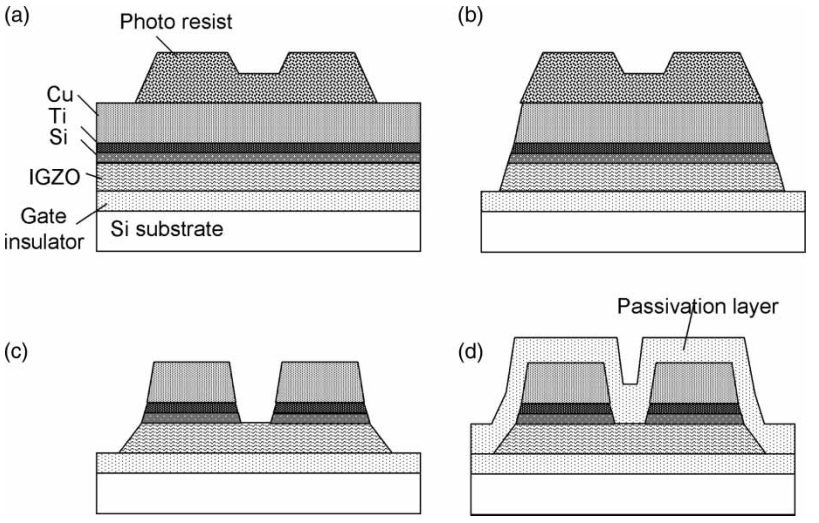

Figure 1. Schematic TFT structure and process flow using a stacked barrier layer: (a) after photolithography for etching the S/D and active layer; (b) after the wet etching of the Cu/Ti/IGZO interconnections; (c) after the dry etching of the Si interconnections using SF_6 plasma; and (d) after passivation layer deposition.

2. Experimental details

To evaluate the applicability of the Ti/Si barrier metal for the BCE-type TFT barrier layer, the interfacial reaction and the interdiffusion were examined. In addition, to test the process feasibility, the etching selectivity, contact resistance, and TFT characteristics were investigated.

The interfacial reaction/interdiffusion between the double-layered Ti/Si barrier metal and the oxide semiconductor film was analyzed using a cross-sectional transmittance electron microscope (TEM) and a secondary ion mass spectrometry (SIMS). The Cu/Ti/Si/$InGaZnO_4$ (IGZO) and Cu/Ti/IGZO-stacked films were deposited via DC magnetron sputtering.

To compare the performance of the BCE-type TFTs with that of the ESL-type TFTs, the characteristics of both were evaluated. Figure 1 shows the process flow of the TFTs that were used in this study. An n^+-Si substrate with a thermal oxide layer (250 nm) was used as a gate electrode and a gate insulator, respectively. IGZO semiconductor films with 50 nm thicknesses were deposited via DC magnetron sputtering. After the IGZO film deposition, the substrate was heated at 350°C for 1 h in an O_2 atmosphere, with H_2O, as a pre-annealing process [10]. The stacked Cu (300 nm)/Ti (10–50 nm)/n^+-Si (5–30 nm) layer was deposited via DC magnetron sputtering as S/D interconnections. A conventional Cu (300 nm)/Ti (50 nm) layer was also prepared for comparison. After the patterning of the Cu/Ti layers via wet etching or the lift-off process, the remaining Si layer was dry-etched using the SF_6 and Ar gas mixture. Then N_2O plasma irradiation was carried out on the IGZO surface (i.e. Si-etched surface) before the formation of passivation layers using SiN/SiO_2 films [11]. Post-annealing was carried out at either 250°C or 350°C for 30 min. The channel width (W)/length (L) was 210/20 μm for the ESL-type TFTs and 210/10 μm for the BCE-type TFTs. The measurements were done using a HP4145B parameter analyzer. The gate voltage (V_g) was swept between −30 and 30 V, while the drain voltage (V_{sd}) was fixed at 10 V.

The contact characteristics were measured using TFT devices and Kelvin patterns. To evaluate the etching selectivity, both the wet- and dry-etching rates were measured. For wet etching, a mixture acid etchant (KSMF-240; made by Kanto Chemical and originally developed for Ti/Al/Ti) was used. For dry etching, the conventional reactive-ion etching method was used. The gas flow ratio of the SF_6/Ar gas mixture was 20/80 sccm. The RF power and gas pressure were 30 W and 20 Pa, respectively.

The band diagram of the Ti/Si/IGZO-stacked structure was determined using a combined analytical system equipped with high-energy reflection electron energy-loss spectroscopy (EELS), ultraviolet photoelectron spectroscopy (UPS), and electron spectroscopy for chemical analysis (ESCA) in one vacuum chamber (high-energy reflection EELS/UPS/plasmon loss/ESCA: HiRUPE), which enabled all the measurements to be carried out without breaking the vacuum.

3. Results and discussion

Figure 2 shows a typical cross-sectional TEM image for a Cu/Ti/Si/IGZO-stacked film. A new layer was observed between the Ti and Si layers, which indicated that an interfacial reaction had occurred between the Ti and Si layers. On the other hand, no interfacial layer was observed between the Si and IGZO layers. These two layers remained homogeneous, indicating that no interfacial layer is formed between them during the thermal annealing. Figure 3(a) shows a cross-sectional TEM image of the Ti/IGZO-stacked film.

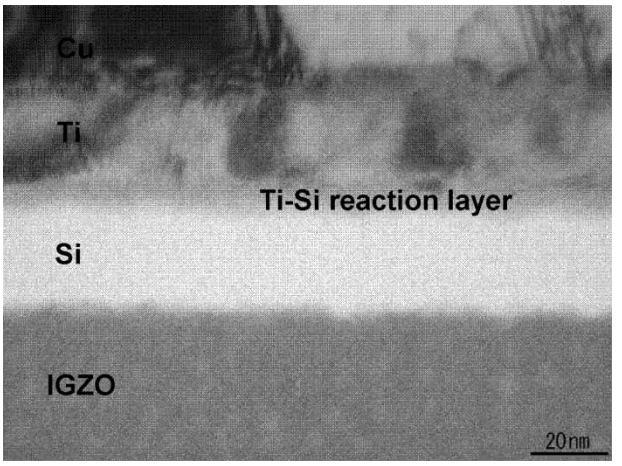

Figure 2. Cross-sectional TEM image of Cu/Ti/Si/IGZO after post-annealing (350°C, 30 min).

It can be seen that a redox reaction occurred at the interface between the Ti and IGZO layers. The reaction also caused void formation and crystallization in the IGZO layer, as indicated by the arrows. It should be noted that no hillock-like defects and peeling off of the S/D interconnections, as shown in Figure 3(b), were observed for the Cu/Ti/Si/IGZO-stacked film.

To evaluate the interdiffusion of each element, SIMS analysis was performed for the Cu/Ti/Si/IGZO- and Cu/Ti/IGZO-stacked films. As shown in Figure 4, In, Zn, and Ga were not observed in the Cu layer of the Cu/Ti/Si/IGZO-stacked films. Moreover, the depth profiles of the IGZO layer are similar to those of the others (In, Zn, and Ga), along with the depth. The results indicate that the Ti/Si barrier layer suppresses the interdiffusion between the S/D interconnection and the oxide semiconductor layer. On the other hand, the SIMS depth profile for the Cu/Ti/IGZO-stacked film shows that Ga atoms diffused into the Cu film (Figure 5), and that the homogeneity of the IGZO layer totally deteriorated. According to Arai *et al.* [8], the Ti/IGZO interfacial redox reaction deteriorates the in-plane uniformity in the IGZO TFT transfer curves. These TEM and SIMS results indicate that the Ti/Si barrier layer suppresses any defect formation due to the interfacial reaction and the interdiffusion between the oxide semiconductor and the barrier layer.

To evaluate the etching selectivity of the oxide semiconductor and the barrier layer, the etching rates of Cu, Ti, Si, and IGZO were measured for both dry and wet etching. The patterning process of the Cu/Ti/Si interconnection was as follows: (1) the Cu/Ti layer was wet-etched using KSMF-240 (Kanto Chemical) and (2) the Si layer was dry-etched using fluoride gas. The etching rates of Cu, Ti, and Si using KSMF-240 were 148, 120, and 2.8 nm/min, respectively. It was shown that the etching rates of Cu and Ti were more than 40 times faster than that of Si. On the other hand, the etching rates of Si and IGZO using SF_6 diluted by Ar were 116 and 0.6 nm/min, respectively, confirming that the etching rate of Si is about 200 times faster than that of IGZO. Figure 6 shows the cross-sectional TEM image of the Ti/Si/IGZO-stacked film after the Si dry etching. Note that the burr formed at the Ti edge was due to the patterning of the Ti layer using the lift-off process. This image indicates that the surface damage of IGZO is not introduced by the Si dry etching. Thus, the double-layered Ti/Si barrier metal has good etching selectivity. As a result, the Cu/Ti/Si interconnection can be patterned by the two-step etching process without damage to the IGZO surface.

To evaluate the contact properties between the barrier and IGZO layers, the *I–V* characteristics of the TFT devices were compared. Figure 7 shows the results of the *I–V* measurement for the samples without post-annealing, with post-annealing at 250°C for 30 min, and with post-annealing at 300°C for 30 min. Here, the change in the absolute *I* values was due to the change in the channel resistance between the S/D interconnections during the thermal annealing. It is shown that the sample without post-annealing indicates non-ohmic contact behavior. On the other hand, both annealing samples showed an ohmic-contact property. It was confirmed that the Ti/Si/IGZO contacts became ohmic after thermal annealing at temperatures higher than 250°C. The contact resistivities of the Ti/IGZO and Ti/Si/IGZO contacts are summarized in Figure 8. The contact resistivity of the Ti/Si/IGZO contact was in the order of $10^{-2}\,\Omega\,cm^2$ and was slightly larger than that of the Ti/IGZO contact, probably due to the barrier at the Si/IGZO interface. When

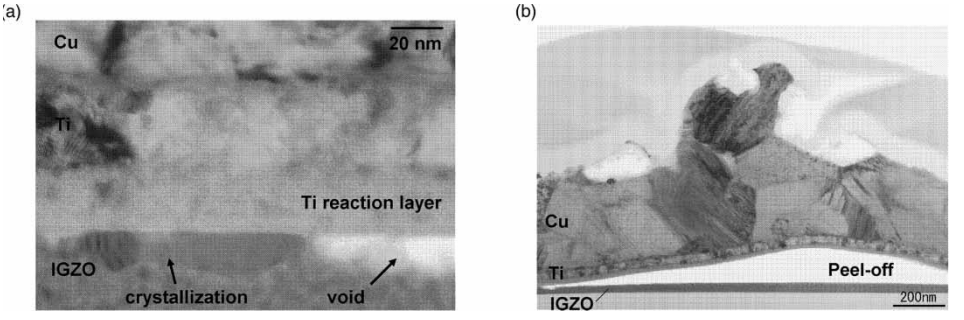

Figure 3. Cross-sectional TEM images of Cu/Ti/IGZO: (a) highly magnified image and (b) lowly magnified image.

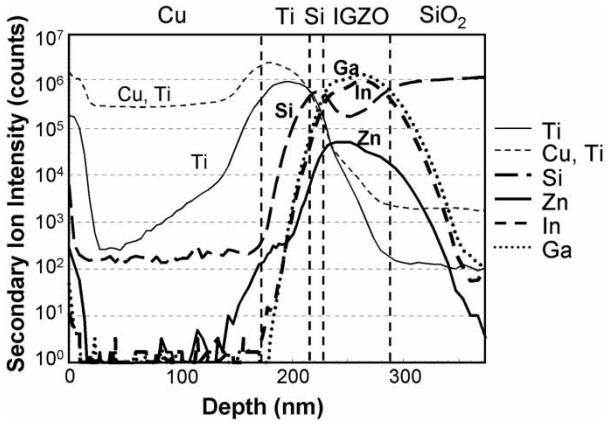

Figure 4. SIMS profiles of Cu/Ti/Si/IGZO after post-annealing (350°C, 30 min).

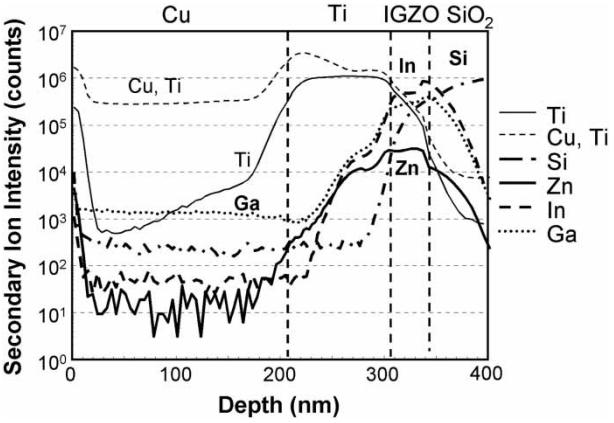

Figure 5. SIMS profiles of Cu/Ti/IGZO after post-annealing (350°C, 30 min).

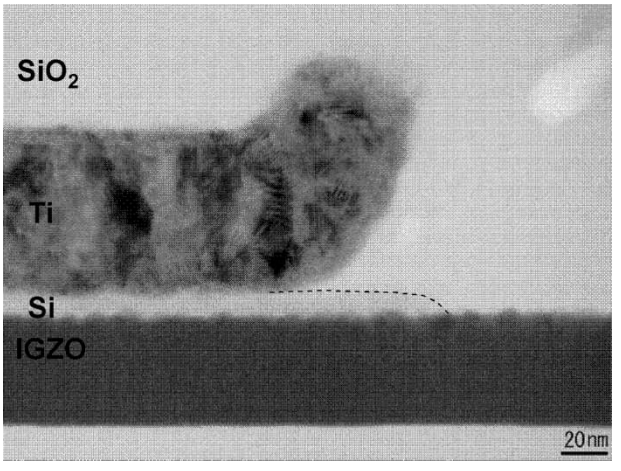

Figure 6. Cross-sectional TEM image of Cu/Ti/Si/IGZO after Si dry etching.

the contact resistance reaches about $1\,\Omega\,cm^2$, it becomes comparable to the channel resistance, assuming that the size of the contact is $200 \times 200\,\mu m^2$. It is seen that the contact resistivities of both the Ti/Si/IGZO and Ti/IGZO contacts

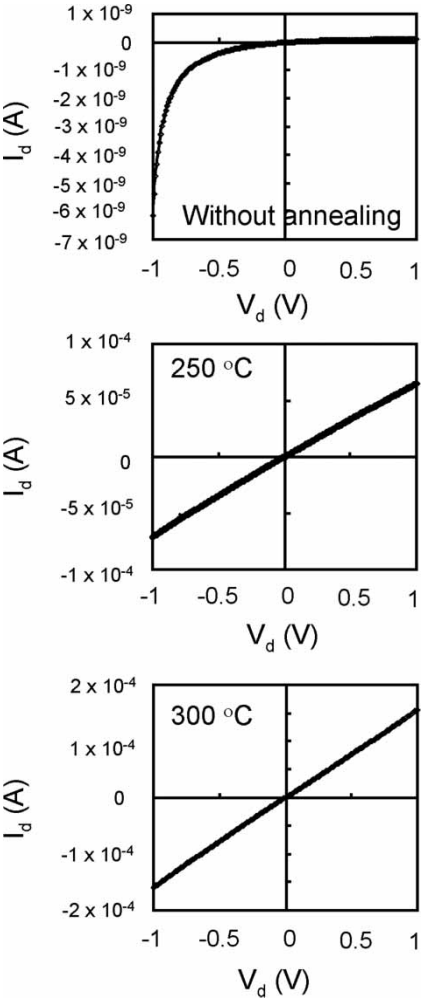

Figure 7. *I–V* measurement results: (a) without-annealing sample; (b) 25°C-annealing sample; and (c) 300°C-annealing sample.

were much smaller than the channel resistance. Thus, the contact resistance of the Ti/Si/IGZO contact is negligible.

Finally, the TFT characteristics of the BCE- and ESL-type TFTs were compared (Figure 9(a) and (b)). Both samples were annealed at 300°C for 30 min after the TFT fabrication. The values of V_{th}, SS, and μ_{FE} for the BCE- and ESL-type TFTs were 6.5 and 9.0 V, 1.01 and 0.93 V/decade, and 5.66 and 4.55 cm^2/V, respectively. The two TFT types have almost identical TFT characteristics, indicating that the proposed Ti/Si barrier layer is effective not only for the ESL-type TFTs but also for the BCE-type ones.

Regarding the protection mechanism as an interfacial reaction barrier, the standard free energies for the formation of In, Zn, and Ga oxides at 350°C are about −550, −630, and −650 kJ/mol O_2, respectively [12–14]. On the other hand, the standard-free energies for the formation of Ti and Si oxides at 350°C are about −850 and −880 kJ/mol O_2 [12–14]. Those of In, Zn, and Ga are lower than those of Ti and Si [15]. This means that the Ti and Si oxides are more stable than the In, Zn, and Ga oxides. Thus, redox

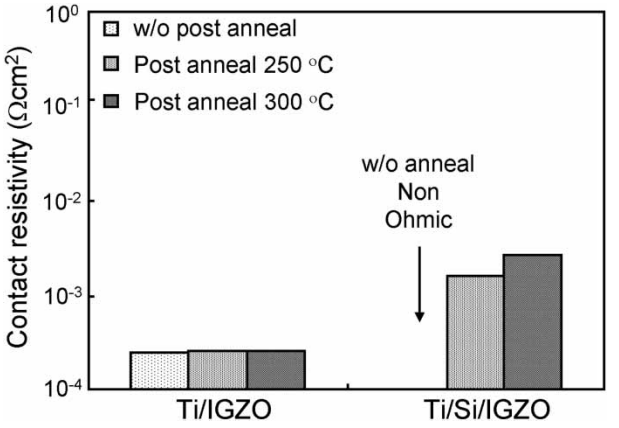

Figure 8. Cu/Ti/Si/IGZO and Cu/Ti/IGZO contact resistivity for the without-annealing and the post-annealing (250°C, 300°C, 30 min) samples.

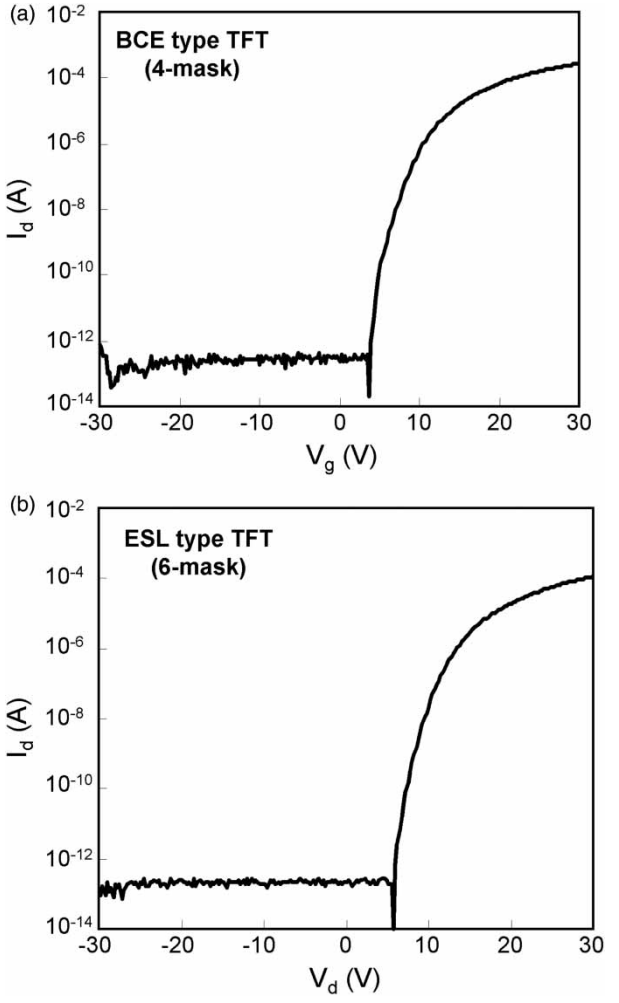

Figure 9. TFT transfer characteristics of Cu/Ti/Si/IGZO after post-annealing (300°C, 30 min): (a) BCE-type TFT; and (b) ESL-type TFT.

reaction can occur between the oxide semiconductor and the S/D metal layer as long as their standard-free energies of oxidation are lower than that of IGZO. This is true in the case of both Ti and Si. As can be seen in Figures 2 and 3(a), oxide layers were formed at the interface, but the Ti oxide grew faster than the Si oxide did, probably due to the different oxide diffusion mechanism [12]. It is thought that the interfacial reactions between the Si and IGZO layers are confined to a very thin area. Thus, the interfacial reaction and the interdiffusion do not cause problems such as crystallization and void formation in the IGZO layer.

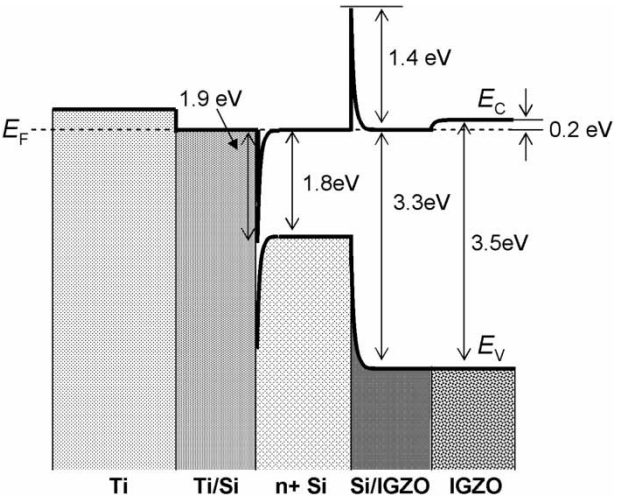

Figure 10. Band diagram of Ti/Si/IGZO as determined by HiRUPE.

Figure 10 shows the band diagram of the Ti/Si/IGZO layers determined via HiRUPE. The barrier was observed between the Si and Si/IGZO interfacial layers, but the interfacial layer was very thin after the thermal annealing, implying that the high electrical conduction is not on account of the formed barrier. It is also likely that the confined redox reaction induced oxygen-related defects at the interface, resulting in an increase in the tunneling current between the Si and IGZO layers.

4. Summary

The double-layered Ti/Si barrier metal for oxide TFTs that facilitates the BCE-type TFT process in the production line were demonstrated. The barrier layer met the criteria, such as limited interfacial reaction, no interdiffusion, low contact resistivity, and sufficient etching selectivities. It is considered that the growth rate of Si oxide is much slower than that of Ti oxide, resulting in excellent barrier properties. The Ti/Si-barrier-layer TFTs have almost the same characteristics between the BCE- and ESL-type TFTs. It is concluded that the present double-layered Ti/Si barrier layer can be used for the oxide semiconductor TFTs not only for the ESL type but also for the BCE type, which are fabricated through the four- or five-mask process.

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