

Warpage Simulation by the CTE mismatch in Blanket Structured Wafer Level 3D packaging

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In 3D wafer-stacking technology, one of the major issues is wafer warpage. Especially, The important reason of warpage has been known due to CTE(Coefficient of Thermal Expansion) mismatch between materials. It was too hard to choose how to make the FE model for blanket structured wafer level 3D packaging, because the thickness of each layer in wafer level 3D packaging was too small (micro meter or nano meter scale) comparing with diameter of wafer (6 or 8 inches). In this study, the FE model using the shell element was selected and simulated by the ANSYS WorkBench to investigate effects of the CTE on the warpage. To verify the FE model, it was compared by experimental results.

KEYWORDS: Solder joints, Warpage, FEM analysis, CTE, Wafer stacking

1. Introduction

3D wafer stacking technology has been great interest to microelectronic industries. There are four types of 3D stacking options, die-to-die stacking, die-to-wafer stacking, package-to-package stacking and wafer-to-wafer stacking. Among them, wafer-to-wafer stacking is great interest to many researchers because of smaller package size, lower cost, improved electrical performance, no need for known good die (KGD), and possibly elimination of underfill⁽¹⁻⁶⁾.

Among many technical challenges in 3D wafer stacking explained elsewhere, the wafer warpage is an essential and significant processing issue to be resolved for multi-stacked wafers.

As gradually thinning the thickness of the die and the substrate, warpage is raised on the reliability issue, especially, warpage caused by the CTE mismatch between layered materials of the stacked package. However, none of simulations have been yet. Such a warpage due to the stress concentration by grinding and bonding, has a great influence on the reliability and cracks^(7,8). In general, thin films have two kinds of residual stresses; namely, thermal mismatch stress and intrinsic mechanical stress.

Generally, it is difficult to choose the FE model for blanket structured wafer level 3D packaging, because the thickness of each layer in wafer level 3D packaging is too small comparing with diameter of wafer. In this study, the FE model using the shell element is selected and simulated by the ANSYS WorkBench to investigate effects of the CTE on the warpage. To verify the FE model, it is compared by test results.

2. Experiments

2.1 Experimental Results

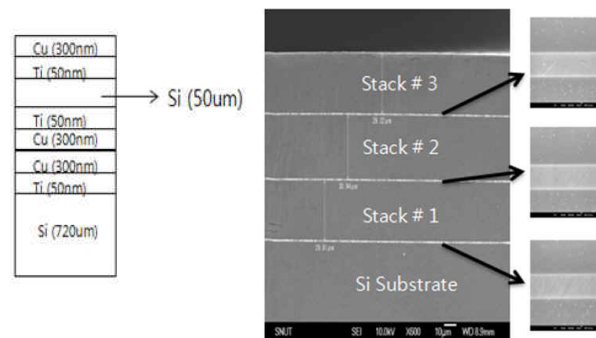


Fig. 1 Schematic diagram of stacked wafers

Fig. 1 shows a schematic diagram of stacked wafers. Ti and Cu were sputtered on the substrate Si for bonding. This process was performed at 400°C.

After bonding, through the grinding process, the top Si wafer of the stack #1 was 30µm. The stack #2 and the stack #3 were fabricated following the same procedure.

Fig.2 shows the wafer curvature of each wafer stack by warpage in test. Cu was deposited on the Si wafer. Cu on Si curvature was measured to 20µm. After stack #1 process, the curvature was decreased down to 15µm. Because of the initial Si wafer curvature,

5 μ m, Only Cu on Si was higher than Stack #1 relatively. After Stacks #2 and #3, the curvature of the wafer was getting increased. But the relative increment of wafer bow was getting reduced. Through the experiments, it was found that both the CTE mismatch and the thickness of the thinned Si influenced on the warpage of the stacked wafers⁽¹⁻³⁾.

2.2 Discussion

Based on the results of the experiments, as the stacking number of wafers increased, warpage became increasing absolutely. But the increment of warpage was getting reduced relatively. There are several reasons, such as the CTE mismatch between materials and the residual stresses that occurs during grinding and bonding processes.

In this study, by using the FE simulations it is investigated the phenomenon of warpage that occurs due to only the CTE mismatch.

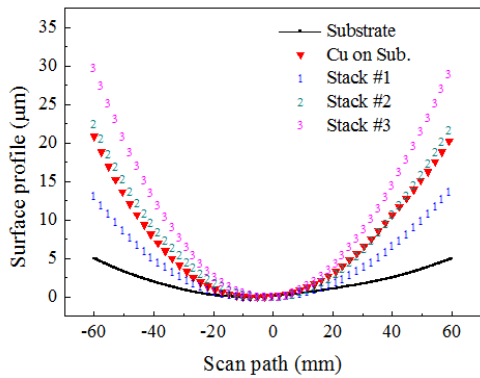


Fig. 2 Wafer Curvature by warpage in test

3. Modeling and Simulations

3.1 Modeling

3.1.1 Modeling and Meshing

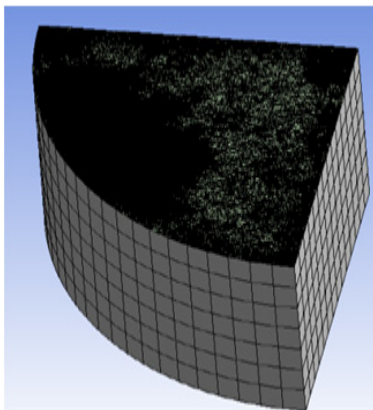


Fig. 3 1/4 FE modeling of single wafer using solid element

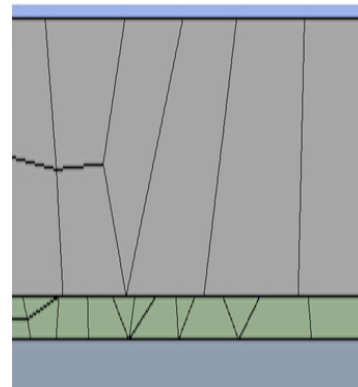


Fig. 4 Meshing of single wafer

For the simulations, the ANSYS 13.0 program is used. Using the solid element which is one of the methods to make modeling the stacked wafers, it is modeled as 1/4 size as shown in Fig. 3. However, using this element, meshing does not proceed due to very small thicknesses of Ti and Cu (micro meter or nano meter). As shown in Fig. 4, meshing does not proceed perfectly in Ti and Cu layers. Either, meshing quality is very low as shown in Fig 5. Meshing quality is better as it is closer to 1.

Because the FE model using the solid element does not fit to analyze the warpage. The other FE model using the shell element, is used as shown in Fig. 6. Unlike the solid element, its meshing goes smoothly in all of the layers such as Si, Ti and Cu as shown in Fig 6. Also, meshing quality is very good because it is close to 1 as shown in Fig. 7. Boundary conditions are free-free.

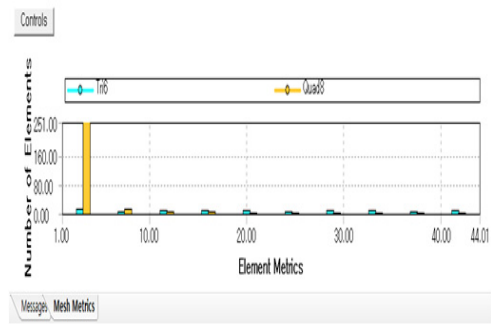


Fig. 5 Meshing quality of the FE model using the solid

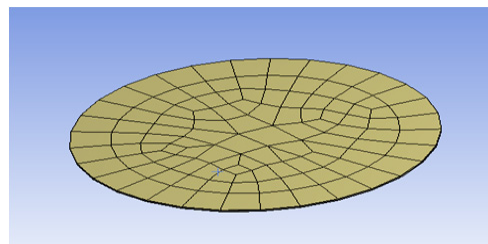


Fig. 6 Meshed FE model using the shell element

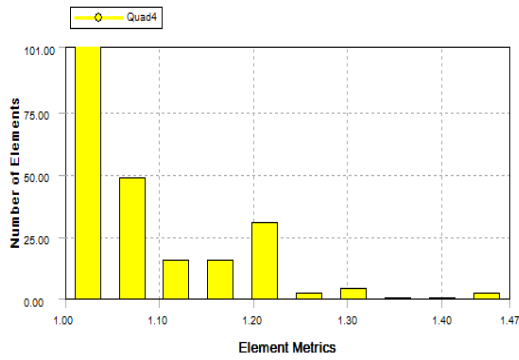


Fig. 7 Meshing quality of the FE model using the shell

Therefore, in this study, the FE model using the shell element is used to simulate warpage.

3.1.2 Transient thermal analysis on single wafer

Transient thermal analysis is carried out using the distribution of temperature by time on single wafer from the experimental data. The distribution of temperature by time as shown Fig. 8 is applied to bottom of the wafer. Total analysis time is 1,000 seconds which is the same as sputtering time.

Through the results of analysis as shown in Fig. 9, it is found that there is almost no difference in temperature between the bottom and the top of the wafer. Also, temperature is very fast transferred on the wafer as shown in Table 1.

3.1.3 Transient structure analysis

In order to simulate the warpage in the stacked wafers, a transient analysis is executed. All materials are applied in the elastic range and they have isotropic properties. Properties of materials used in simulations are shown in Table 2.

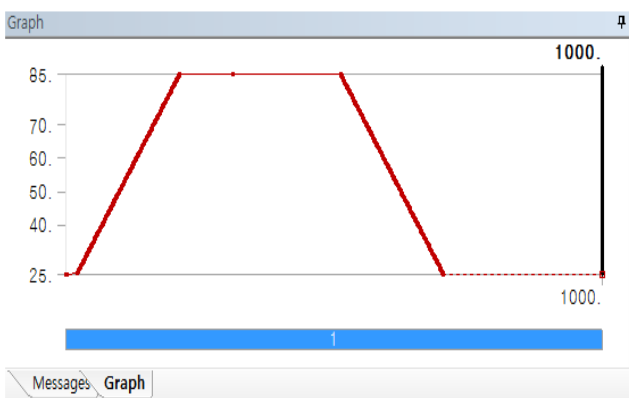


Fig. 8 Distribution of temperature in sputtering (x-axis : time (seconds), y-axis : temperature (°C))

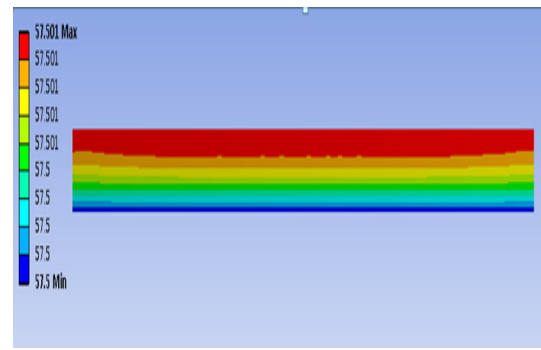


Fig. 9 Distribution of temperature on single wafer by transient thermal analysis

Table 1 Results of temperature transfer by transient thermal analysis

Time (second)	Temperature (°C) (Bottom of wafer)	Temperature (°C) (Top of wafer)
120	56.249	56.25
400	85	85
600	57.5	57.501
700	26.25	25.251
900	25	25

According to the experimental data, input temperatures for simulations are applied to the FE model. The distribution of temperature during bonding process is as shown in Fig. 10

Table 2 Properties of materials in transient analysis

	CTE(1/°C)	Poisson's ratio	Young's modulus (MPa)	Density (kg/m ³)
Si	2.501E-06	0.28	112,400	2,329
Ti	8.9E-06	0.34	116,000	4,500
Cu	1.64E-05	0.343	110,000	8,911

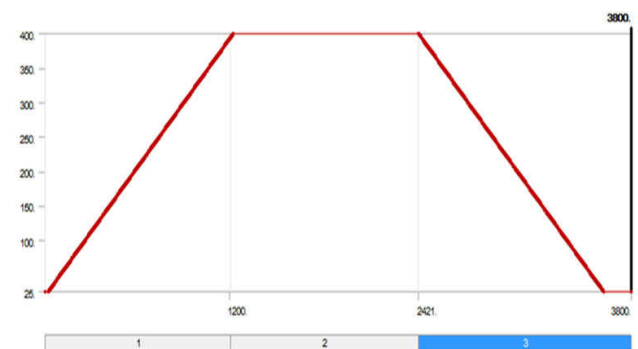


Fig. 10 Distribution of temperature during the bonding in simulations (x-axis : time (seconds), y-axis : temperature (°C))

3.2 Simulations & Results

The results of simulations are shown in Fig. 11. Maximum z-directional deformation by warpage on the center of single wafer is about $10.5\mu\text{m}$ at the highest temperature (85°C) as shown in Fig. 12. Also, distribution of von Mises stress on single wafer is about 157.5Mpa at the highest temperature (85°C). However, both values are almost negligible when temperature comes back to 25°C . It is because maximum stress (157.5Mpa) does not exceed the yield strength as shown in Table 3. Maximum z-directional deformation by warpage of wafers on stack #1 is about $8.12\text{e-}25\mu\text{m}$ at the highest temperature as shown in Fig. 13 and Fig. 14, and maximum von Mises stress by warpage of wafers on stack #1 is about $2.1\text{e-}5\text{Mpa}$ at the highest temperature. Unlike single wafer, both values are close to 0 regardless of time and temperature. Also, Maximum z-directional deformation and von Mises stress by warpage of wafers on stack #2 are similar to the results by warpage of wafers of the stack #3 as shown in Fig. 15 and Fig. 16.

Table 3 Yield strengths of materials

	Yield strength (MPa)
Si	7,000
Ti	140
Cu	33.3

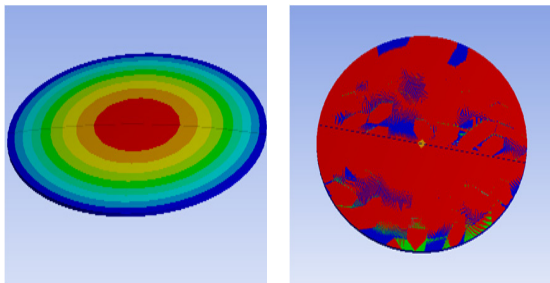


Fig. 11 Distributions of z-directional deformation and von Mises stresses for single wafer

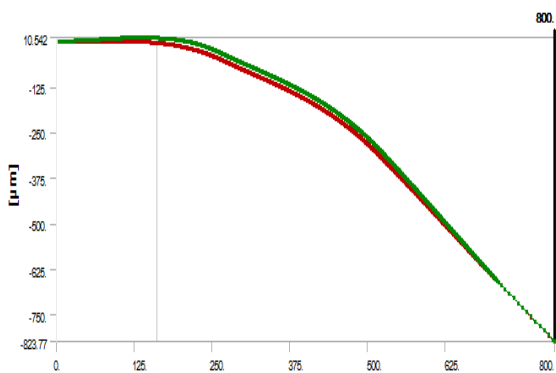


Fig. 12 Distribution of z-directional deformation by warpage of single wafer (x-axis : radial direction of wafer, mm)

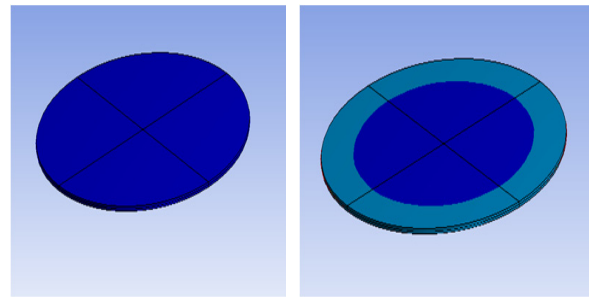


Fig. 13 Distributions of z-directional deformation and von-Mises stresses for wafers of stack #1

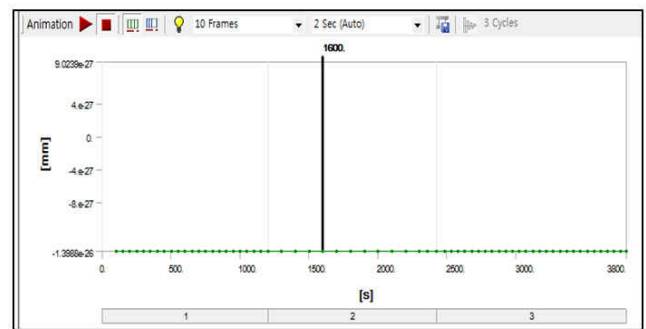


Fig. 14 Distribution of z-directional deformation by warpage of wafers of stack #1

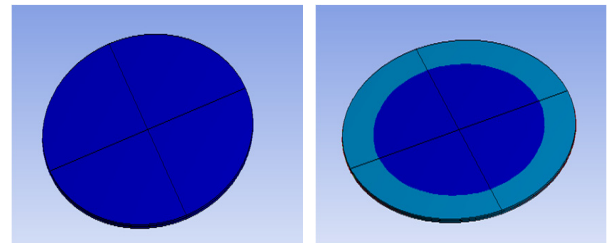


Fig. 15 Distributions of z-directional deformation and von Mises stresses for wafers of stack #2

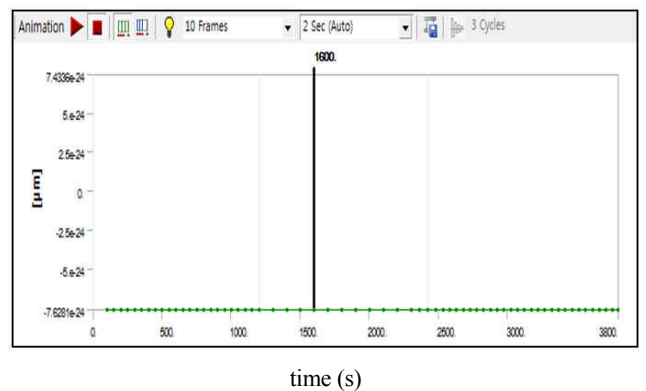


Fig. 16 Distribution of z-directional deformation by warpage of wafers of stack #2

Table 4 Results of warpage simulations

No. of stacks	z-directional deformation of warpage (μm)
Single wafer	10.5
Stack #1	8.12e-21
Stack #2	2.7e-24
Stack #3	2.4e-24

4. Conclusion

As the stacking technology has been applied to the wafer level 3D packaging, warpage became one of hot issues in the micro system packaging.

In this study, a new FE model for blanket structured wafer level 3D packaging was proposed and built, because the thickness of each layer in wafer level 3D packaging was too small comparing with diameter of wafer. The FE model using the shell element was selected and simulated by the ANSYS WorkBench to investigate effects of the CTE mismatch between materials on the warpage. The FE model for the simulations was verified by the tests.

In the simulation for the single wafer, the maximum deformation of z-direction related to the warpage occurred at the highest temperature, 85°C. However, when temperature dropped to 25°C, there was no more warpage, because von Mises stresses was not over the yield stresses of the Si, Cu and Ti.

The results of the simulations for other stacked wafers, such as the stack #1, the stack #2 and the stack #3, were close to zero regardless of changes in the temperature and the time. However, the results of the experiments showed micro-meter scaled values. The reasons of the difference between simulations and experiments for the stacked wafers were the structured symmetry and utilization of isotropic material properties in the simulations. Therefore, deformation of warpage due to CTE mismatch might be negligible.

In order to obtain a better FE model, the crystalline structure of the

Si wafer according to anisotropic properties should be applied. Also, Residual stress that occurs in the stacking process should be considered.

ACKNOWLEDGMENTS

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