

A Photovoltaic Power Management System using a Luminance-Controlled Oscillator for USN Applications

Ji-Eun Jeong*, Jun-Han Bae*, Jinwoong Lee**, Caroline Sunyong Lee**, Jung-Hoon Chun*, and Kee-Won Kwon*

Abstract—This paper presents a power management system of the dye-sensitized solar cell (DSSC) for ubiquitous sensor network (USN) applications. The charge pump with a luminance-controlled oscillator regulates the load impedance of the DSSC to track the maximum power point (MPP) under various light intensities. The low drop-out regulator with a hysteresis comparator supplies intermittent power pulses that are wide enough for USN to communicate with a host transponder even under dim light conditions. With MPP tracking, approximately 50% more power is harvested over a wide range of light intensity. The power management system fabricated using 0.13 μm CMOS technology works with DSSC to provide power pulses of 36 μA . The duration of pulses is almost constant around 80 μs (6.5 nJ/pulse), while the pulse spacing is inversely proportional to the light intensity.

Index Terms—Maximum power point tracking, load impedance control, luminance-controlled oscillator, ubiquitous sensor network

I. INTRODUCTION

Solar energy, as an alternative power source, has been attracting increasing attention as the reserves of fossil

energy are diminishing [1]. Different from the deposited fossil energy, solar energy instantly disappears unless it is well retrieved and securely stored. Management of the solar energy harvesting system is, therefore, as important as making decent photovoltaic devices.

In the design of a photovoltaic (PV) power management system, the most serious challenge comes from the fact that the amount of harvested power out of PV cells is sensitive not only to the external environmental parameters such as light intensity and temperature [2], but also to the internal structures and properties of the system like load impedance. To cope with the environmental variations, many research groups have proposed the efficient power management systems with maximum power point tracking (MPPT) [2-5]. The MPPT can be accomplished by different methods including design time component matching (DTCM), fractional open circuit voltage (FOC), fractional short circuit current (FSC), perturb and observe (P&O), and incremental conductance (INC). Among the various types of proposed MPPT's, the P&O and INC have been spotlighted because of their predominant efficiency [2, 5]. The P&O method, however, usually requires complicated circuits and power dissipation for time-of-flight power monitoring. Since the P&O method adopt negative feedback algorithm, the P&O method has slow response to the abrupt change of light intensity and it is another concern of P&O [6]. On the other hand, it is getting more important to control the load impedance for the maximum power efficiency, as the PV devices are expanding their applications to the ubiquitous sensor network (USN) [7, 8] using the dye-sensitized solar cell (DSSC) [9].

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In this paper, we propose a PV power management system for MPPT, which adaptively changes the load impedance along with light intensity and temperature without a complicated negative feedback. At first, we implemented the proposed system on a board with poly-Si solar cells and discrete components to check the feasibility of the system and observe the behaviors of internal signals. We also fabricated the power management IC to integrate it with DSSCs to form an energy harvesting system for the wireless sensor network.

The rest of this paper is organized as follows. In Section II, the characteristics of the PV cells utilized by the energy harvesting system are presented. In Section III, the mechanism of MPPT is described, and it is verified through the board-level feasibility study. The Section IV demonstrates the performance of the energy harvesting system where the proposed power management IC and DSSCs are integrated. Finally, Section V concludes the paper.

II. PV CELL CHARACTERISTICS

Fig. 1 shows the fabricated DSSC and its equivalent circuit. The TiO₂ powders are deposited using the nanoparticle deposition system on a 1.1 mm-thick indium-tin-oxide (ITO) glass substrate as described in [10]. The sonication of TiO₂ is followed by the sintering at 500°C for 1 hour. Finally, the electrolyte is injected between the sintered TiO₂ and ITO top electrode. The area and thickness of the DSSC are 1 cm² and 2 μm, respectively. The part of the supplied current (I_{PH}) from the PV cell flows to the internal P-N junction (D_{PV}) and the parasitic source resistance (R_{SH}). Therefore, the harvestable current (I_{PV}) is less than I_{PH}, and the amount of I_{PV} varies depending on the load resistance (R_L).

The measured current-voltage (I-V) and power-voltage (P-V) characteristics of the DSSC under constant

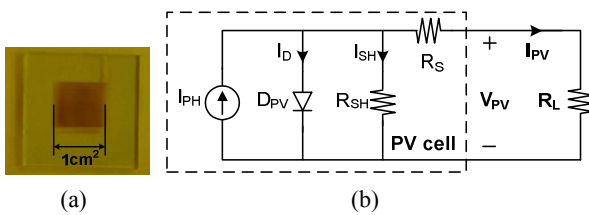


Fig. 1. (a) Micrograph of the fabricated DSSC, (b) equivalent circuit of the cell.

illumination intensity are shown in Fig. 2. P₂ in Fig. 2(a) represents the maximum power point. That is, the area of the rectangle whose diagonal is a line connecting the origin and P₂ becomes the maximum. When a load resistor is directly connected to the output of the PV cell, I_{PV} and V_{PV} are automatically determined by the resistance of R_L. The inverse of the slope of the straight line connecting the origin and the operating point equals to the R_L. Therefore, it is desired to choose proper value of R_L to put the system running in MPP condition (P₂). If the selected load resistance is different from the optimum value, the operating point (e.g. P₁) deviates far from the MPP.

The I-V curves under various light intensity were measured and overlapped in Fig. 3(a). Note that the MPP (V_{MPP} and I_{MPP}) gradually changes as the light intensity varies. Under the strong luminance condition, the operation point with a small load resistance is close to the MPP. However, a large load resistance is desired for better power efficiency in dim light. The optimum output power of the PV cell can be maintained if the load impedance is changed adaptively and quickly with the variations of the light intensity. In the proposed system

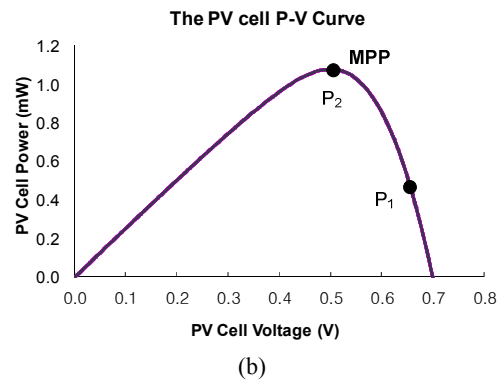
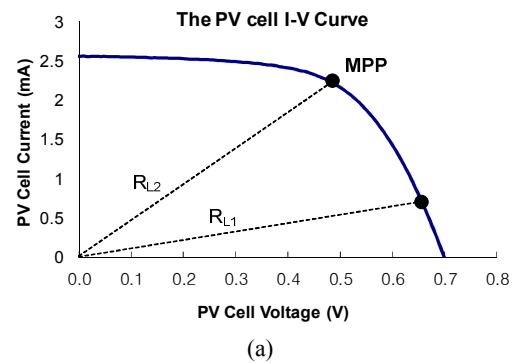
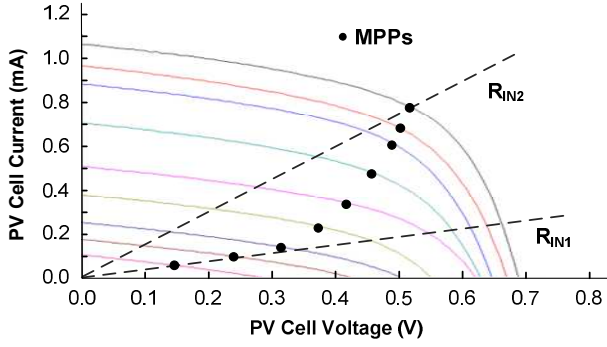
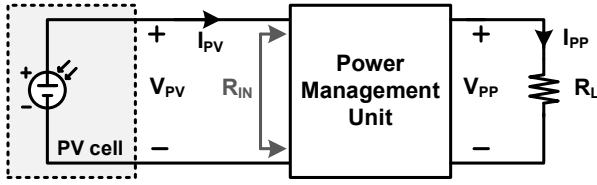


Fig. 2. (a) I-V curve, (b) P-V curve of the photovoltaic cell.



(a)



(b)

Fig. 3. (a) I-V curves at different illuminations, (b) power management unit for MPPT with resistive load.

shown in Fig. 3(b), the PV cell and the load are connected through a power management unit (PMU) so that the input resistance (R_{IN}) of the PMU can be seen by the PV cell as output resistance. The PMU adjusts R_{IN} to harvest the maximum power from the PV cell under various light intensities.

III. MPPT WITH IMPEDANCE CONTROL

1. Circuit Description

Fig. 4 discloses the block diagram of the power management system including PMU. For the comparative study, we also prepared a reference system where the output of the solar cell is directly connected to the load with the fixed resistance. In the adaptive system, a PMU intervenes between the PV cell and the load. Main PV cell and auxiliary PV cell are used for the system. Main PV cell provide main power to the PMU and the load like battery or electronic device. The auxiliary PV cell is used for current sensor. The P_{PV} is the output power of the main PV cell. The P_{PP} and P_0 are the powers transferred to the load with and without the PMU, respectively. The PMU is composed of a single stage charge pump and a luminance-controlled oscillator (LCO). For the MPPT under varying light intensity

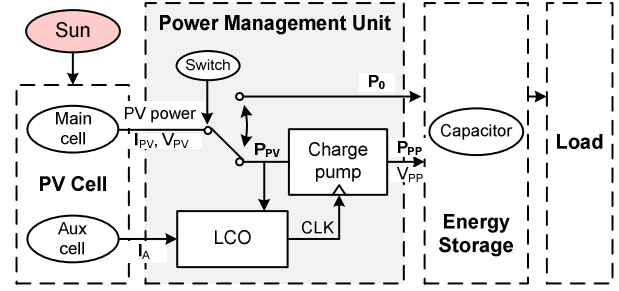
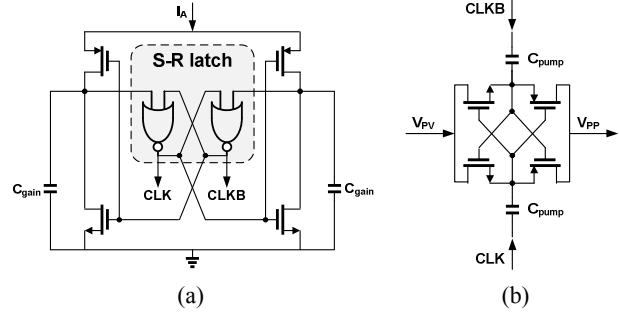


Fig. 4. Block diagram of the proposed MPPT system.



(a)

(b)

Fig. 5. Circuit details of (a) LCO, (b) 1-stage charge pump.

conditions, the PMU controls its input resistance by adjusting the clock frequency of the charge pump according to the following equation [11].

$$R_{IN} = \frac{1}{f_{CLK} \cdot C_{Pump}} \quad (1)$$

Frequency adjustment is achieved through an LCO that senses light intensity by detecting the current (I_A) flowing out of the auxiliary PV cell, and oscillates at the frequency proportional to I_A . A small auxiliary cell is separately used to avoid a loss on the main power path. Since LCO supplied power from the main PV cell, LCO senses current according to the light intensity exclusively.

The circuit implementations of the LCO and charge pump are shown in Fig. 5. The current from the auxiliary PV cell alternately set and reset the S-R latch, thus generating two complimentary clocks, CLK and CLKB. The output of LCO is a pair of non-overlapping clocks due to the S-R latch, which are suitable for operation of the subsequent cross-coupled charge pump. The cross-coupled charge pump is chosen because of its simple structure and high pumping efficiency [12]. The charge pump acts as an impedance transformer with help of LCO and as a voltage up converter as well. Since the

charge pump boosts V_{pp} maximum twice as high as the output voltage of PV cell, PMU can deliver the voltage higher than V_{pv} to the load.

2. Measurement Results

The core impedance control using charge pump frequency manipulation is implemented using commercially available poly-Si solar cells, discrete transistors, and logic gates on a board as shown in Fig. 6. Instead of using the small DSSC, large poly-Si PV cells are used in the preliminary circuit verification because the DSSC is too small to drive large parasitic loads and sustain leakage current of the discrete components. A light emitting diode (LED) is used as a load to confirm the enhancement of the power efficiency by PMU visually. The color and flickering frequency of the LED change with the amount of the supplied power. The size of C_{pump} is set to be 1.0mF considering the sizes of the PV cells and the LED load. Fig. 7 shows the measured characteristics of the PV cells and PMU. The output of the main PV cell is 2.12 V under the dim light condition (465 lux) resulting in the LCO clock frequency of 8.67 KHz and V_{pp} of 4.16 V. Meanwhile, in the bright light (1250 lux), V_{pv} , V_{pp} , and f_{CLK} are increased to 3.00 V, 6.00 V, and 46.07 KHz, respectively. When the luminance

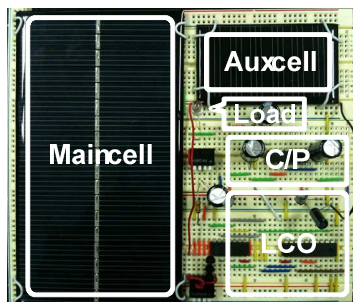


Fig. 6. Board-level implementation MPPT with PMU.

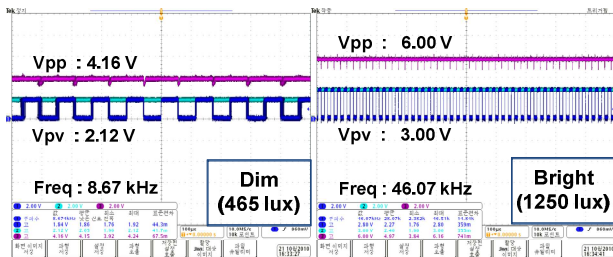


Fig. 7. Measured clock waveforms for charge pump at different luminance.

is weak, clock frequency is low and it becomes high if the luminance goes bright.

Fig. 8 depicts how the operating points of PV cells migrate with the various luminances. When the output of the PV cells is directly wired to the LED, the operating points ($P_{IN1} \sim P_{IN3}$) sit on a line defined by the resistance of LED, that is much larger than the optimum resistance in this experiment. The operating point deviates from the MPP as the illumination condition changes. However, in the PV system attached to the PMU, the input impedance of the PMU is adjusted owing to the frequency gain of LCO, and operating points ($P'_{IN1} \sim P'_{IN3}$) roughly track the MPPs. Although the design is not optimized, the operating points are close to the exact MPPs as shown in Fig. 8(b).

Fig. 9 compares the amount of power extracted from the PV cells and the dynamic MPPT efficiency with and without the PMU. The PMU is made of large discrete components, so that considerable amount of power is dissipated by the PMU, resulting in significant power

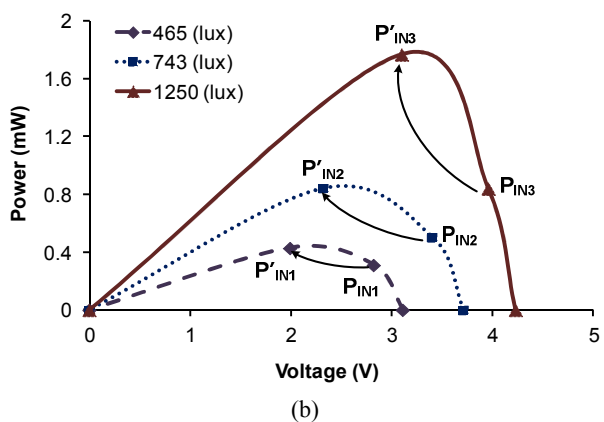
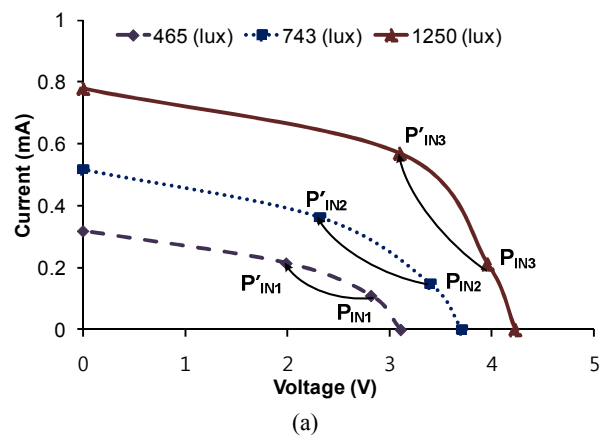


Fig. 8. Output impedance adjustment for MPPT (a) I-V curve, (b) P-V curve.

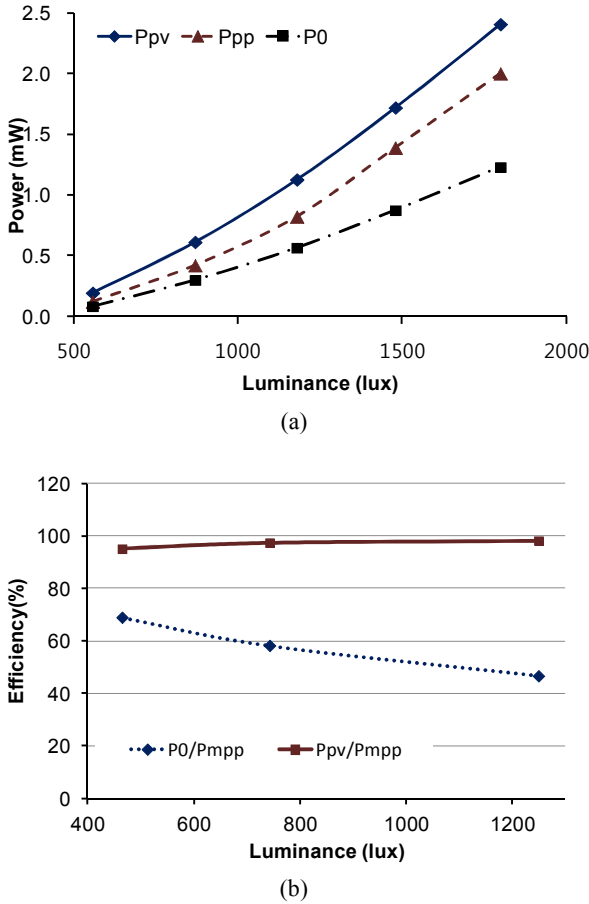


Fig. 9. Comparison of (a) retrieved power, (b) efficiency of the whole system.

loss especially under dim light conditions. Despite the power loss by PMU, 50% more power is harvested over the whole range of light intensity when MPPT is adopted.

IV. INTEGRATED CIRCUIT IMPLEMENTATION

1. Circuit Description

Power management system with LCO and charge pump is implemented as an integrated circuit. It is expected to work with weak power supply such as DSSC that is often accompanied with the wireless sensor network because it can be fabricated on flexible, transparent, or durable substrate [10]. Power management system for wireless sensor network delivers power to the sensor when sufficient power is accumulated to communicate with the host transponder [13], or keeps the surplus of power in the attached battery to keep periodic communication during the energy

harvesting is impossible.

The block diagram of the power management IC is described in Fig. 10. Besides the LCO and charge pump, a low drop-out (LDO) regulator and hysteresis comparator are added to dump power to the load only when the power efficiency is guaranteed. The V_{REF} generation block that is powered by V_{PP} , provides constant reference voltage for hysteresis comparator and LDO regardless of light intensity.

The circuit details of the hysteresis comparator and LDO are shown in Fig. 11. The comparator monitors the amount of the accumulated energy in V_{PP} node and decides whether it is ready to supply power to the load. The hysteresis prevents unnecessary dithering operation of the comparator. The size of hysteresis is proportional to the C_{HYS} . Therefore, C_{HYS} and C_{PP} determine the amount of charge dumped from V_{PP} node to V_{OUT} node at a time. If the load is a USN sensor, the amount of charge in a pulse must be sufficient to report sensor information to the host transponder. The V_{PP} level is sensed by an impedance divider with Z_1 and Z_2 that are parallel arrangement of large resistance and small capacitance to have both fast response and small leakage current [14].

Fig. 12 shows the simulated behavior of LDO with the hysteresis comparator. The upper and lower threshold

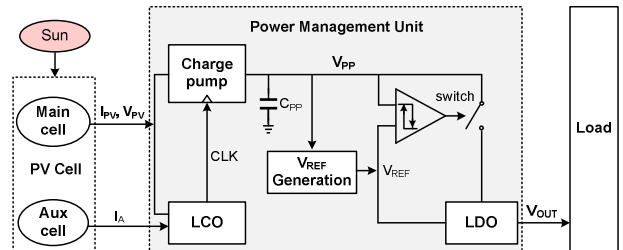


Fig. 10. IC implementation of battery charger with load regulating MPPT scheme.

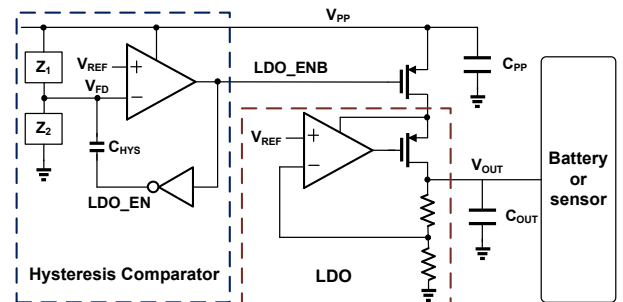


Fig. 11. Circuit details of hysteresis comparator and LDO.

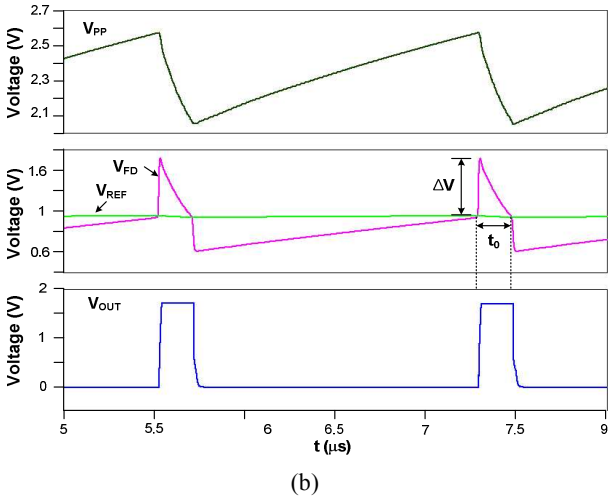
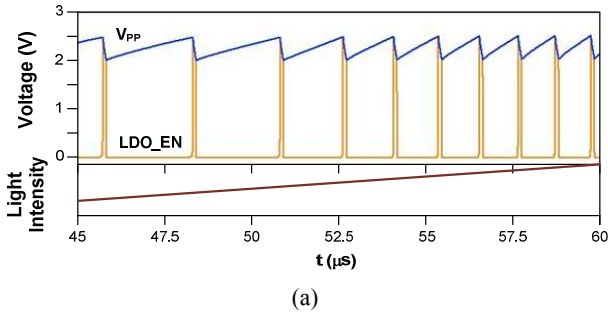


Fig. 12. Simulated behavior of (a) LDO under varying luminance, (b) hysteresis switching in the hysteresis comparator.

voltages of the hysteresis comparator are set to be 2.6 V and 2.0 V, respectively. The V_{PP} level ramps up at a rate proportional to $(C_{pump} * f_{CLK} * V_{PV} / C_{PP})$ by the operation of the charge pump while the LDO_EN is low. The V_{FD} node instantly jumps above V_{REF} by ΔV due to the charge injection by C_{HYS} when V_{FD} surpasses V_{REF} to pull LDO_EN up. The size of ΔV is

$$\Delta V = \frac{C_{HYS}}{C_{HYS} + C_{Z1} + C_{Z2}} V_{PP, \max} \quad (2)$$

where, $V_{PP, \max} \cong V_{REF} (R_{Z1} + R_{Z2}) / R_{Z2}$.

As the LDO_EN turns high, V_{PP} drops at a speed determined by the difference between the power supply by the charge pump and the power consumption through the load. If the consumption is much larger than the supply, the pulse width of LDO_EN is almost independent of the light intensity. The width of the intermittent pulses is

$$t_0 = \frac{\Delta V \cdot C_{PP}}{I_{load}} \left(\frac{C_{Z1} + C_{Z2}}{C_{Z2}} \right) (1 - \alpha) \quad (3)$$

where α represents charge relaxation on V_{FD} node and is inversely proportional to the $R_2 (C_{HYS} + C_{Z1} + C_{Z2})$. Because resistances in Z_2 and C_Z 's are large, α can be neglected in practice.

2. Measurement Results

The proposed power management IC was designed and fabricated using 0.13 μm CMOS technology. Fig. 13(a) and (b) show a micrograph of the die and layout details, respectively. The test setup is shown in Fig. 13(c). The packaged IC is connected with six DSSCs for the main PV cell and one DSSC for the auxiliary cell. Considering the requirements of operating voltage and current of the PMU, three DSSCs are combined first in parallel as a set, and two sets of the DSSCs are connected in series. The evaluation of the fabricated IC is carried out in the solar simulator (Sun 2000 Class A) [15].

Fig. 14(a) shows the waveform of V_{PV} and LDO_EN at different light intensities. V_{PV} is 1.134 V and LDO_ENB pulses arise every 20.3 μs when light intensity is 1.15 KW/m^2 . As the light intensity is increased to 1.5 KW/m^2 , V_{PV} increases to 1.192 V

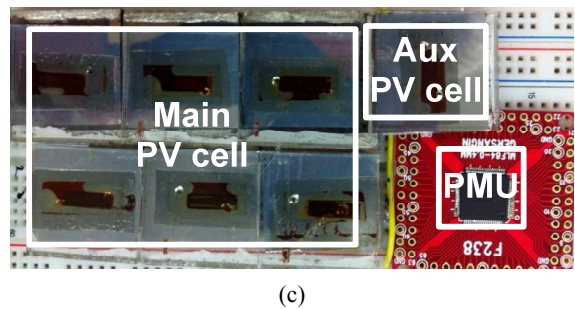
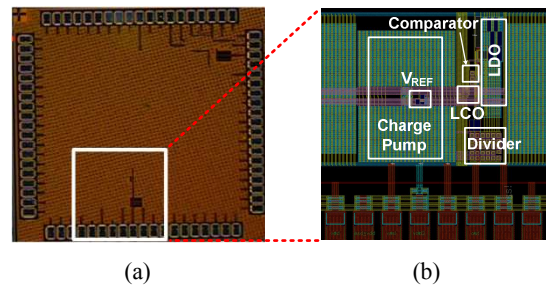


Fig. 13. (a) Chip micrograph, (b) layout of MPPT IC, (c) test setup for packaged MPPT IC with DSSC.

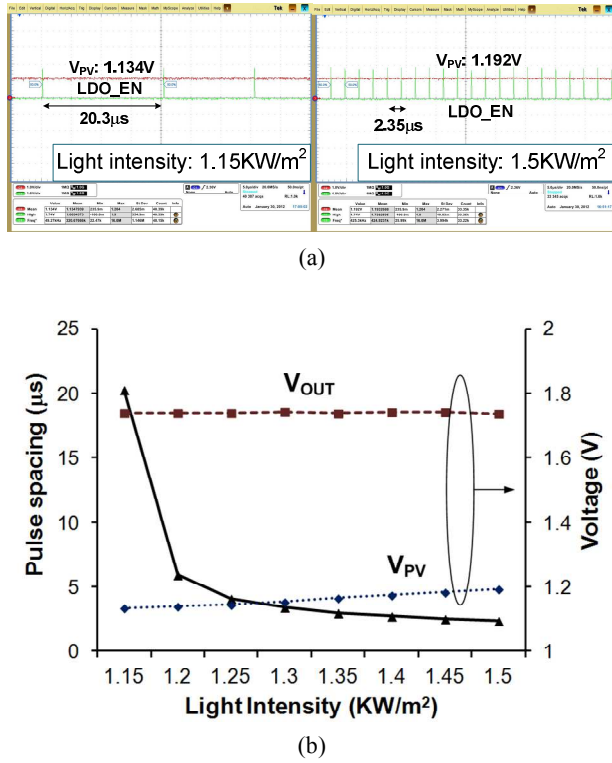


Fig. 14. (a) Waveform of measurement in two cases of light intensity, (b) V_{PV} , V_{OUT} , and pulse spacing under various light intensities.

yielding LDO_ENB pulses every 2.35 μ s. The width of pulse is approximately 80 μ s in average in the whole range of luminance if the load dissipates 36 μ A, delivering 6.5 nJ at every pulse. The energy per pulse can be increased by enlarging C_{pp} or gap between the two thresholds. The pulse spacing is shortened by increasing the illumination and the size of main cells. The V_{PV} , V_{OUT} , and period of LDO_ENB pulse under the light intensity from 1.15 KW/m² to 1.5 KW/m² are shown in Fig. 14(b). V_{OUT} is almost invariant around 1.74 V due to the operation of the LDO. The measurement could not be extended down below 1.0 KW/m² because the efficiency of DSSC that are used in this test is as low as 2.4% and can produce only small power.

The measured efficiency of MPPT (P_{pp}/P_{MPP}) is over 95% from 1.0 KW/m² to 1.5 KW/m². Fig. 15(c) depicts the MPPT efficiency of the system with and without PMU, respectively. Fig. 15(a) and (b) show the movements of operating points. The drastic increase in efficiency is indebted to the significant reduction of the power consumption by PMU circuit as predicted earlier.

When DSSCs are replaced with poly-Si cells, the

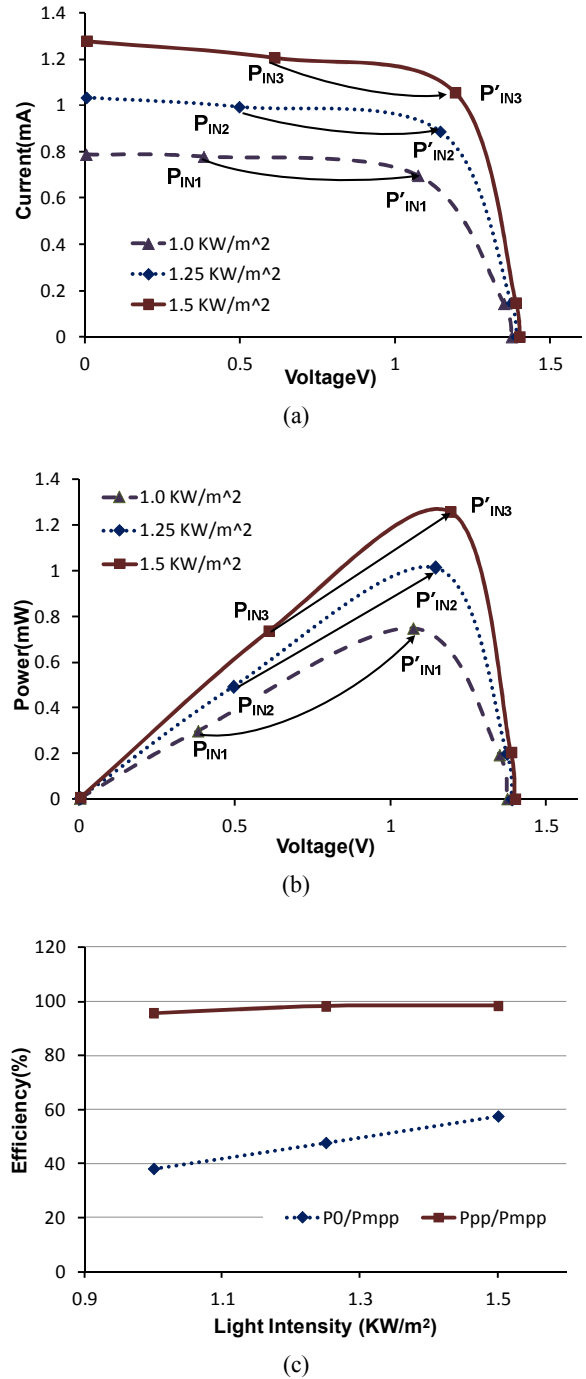


Fig. 15. (a) Output impedance adjustment for MPPT with DSSC I-V curves, (b) P-V curves, (c) efficiency of the MPPT.

MPPT is successfully accomplished by the PMU from 0.2 KW/m² to 1.5 KW/m². The measured MPPT efficiencies (P_{pp}/P_{MPP}) of the system with the proposed power management IC and poly-Si cells, range from 87% to 99% over 0.5~1.5 KW/m² intensity scan. The Fig. 16 shows the measurement results with poly-Si PV cell.

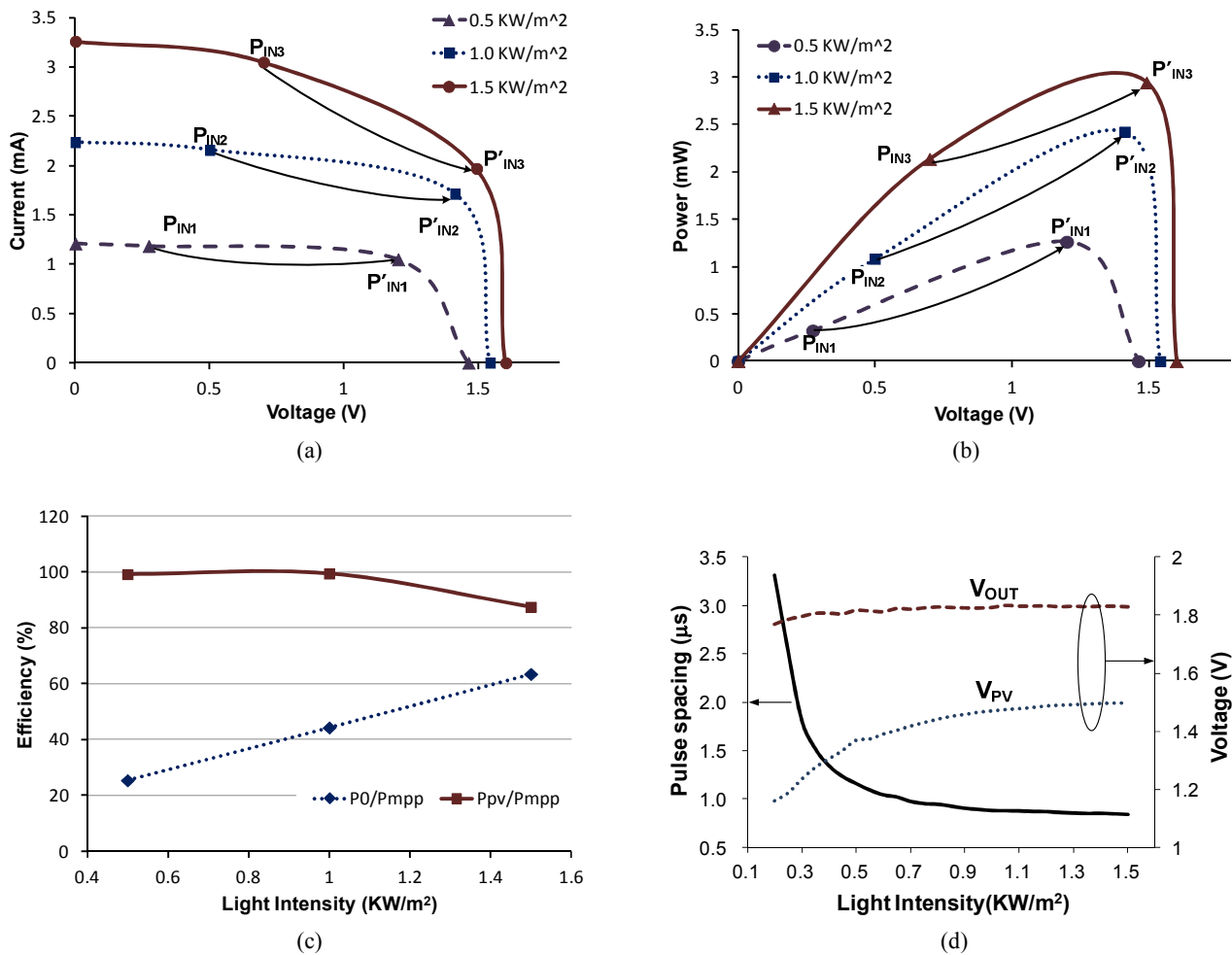


Fig. 16. (a) Output impedance adjustment for MPPT with poly-Si PV cell I-V curves, (b) P-V curves, (c) efficiency of the MPPT, (d) power pulse characteristics.

V. CONCLUSIONS

The proposed photovoltaic power management system provides MPP tracking to maximize the harvested energy from the DSSC, as well as stable power pulse trains for USN sensors. The LCO and charge pump adjust the input impedance of the PMU, that is the output impedance of the PV cell. The power delivery to the load is also regulated by the hysteresis comparator and LDO to guarantee power packets strong enough to complete the communication between USN sensor and transponder. An integrated circuit for the full power management system is fabricated using 0.13 μm CMOS technology and connected to the DSSC to demonstrate USN power supply performance. The power pulse of 6.5 nJ is stably delivered to the load of which the magnitude hardly dependent on the light intensity.

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REFERENCES

- [1] Prashant V. Kamat, "Meeting the Clean Energy Demand: Nanostructure Architectures for Solar Energy Conversion," *J. Phys. Chem. C*, vol.111, no.7, pp.2834-2860, Feb. 2007.
- [2] Giovanni Petrone, et al., "Reliability Issues in Photovoltaic Power Processing Systems," *IEEE*

- Trans. Industrial Electronics*, vol.55, no.7, pp.2569-2580, Jul., 2008.
- [3] Nicola Femia, et al., "Optimization of perturb and observe maximum power point tracking method," *IEEE Trans. Power Electronics*, vol.20, no.4, pp.963-973, Jul., 2005.
- [4] Trishan Eswam and Patrick L. Chapman, "Comparison of Photovoltaic Array Maximum Power Point Tracking Techniques," *IEEE Trans. Energy Conversion*, vol.22, no.2, pp.439-449, Jun., 2007.
- [5] Roberto Faranda and Sonia Leva, "Energy comparison of MPPT techniques for PV Systems," *WSEAS Trans on Power Systems*, vol.3, no.6, pp.446-455, Jun., 2008.
- [6] Chee Wei Tan, Tim C. Green, and Carlos A. Hernandez-Aramburo, "Analysis of perturb and observe maximum power point tracking algorithm for photovoltaic applications," *IEEE 2nd Power and Energy Conf.*, Dec., 2008. pp.237-242
- [7] Brett A. Warneke and Kristofer S.J. Pister., "An ultra-low energy microcontroller for smart dust wireless sensor networks," *IEEE Int'l Solid-State Circuits Conf.*, Feb., 2004. pp.316-317
- [8] Vijay Raghunathan, et al., "Design Considerations for Solar Energy Harvesting Wireless Embedded Systems," *Proceedings of the 4th Int'l Symposium on Information Processing in Sensor Networks (IPSN)*, Apr., 2005, pp. 457-462
- [9] Daniele Bari, et al., "Reliability Study of Ruthenium-Based Dye-Sensitized Solar Cells," *IEEE J. of Photovoltaics*, vol.2, no.1, pp.27-34, Jan., 2012
- [10] Yang-Hee Kim, et al., "Deposition of TiO₂ layers for dye-sensitized solar cells using nano-particle deposition system," *Current Applied Physics*, vol.11, no.1, pp.s122-s126, Jan., 2011.
- [11] Q. Yifeng, et al., "5 μ W-to-10mW Input Power Range Inductive Boost Converter for Indoor Photovoltaic Energy Harvesting with Integrated Maximum Power Point Tracking Algorithm," *IEEE ISSCC Tech. Dig.*, pp.118-119, Feb. 2011
- [12] Chun Yu Cheng, et al., "Design of a Low-Voltage CMOS Charge Pump," *IEEE 4th Int'l Symp. Electronic Design, Test and Applications on*, Jan., 2008, pp.342-345
- [13] M. Ferri, et al., "A 0.35- μ m CMOS Solar Energy Scavenger with Power Storage Management System," *Research in Microelectronics and Electronics (PRIME)*, Jul. 2009, pp.88-91
- [14] Jong-Min Baik, Jung-Hoon Chun, and Kee-Won Kwon, "A power efficient voltage up-converter for embedded EEPROM application," *IEEE Trans. Circuits and Systems II: Express Briefs*, vol.57, no.6, pp.435-439, Jun., 2010.
- [15] <http://www.abet-technologies.com/solar-simulators/sun-2000-class-a>



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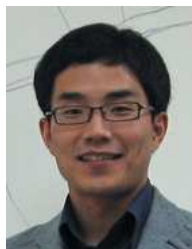
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