

Asymmetric Cascaded Multi-level Inverter: A Solution to Obtain High Number of Voltage Levels

M. R. Banaei[†] and E. Salary*

Abstract – Multilevel inverters produce a staircase output voltage from DC voltage sources. Requiring great number of semiconductor switches is main disadvantage of multilevel inverters. The multilevel inverters can be divided in two groups: symmetric and asymmetric converters. The asymmetric multilevel inverters provide a large number of output steps without increasing the number of DC voltage sources and components. In this paper, a novel topology for multilevel converters is proposed using cascaded sub-multilevel Cells. This sub-multilevel converters can produce five levels of voltage. Four algorithms for determining the DC voltage sources magnitudes have been presented. Finally, in order to verify the theoretical issues, simulation is presented.

Keywords: Voltage Levels, Asymmetric state, H-bridge cascaded.

1. Introduction

Multilevel inverters produce a stepped output phase voltage with a refined harmonic profile when compared to a two-level inverter [1, 2]. The concept of multilevel inverters, introduced about 30 years ago [1], entails performing power conversion in multiple voltage steps to obtain improved power quality, lower switching losses, better electromagnetic compatibility, and higher voltage capability. Nowadays, there exist three commercial topologies of multilevel voltage source inverters: the most popular being the diode-clamped [3, 4], flying capacitor [5, 6] and cascaded H-bridge [7-9] structures. Among these inverter topologies, cascaded multilevel inverter reaches the higher output voltage and power levels, and the higher reliability due to its modular topology and the simplicity [10].

Among these inverter topologies, the cascaded H-bridge multilevel inverters require the least number of total main components. One aspect which sets the cascaded H-bridge apart from other multilevel inverters is the capability of utilizing different DC voltages on the individual H-bridge cells which results in splitting the power conversion and asymmetrical multilevel inverters can be obtained [8, 9]. To provide a large number of output steps without increasing the number of DC voltage sources, asymmetric multilevel converters can be used. The cascaded H-bridge can operate as symmetric or asymmetric converter. In asymmetric multilevel converters the DC voltage sources are proposed to be chosen as different value according to different methods [11-13].

Recently, several multilevel inverter topologies have

been developed for cascaded multilevel inverters. Novel topologies of cascaded multilevel inverters using a reduced number of switches and gate driver circuits are presented in recent years [14-18]. In [14, 15] novel configuration of cascaded multilevel inverters have been proposed. The suggested topologies need fewer switches and gate driver circuits but they require multiple DC sources and some switches of suggested topologies have high peak inverse voltage. The proposed inverter in [14] can be used as symmetric and asymmetric converter and three algorithms for determination of magnitudes of DC voltage sources have been presented but in asymmetric converter it has some limitations. In asymmetric state to obtain uniform step voltage it can not be used from Trinary algorithm for determination of magnitudes of DC voltage sources. It can not perform difference operation among DC sources. In order to increase the steps in the output voltage, a new topology has been recommended in [17], which benefits from a series connection of sub-multilevel converters. In [18], the optimal structures for this topology are investigated for various objectives such as minimum number of switches and DC voltage sources and minimum standing voltage on the switches for producing the maximum output voltage levels [18]. These topologies require multiple DC sources and bi-directional switches. Although these topologies need a less number of bi-directional switches but need great number of IGBTs.

Operations of multilevel inverters depend on modulation strategies. There are several modulation strategies for multilevel inverters.

2. Presented Topology in [15]

Fig. 1 shows proposed structure in [15]. The basic unit for the multilevel converter presented in [15], is illustrated in Fig. 1. This consists of two DC voltage sources (with a

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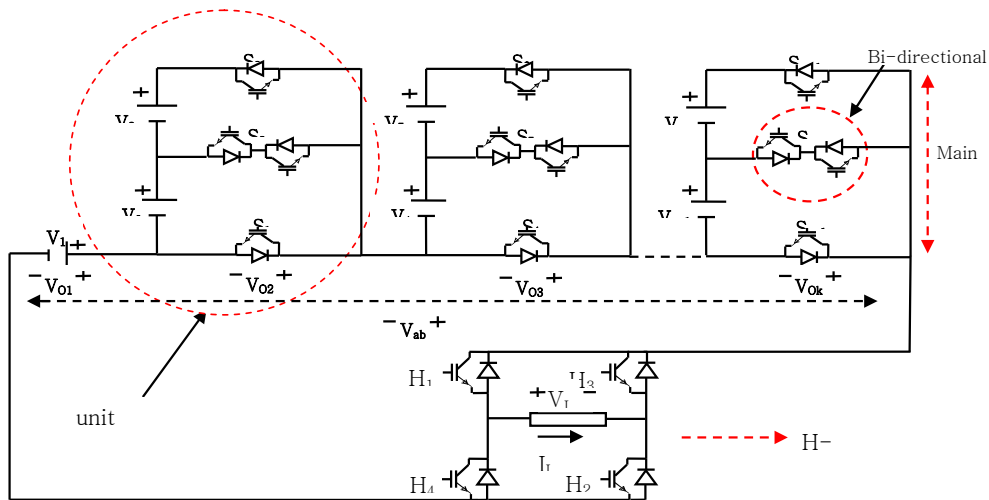


Fig. 1. Proposed structure in [15].

voltage equal to V_{dc} two unidirectional switches and a bidirectional switch. The basic unit shown in Fig. 1 can be extended. If n dc voltage sources are used in the extended unit as shown in Fig. 1, then the number of output voltage levels (S) and switches (N_{sw}) are given by the following equations, respectively [15]:

$$S = 2n + 1 \quad (1)$$

$$N_{sw} = \frac{3S + 7}{4} \quad n \text{ is odd} \quad (2)$$

$$N_{sw} = \frac{3S + 9}{4} \quad n \text{ is even} \quad (3)$$

The suggested topology [15] operates in symmetric state and some switches (H-bridge) of suggested topology have high peak inverse voltage.

3. Cascaded Sub-Multilevel Cells

If two switches are added to basic recommended unit in [15], a new sub-multilevel inverter is obtained. Fig. 2 shows the suggested sub-multilevel inverter. This consists of two DC voltages equal to V_1 and five switches. The main advantages of the proposed converter are doubling

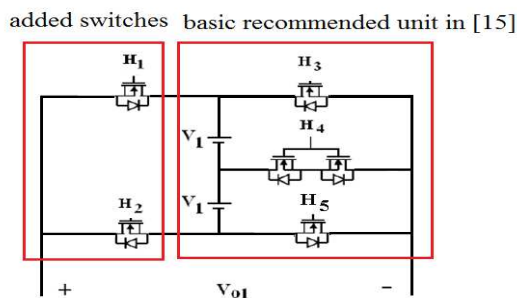


Fig. 2. Suggested sub-multilevel inverter.

the output voltage levels. Table 1 indicates the values of V_{O1} for states of switches. The sub-multilevel inverter can generate five voltage output levels.

Table 1. Values of V_{O1} for states of switches.

Level	ON switches
0	$H_2 H_5$ or $H_1 H_3$
V_1	$H_2 H_4$
$2V_1$	$H_2 H_3$
$-V_1$	$H_1 H_4$
$-2V_1$	$H_1 H_5$

This topology achieves reduction in the number of switches required, using only five switches while in any of the other three famous configurations (H-bridge cascaded, diode clamped and flying capacitor multilevel inverters) to generation of five levels eight switches are needed. The basic unit shown in Fig. 2 can be extended as shown in Fig. 3. Fig. 3 shows the circuit topology of the proposed inverter that is called Cascaded Sub-Multilevel Cells. DC voltage sources are independent each other, and value of them could be determined by different methods. In the other hand the Cascaded Sub-Multilevel Cells structure can operate as symmetric and asymmetric multilevel inverter.

The Cascaded Sub-Multilevel Cells requires unidirectional and bi-directional switches. The unidirectional switches have been made of common emitter anti-parallel MOSFET with diode. The bi-directional switches with capability of blocking voltage and conducting current in both directions are needed in Cascaded Sub-Multilevel Cells structure. There are several arrangement can be used to create such a bi-directional switch. The common drain anti-parallel MOSFET with diode pair arrangement shown in Fig. 1 has been used in this paper. This bi-directional switch arrangement consists of two diodes and two MOSFET. Each switch requires one gate driver. Each switch in the inverters requires an isolated driver circuit. The isolation

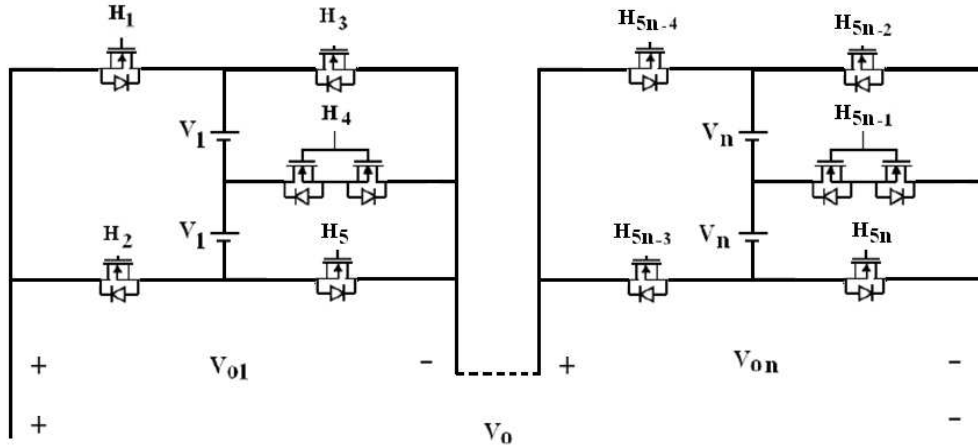


Fig. 3. Circuit topology of the proposed inverter.

can be given using either pulse transformers or opto-isolators [14]. The reliability of a multilevel inverter is proportional to the number of its components. Clamping diodes and balancing capacitors are not needed in the Cascaded Sub-Multilevel Cells. Another advantage of the Cascaded Sub-Multilevel Cells is circuit layout flexibility and modularized circuit layout and packaging is possible in it same as H-bridge cascaded topology. The number of output voltage levels can be easily adjusted by changing the number of sub-multilevel inverters.

4. Switching Algorithm

Several modulation strategies have been proposed for multilevel inverters. The modulation methods used in multilevel inverters can be classified according to switching frequency [19-25]. In this paper, the fundamental frequency switching technique has been used but in this paper calculation of optimal switching angles and minimizing total harmonic distortion (THD) is not the final goal. The advantageous of the fundamental frequency switching method is its low switching frequency compared to the other control methods [25]. The modulation of the

Cascaded Sub-Multilevel Cells is to choose a series of switching angles to combine separate elements into a single unit as desired sinusoidal voltage waveform. Fig. 4 shows a generalized quarter wave, symmetric, staircase voltage waveform synthesized by a $2s + 1$ level inverter, where s is the number of switching angles.

For uniform step waveform, the Fourier series expansion of the output voltage waveform using the fundamental frequency switching scheme shown in Fig. 5 is given by:

$$V_o(\omega t) = \sum_{p=1,3,\dots}^{\infty} \frac{4V_{dc}}{p\pi} (\cos(p\theta_1) + \cos(p\theta_2) + \dots + \cos(p\theta_s)) \sin(\omega t) \quad (4)$$

The switching angles can be found by solving the following equations:

$$\left. \begin{aligned} \cos(\theta_1) + \cos(\theta_2) + \dots + \cos(\theta_s) &= m \\ \cos(3\theta_1) + \cos(3\theta_2) + \dots + \cos(3\theta_s) &= 0 \\ &\vdots \\ \cos(p\theta_1) + \cos(p\theta_2) + \dots + \cos(p\theta_s) &= 0 \end{aligned} \right\} \quad (5)$$

where $m = \frac{\pi V_1}{4V_{dc}}$ and the modulation index m_a is given by

$m_a = m/s$. Here V_1 is magnitude of fundamental harmonic. For example, to control the fundamental amplitude and to eliminate harmonics in the five-level inverter, two nonlinear equations can be set up as follows:

$$\begin{aligned} \cos(\theta_1) + \cos(\theta_2) &= m \\ \cos(3\theta_1) + \cos(3\theta_2) &= 0 \end{aligned}$$

Different algorithm such as iterative method and artificial neural networks can be used to solving the set of nonlinear equation.

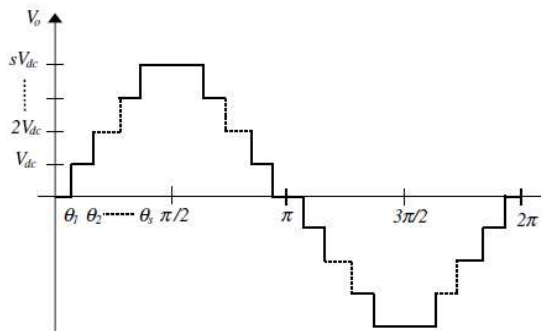


Fig. 4. A generalized quarter wave, symmetric, stepped voltage waveform.

In the simple method the switching angles can be found by solving the following equation:

$$\theta_s = \sin^{-1}\left(\frac{sV_{dc}}{V_{peak}}\right) \quad (6)$$

where V_{peak} is the peak value of the reference voltage. The frequency of output voltage is the same as frequency of sine reference wave. Fig. 5 show the basic concept of the conduction angle determination. In this figure half cycle of sine reference wave has been shown. Operation of five-level Cascaded Sub-Multilevel Cells is shown in Fig. 6. Modulation waveforms to switching are shown in Fig. 6(a). At each instant, the result of the comparison is decoded in order to generate the correct switching function corresponding to a given output voltage level. The switching pulses are shown in Fig. 6(b). In Fig. 6(b), Z indicates to zero level, P₁ and P₂ indicate to positive levels and N₁ and N₂ indicate to negative levels. Switching pulses

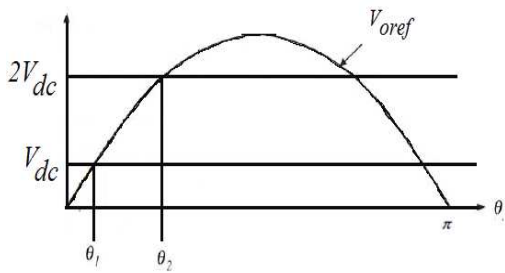


Fig. 5. Basic concept of the conduction angle determination.

produce input gate signals of switches that are shown in Fig. 6(c). The output voltage of this example is shown in Fig. 6(d).

5. Operational Principle of the Cascaded Sub-Multilevel Cells

The operational principle of the Cascaded Sub-Multilevel Cells is to generate five level output voltage by each sub-multilevel inverter.

The output phase voltage is obtained by summing the output voltage of sub-multilevel inverters as the following:

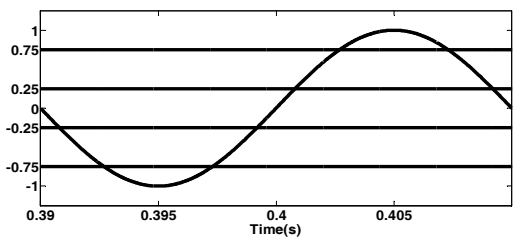
$$V_o = V_{o1} + V_{o2} + \dots + V_{on} \quad (7)$$

If all DC voltage sources in Fig. 1 are equal to $\frac{V_{dc}}{2}$

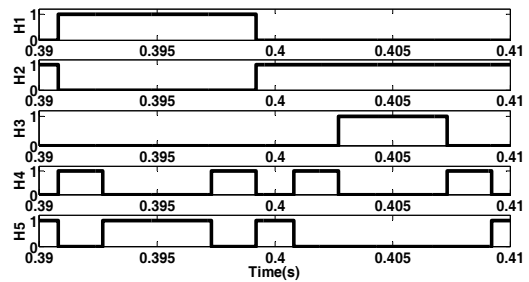
($V_1 = V_2 = \dots = V_n = \frac{V_{dc}}{2}$), the inverter is then known as symmetric multilevel inverter. The number of output voltage levels (S) in symmetric multilevel inverter may be related to the number of sub-multilevel inverters (n) by:

$$S = 4n + 1 \quad (8)$$

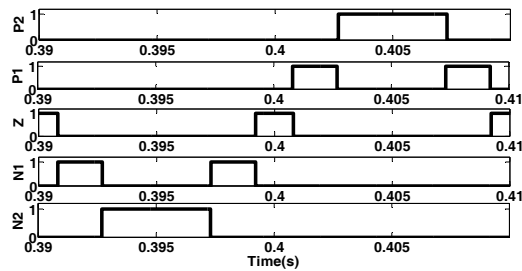
The maximum output voltage for this topology is obtained by summing the DC voltage sources and it (V_{Omax}) is:



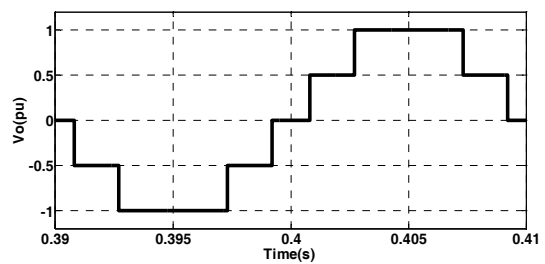
(a)



(c)



(b)



(d)

Fig. 6. Operation of five-level Cascaded Sub-Multilevel Cells topology (a) modulation signals (b) Switching pulses (c) gates signals (d) output phase voltage.

$$V_{O_{\max}} = n \frac{V_{dc}}{2} \quad (9)$$

To provide a large number of output levels without increasing the number of components, asymmetric multilevel inverters can be used. The DC voltage sources are proposed to be chosen according to a geometric progression with a factor of two (Binary) or three (Trinary) in cascaded H-bridge inverters [8, 11-14]. The Cascaded Sub-Multilevel Cells can be used as asymmetric multilevel inverters and Binary or Trinary methods can be used to choose value of DC voltage sources. In the following, we propose three methods for determination value of DC voltage sources for n cascaded sub-multilevel inverters. Existence of different algorithm to determine value of DC voltage sources gives flexibility to multilevel inverter and freedom action for designer.

In Binary and Trinary methods, the values of DC voltage sources are chosen according to the following equations:

$$V_i = (2^{i-1}) \frac{V_{dc}}{2}, \quad i = 1, 2, \dots, n \quad (10)$$

$$V_i = (3^{i-1}) \frac{V_{dc}}{2}, \quad i = 1, 2, \dots, n \quad (11)$$

In third method the DC voltage sources are suggested to be chosen according to the following algorithm:

$$V_i = (5^{i-1}) \frac{V_{dc}}{2}, \quad i = 1, 2, \dots, n \quad (12)$$

For n cascaded sub-multilevel inverters, the effective number of output voltage levels and maximum output voltages are given by Table 2. The total numbers of components needed in these four methods are totally different at higher voltage levels.

Fig. 7 shows an example of novel multilevel inverter that consists of two sub-multilevel inverters. If the suitable values for DC voltage sources are selected and proper switching are used, then output voltage levels between $+2(V_1+V_2)$ and $-2(V_1+V_2)$ can be obtained. These levels are:

$$0, \pm V_1, \pm V_2, \pm 2V_1, \pm 2V_2, \pm(V_1 \pm V_2), \pm(2V_1 \pm V_2), \pm(V_1 \pm 2V_2) \text{ and } \pm(2V_1 \pm 2V_2)$$

The maximum output voltage of this new topology is $2(V_1+V_2)$. The different modes of the Cascaded Sub-Multilevel Cells topology shown in Fig. 4 are demonstrated in Table 3. Note that different switching patterns for producing the zero level exist and in Table 3 only two patterns of them is shown. A current path to obtain $V_1 - 2V_2$ level has shown in Fig. 7.

Table 2. Output voltage levels and maximum output voltages.

	voltage levels	$V_{O_{\max}}$
Symmetric	$4n + 1$	$(2n) \frac{V_{dc}}{2}$
Binary	$2^{n+2} - 3$	$(2^{n+1} - 1) \frac{V_{dc}}{2}$
Trinary	$2(3^n - \frac{1}{2})$	$(3^n - 1) \frac{V_{dc}}{2}$
Third method	$5n$	$(\frac{5^n - 1}{2}) \frac{V_{dc}}{2}$

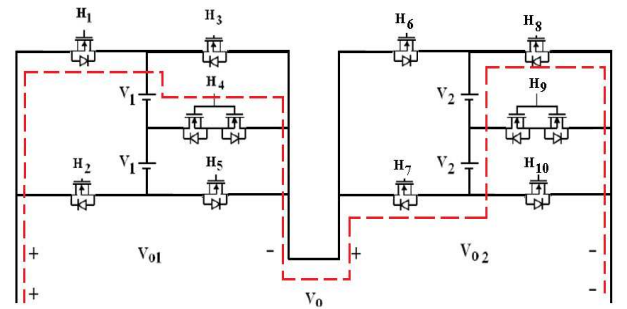


Fig. 7. Novel multilevel inverter with two sub-multilevel inverters.

Table 3. Different output voltage modes of Cascaded Sub-Multilevel Cells.

On Switches	V_o	On Switches	V_o
H ₂ H ₄ H ₆ H ₈	V_1	H ₁ H ₄ H ₇ H ₁₀	$-V_1$
H ₂ H ₃ H ₆ H ₈	$2V_1$	H ₁ H ₅ H ₇ H ₁₀	$-2V_1$
H ₁ H ₃ H ₇ H ₉	V_2	H ₂ H ₅ H ₆ H ₉	$-V_2$
H ₁ H ₃ H ₇ H ₈	$2V_2$	H ₂ H ₅ H ₆ H ₁₀	$-2V_2$
H ₂ H ₄ H ₇ H ₉	$V_1 + V_2$	H ₁ H ₄ H ₆ H ₉	$-V_1 - V_2$
H ₂ H ₄ H ₆ H ₉	$V_1 - V_2$	H ₁ H ₄ H ₇ H ₉	$-V_1 + V_2$
H ₂ H ₃ H ₇ H ₉	$2V_1 + V_2$	H ₁ H ₅ H ₆ H ₉	$-2V_1 - V_2$
H ₂ H ₃ H ₆ H ₉	$2V_1 - V_2$	H ₁ H ₅ H ₇ H ₉	$-2V_1 + V_2$
H ₂ H ₄ H ₇ H ₈	$V_1 + 2V_2$	H ₁ H ₄ H ₆ H ₁₀	$-V_1 - 2V_2$
H ₂ H ₄ H ₆ H ₁₀	$V_1 - 2V_2$	H ₁ H ₄ H ₇ H ₈	$-V_1 + 2V_2$
H ₂ H ₃ H ₇ H ₈	$2V_1 + 2V_2$	H ₁ H ₅ H ₆ H ₁₀	$-2V_1 - 2V_2$
H ₂ H ₃ H ₆ H ₁₀	$2V_1 - 2V_2$	H ₁ H ₅ H ₇ H ₈	$-2V_1 + 2V_2$
H ₁ H ₃ H ₆ H ₈	0	H ₂ H ₅ H ₇ H ₁₀	0

Depending on the availability of DC sources, the voltage levels are not limited to a specific ratio. By using DC sources with different value in any unit, more levels can be created in the output voltage, but this paper is focused on a general design principle of a uniform step multilevel inverter, with n series-connected sub-multilevel inverters per phase.

Although this topology requires multiple DC sources, it may be available in some systems such as photovoltaic panels, fuel cells and DC battery which can generate DC voltage sources.

6. Comparison Study

In comparison with the traditional two-level converters and by increasing the number of voltage levels, the small voltage levels to the generation of high power quality waveforms, lower harmonic components, lower voltage ratings of components, lower switching losses, reduction of dv/dt stresses on the load and gives the possibility of working with low speed semiconductor switches [28, 29]. The main disadvantage associated with the multilevel inverters is requiring a great number of semiconductor switches. Each switch in the inverter requires an isolated driver circuit. The isolated driver circuits need separate isolated power supply for each semiconductor switch. Hence the reliability of a multilevel inverter is proportional to the number of its components.

In comparison among the most popular multilevel inverters and Cascaded Sub-Multilevel Cells we can say: Clamping diodes are not required in the flying capacitor, cascaded H-bridge and Cascaded Sub-Multilevel Cells while balancing capacitors are not needed in the diode-clamped, cascaded H-bridge and Cascaded Sub-Multilevel Cells. Cascaded H-bridge and Cascaded Sub-Multilevel Cells requires multiple DC sources. Table 4 compares the main power component requirements per phase leg among these four multilevel inverters in symmetric state, where S is the number of voltage levels. In Table 4, the number of main switches needed by each inverter to achieve the same number of voltage levels is the same except for the Cascaded Sub-Multilevel Cells. The Cascaded Sub-Multilevel Cells thirteen-level inverter, for example, requires 15 main switches, while the other multilevel inverters need 24 switches.

Among the mature multilevel inverters, the cascaded H-bridge multilevel inverter requires the least number of components to achieve the same number of output voltage levels. With its modularized structure, it can flexibly expand the output power capability and is favorable to manufacturing so to probe the reduction in component numbers achieved by new configuration; comparison between cascaded topology and new multilevel in asymmetric state is shown.

Operation of Cascaded Sub-Multilevel Cells in asymmetric state is the same as cascade H-bridge inverter but in the cascade H-bridge one DC source exists in H-bridge unit while in the Cascaded Sub-Multilevel Cells two DC sources exist in sub-multilevel inverter. In the other hands one DC source divided two DC sources and sum of DC sources values in Cascaded Sub-Multilevel Cells is equal to one DC source value in cascade H-bridge inverter. Table 5 shows comparison of the number of switches (No. of sw) between Cascaded Sub-Multilevel Cells in this paper with the cascade H-bridge in asymmetric states for some cases in production S level voltage.

Another situation that requires a solution in inverters is the ratings of semiconductor switches. In other word,

voltage and current ratings of the switches in a multilevel inverter have important function on the cost and realization of the inverter. The currents of all switches are proportional with the rated current of the load but this is not the case for the voltage rating of the switches. In multilevel inverters the voltage rating of the switches or peak inverse voltage (PIV) of switches are proportional with the value of DC sources or DC buses and structure of inverter. To provide a large number of output levels without increasing the number of switches, asymmetric multilevel inverters can be used but the voltage rating of the switches is bigger than symmetric multilevel inverters when both groups produce same voltage value. In suggested sub-multilevel inverter that is shown in Fig. 2 two groups of switches exist.

PIV of unidirectional switches is the same as cascade H-bridge switches but PIV of bi-directional switches is half of other switches PIV. In comparison between cascade H-bridge and Cascaded Sub-Multilevel Cells, symmetric state is compared with symmetric state and asymmetric state with asymmetric state.

In the third algorithm to selection DC sources value the voltage rating of the switches is bigger than other states but asymmetric multilevel inverter with this algorithm can produce larger number of levels than other states.

Table 4. Comparison of power component requirement in symmetric state.

Inverter	Diode-clamped	Flying capacitor	Cascaded H-bridge	Cascaded Sub-Multilevel Cells
Main Switches	2(S-1)	2(S-1)	2(S-1)	$\frac{5(S-1)}{4}$
DC Source (DC bus)	S-1	S-1	$\frac{S-1}{2}$	$\frac{S-1}{2}$
Clamping Diode	2(S-1)	0	0	0
Balancing Capacitor	0	$\frac{(S-1)(S-2)}{2}$	0	0

Table 5. Comparison of main switches requirement between cascade H-bridge and Cascaded Sub-Multilevel Cells.

Binary				Trinary				Fifnary	
Cascaded		Cascaded Sub-Multilevel Cells		Cascaded		Cascaded Sub-Multilevel Cells		Cascaded Sub-Multilevel Cells	
S	No. of sw	S	No. of sw	S	No. of sw	S	No. of sw	S	No. of sw
7	8	13	10	9	8	17	10	25	10
15	12	29	15	27	12	53	15	125	15

Reduction of dv/dt stresses on the load is one of the advantageous of multilevel inverters. By using Cascaded Sub-Multilevel Cells the dv/dt stresses on the load is less than cascade H-bridge inverter because in the cascade H-bridge one DC source exists in H-bridge unit while in the Cascaded Sub-Multilevel Cells two DC sources exist in sub-multilevel inverter. In design inverter with 1000 V

maximum voltage when number of H-bridge cells in cascaded H-bridge and sub-multilevel inverters in Cascaded Sub-Multilevel Cells is the same, for example, cascaded H-bridge requires four DC sources with 250 V value and voltage steps is 250 V, while the Cascaded Sub-Multilevel Cells need eight DC sources with 125 V value and voltage steps is 125 V. So by using of Cascaded Sub-Multilevel Cells dv/dt stresses on the load is half of state that load is fed by cascade H-bridge. The two main components of the power losses in a switch are conduction losses and switching losses. Always, in each sub-multilevel inverter, a set of two switches is on at any given time. In design nine-level symmetrical multilevel inverters, for example, eight switches are on at any given time in cascaded H-bridge, while the Cascaded Sub-Multilevel Cells need four switches to generate one level so Cascaded Sub-Multilevel Cells has less on-state voltage drop and conduction losses of switches.

7. Simulation Results

In order to verify the validity of the proposed multilevel inverter in the generation of a desired output voltage, a prototype is simulated based on the suggested topology according to that one shown in Fig. 2 and 4. The MATLAB software has been used for simulation. The system parameters in simulation are listed in Table 6.

Table 6. Simulation study parameters.

	Nominal frequency	R-L Load	DC sources
values	50HZ	70 Ω , 55 mH	120V

6.1. Symmetric state

In the first simulation all DC voltage sources are the same. The magnitude of each voltage sources is considered 25 V ($V_1 = V_2 = \frac{V_{dc}}{2} = 25$ V). This structure generates nine voltage levels in each output phase. Table 7 shows the ON switches lookup table of nine-level multilevel inverter. It is important to note that there are different switching patterns for producing the voltage levels. Fig. 8(a) and 8(b) reveal the output voltage waveform and harmonic spectrum of load voltage, respectively.

Table 7. Look-up table of a single-phase nine-level inverter.

On Switches	V_o	On Switches	V_o
$H_2 H_4 H_6 H_8$	30	$H_1 H_4 H_7 H_{10}$	-30
$H_2 H_3 H_6 H_8$	60	$H_1 H_5 H_7 H_{10}$	-60
$H_2 H_3 H_7 H_9$	90	$H_1 H_5 H_6 H_9$	-90
$H_2 H_3 H_7 H_8$	120	$H_1 H_5 H_6 H_{10}$	-120
$H_1 H_3 H_6 H_8$	0	$H_2 H_5 H_7 H_{10}$	0

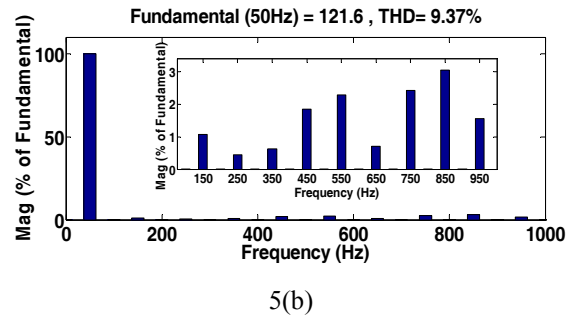
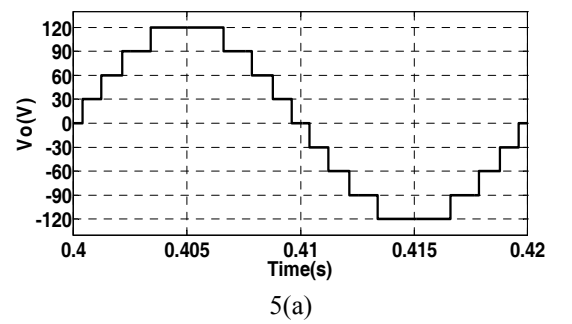


Fig. 8. Nine-level multilevel inverter: (a) output phase voltage; (b) harmonic spectrum of load voltage.

Another set of waveforms for a 9-level inverter are shown in Fig. 9. In this state, the switching angles are selected to eliminate or weak 3rd, 5th and 7th harmonics at $m_a=0.6125$. This figure shows ability of proposed converter in selective harmonic elimination.

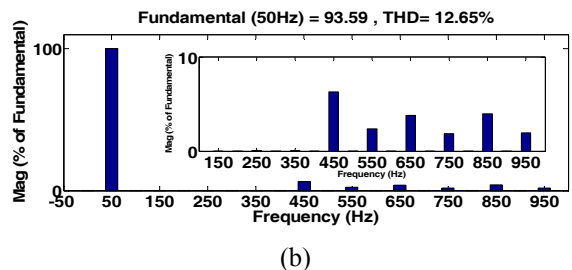
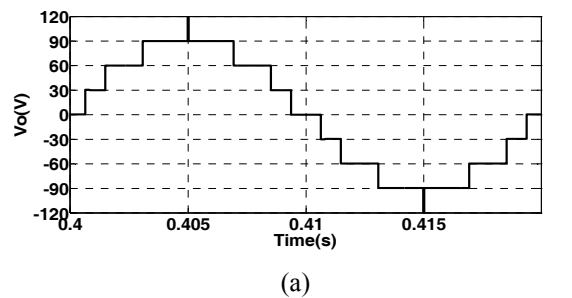


Fig. 9. (a) Output voltage, (b) corresponding FFT of 9 level inverter for 3rd, 5th and 7th harmonics elimination

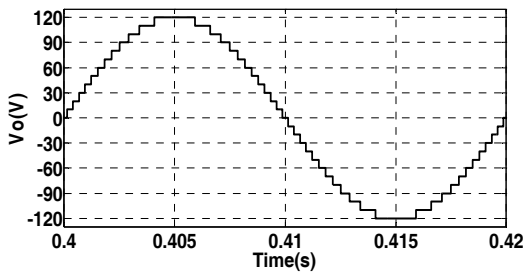
6.2. Asymmetric state

Fifnary algorithm is chosen to show Cascaded Sub-Multilevel Cells capability in operation at asymmetric

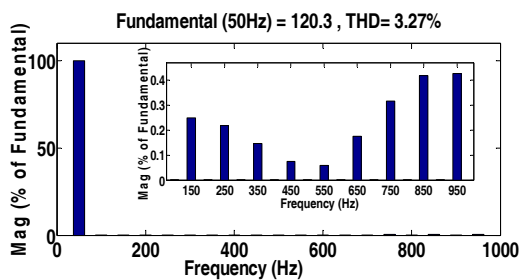
states. If the DC voltage sources in the Cascaded Sub-Multilevel Cells are chosen as $V_1 = 10\text{ V}$ and $V_2 = 50\text{ V}$, this circuit can generate twenty five level voltages. Table 8 shows the ON switches lookup table of twenty five-level multilevel inverter. The output voltage waveform and harmonic spectrum of load voltage are shown in Fig. 10(a) and 10(b), respectively.

Table 8. Look-up table of a single-phase twenty five-level inverter.

On Switches	$V_o(\text{V})$	On Switches	$V_o(\text{V})$
$H_2 H_4 H_6 H_8$	10	$H_1 H_4 H_7 H_{10}$	-10
$H_2 H_3 H_6 H_8$	20	$H_1 H_5 H_7 H_{10}$	-20
$H_1 H_3 H_7 H_9$	30	$H_2 H_5 H_6 H_9$	-30
$H_1 H_3 H_7 H_8$	40	$H_2 H_5 H_6 H_{10}$	-40
$H_2 H_4 H_7 H_9$	50	$H_1 H_4 H_6 H_9$	-50
$H_2 H_4 H_6 H_9$	60	$H_1 H_4 H_7 H_9$	-60
$H_2 H_3 H_7 H_9$	70	$H_1 H_5 H_6 H_9$	-70
$H_2 H_3 H_6 H_9$	80	$H_1 H_5 H_7 H_9$	-80
$H_2 H_4 H_7 H_8$	90	$H_1 H_4 H_6 H_{10}$	-90
$H_2 H_4 H_6 H_{10}$	100	$H_1 H_4 H_7 H_8$	-100
$H_2 H_3 H_7 H_8$	110	$H_1 H_5 H_6 H_{10}$	-110
$H_2 H_3 H_6 H_{10}$	120	$H_1 H_5 H_7 H_8$	-120
$H_1 H_3 H_6 H_8$	0	$H_2 H_5 H_7 H_{10}$	0



6(a)



6(b)

Fig. 10. Twenty five-level multilevel inverter (a) output phase voltage and (b) harmonic spectrum of load voltage.

The inverter can output twenty five-level voltages per phase with the fewest components. Total harmonic distortion (THD) of output voltage is as low as 5%. It can be observed from the harmonic spectrum of voltages that, presented topology is effective to meet low harmonic level.

8. Conclusions

Multilevel converters are very interesting for high voltage applications, energy conversion and considerably improve the output voltage quality. This paper has proposed a new topology of the cascaded converter called Cascaded Sub-Multilevel Cells. The main advantages of the Cascaded Sub-Multilevel Cells are:

- improve the output voltage quality
- reduced number of switching devices
- operates in symmetric an asymmetric states
- existence of different algorithms for calculating of magnitudes of DC voltage sources and freedom action to designer for design multilevel inverter
- small on-state voltage drop and conduction losses
- reduction of dv/dt stresses on the load

Four procedures for calculating of magnitudes of DC voltage sources have been presented. These procedures give freedom action to designer for design multilevel inverter. Comparison between the conventional topologies of multilevel inverters and the proposed multilevel inverter is shown in this paper and simulation results exhibit the good performance and feasibility of the proposed topology.

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