A 12-b Asynchronous SAR Type ADC for Bio Signal Detection

Shin-Il Lim*, Jin Woo Kim*, Kwang-Sub Yoon, and Sangmin Lee****

***Abstract*—This paper describes a low power asynchronous successive approximation register (SAR) type 12b analog-to-digital converter (ADC) for biomedical applications in a 0.35 μm CMOS technology. The digital-to-analog converter (DAC) uses a capacitive split-arrays consisting of 6-b main array, an attenuation capacitor C and a 5-b sub array for low power consumption and small die area. Moreover, splitting the MSB capacitor into sub-capacitors and an asynchronous SAR reduce power consumption. The measurement results show that the proposed ADC achieved the SNDR of 68.32 dB, the SFDR of 79 dB, and the ENOB (effective number of bits) of 11.05 bits. The measured INL and DNL were 1.9LSB and 1.5LSB, respectively. The power consumption including all the digital circuits is 6.7 μW at the sampling frequency of 100 KHz under 3.3 V supply voltage and the FoM (figure of merit) is 49 fJ/conversion-step.**

***Index Terms*—SAR type ADC, biomedical, split capacitor array, asynchronous control**

I. INTRODUCTION

The successive approximation register (SAR) type analog-to-digital converter (ADC) is widely used in autonomous sensor system and/or in portable sensory system for its low power consumption with a sampling rate ranging from a few KHz to tens of MHz [1-5]. Low power consumptions are caused by its simple hardware that requires only a comparator, a capacitor array and digital logic. N-step successive approximations for N-bit resolution make SAR type ADC suitable for the applications of low and medium signal bandwidth. Biomedical applications such as ECG (electro cardiogram) and EEG (electroencephalogram) generally employed a SAR type ADC for its low signal frequency with high accuracy. Especially in handheld or portable medical devices for EEG and ECG signal detection, the high resolution with low power SAR type ADC is highly required [2-4]. Since the SAR type ADC is generally implemented with the capacitor array, it requires large chip area, if it is implemented with direct binary weighted capacitor array in high resolution applications (>10 bits). This paper describes the 12-bit SAR type ADC for the hand-held or portable biomedical devices with low power consumption and small chip area. The 12-b SAR ADC with split capacitor array is proposed not only to reduce a layout area, but also to decrease power consumption, such that the proposed ADC is suitable for

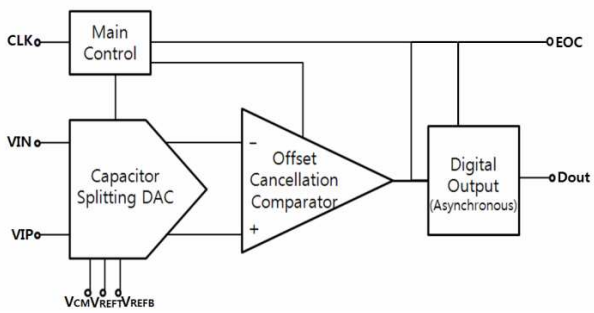

Fig. 1. Block diagram of 12-b SAR ADC.

Manuscript received Aug. 1. 2012; accepted Jan. 9, 2013.
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biomedical application such as ECG (electro cardiogram) and EEG (electroencephalogram). Fig. 1 shows the block diagram of the proposed 12-b SAR ADC. It has a capacitive split-array based DAC, an output-offset-cancelled comparator, a SAR and an asynchronous control block.

The details are in the following section. The architecture of the proposed DAC is described in Section II. Section III shows the circuit description and asynchronous control. The measurement results are presented in Section IV. The conclusion is drawn in Section V.

II. ARCHITECTURE OF THE PROPOSED DAC

Fig. 2 shows the DAC architecture in 12-bit ADC. The one input of DAC utilizes capacitive split-array consisting of 6-b main array, an attenuation capacitor C, and a 5-b sub array. The 6-b main capacitor array is sub-divided into two 5-b arrays as shown in Fig. 2 to reduce the switching power consumption [1]. The conversion requires 12 clock periods of the main clock; the first period is for the input sampling and next 11 periods are for remaining successive approximation cycles. During the input sampling, the MSB can be determined as in the reference [1-4]. Therefore, we need the 11-bit array of capacitors just for remaining 11-bit successive conversion, which means that the overall capacitors are reduced to one half compared to those of conventional direct implementation that requires 12 successive conversion steps excluding sampling periods. For example, if we use binary weighted capacitor array for 12-bit fully differential DAC as in the conventional way, we needs the total number of $2x2^{12}C$ capacitors, where C means unit size capacitor. But if the MSB decision technique is adopted during sampling, the total number of capacitors can be reduced down to $2x2^{11}C$ in fully differential DAC. The combinations of a 6-b main array, one attenuation capacitor and a 5-b sub array in one input of DAC need total number of 96C (63C+C+32C) capacitors, while 2x96C capacitors for fully differential DAC. This capacitor split-array with attenuation capacitor reduces the DAC area significantly.

However, this series connection of attenuation capacitor C to 5-b sub-array induces considerable mismatching voltage error. (Instead of the ideal attenuation capacitor value of 1.016C, we adopted C as the attenuation capacitor even it bears minor errors.) For the code of 'x00000011111', the worst-case inherent mismatching error voltage, V_{err}, can be calculated by the following Eq. (1).

$$V_{err} = \left(\frac{32}{2048}C - \frac{32/33}{63+32/33}C\right) \times \frac{(V_{reft} - V_{refb})}{2} \quad (1)$$

For the supply voltage of 3.3V (V_{reft} =3.3V and V_{refb} =0V), V_{err} is 770uV (0.96LSB). In case the code of 'x11111100000,' the absolute value of V_{err} is same but the sign is reversed. With the attenuation capacitor C rather than 1.016C, the worst-case inherent mismatching error voltage is estimated to 0.96LSB even though other circuits have no errors. The size of unit capacitor to 2C

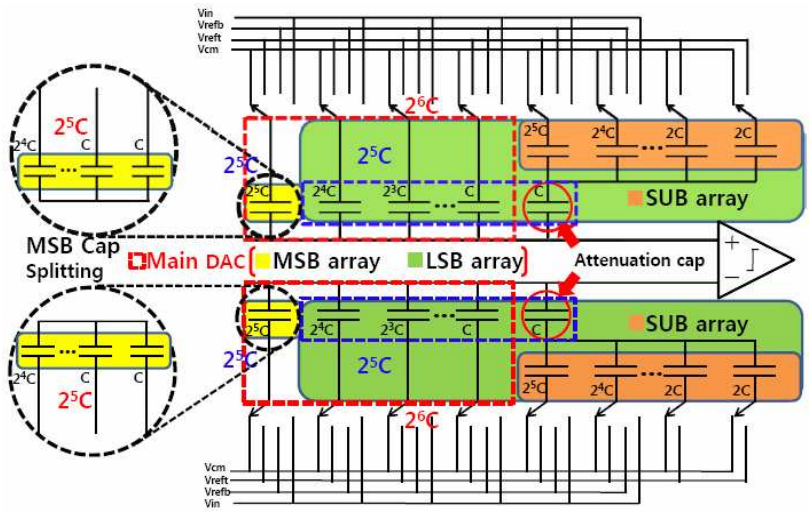

Fig. 2. Diagram of the proposed DAC architecture.

rather than C in 5-b sub-array reduces the worst case inherent mismatching error voltage. As for the same code of 'x00000011111' with the unit capacitor size of 2C, the worst-case inherent mismatching error voltage, V_{err}, also can be calculated by Eq. (2).

$$V_{err} = (\frac{32}{2048}C - \frac{64/65}{63+64/65}C) \times \frac{(V_{reft} - V_{refb})}{2} \quad (2)$$

With the same supply voltage of 3.3V (V_{reft} =3.3V and V_{refb} =0V), V_{err} is reduced to 391uV (0.48LSB) without calibration. Therefore we adopted 2C as an unit size capacitor in 5-b sub-array as shown in Fig. 2 and the total number of capacitors in fully differential DAC are 2x128C {2x(63C+C+64C)}. This increase in 64C capacitors for reducing nonlinearity errors does not affect the chip size severely.

The switching energy can be reduced with another split arrays of capacitors [1]. As an example, consider the 3-b MSB (4C) capacitor subdivided into two 2-b sub-array (2C+C+C) as shown in the left side of Fig. 3 and the capacitor switching process from 2nd compare to 3rd compare just after the decision of MSB in 1st compare process (not shown in this Fig. 3). When the code is changed from '100' to '010' (down conversion to lower side) during the successive approximation process, only 2Cs in the left 2-b sub-array are switched in this split capacitor array architecture, while 6Cs (4Cs and 2Cs) are switched in conventional binary weighted capacitor array architecture. Small numbers of capacitors are switched in this split capacitor array architecture. This small numbers of switching capacitors produce less switching energy consumption. This concept was applied and extended to the proposed 12-bit ADC to reduce the total switching power consumption. By splitting the MSB capacitor into sub-capacitors, the switching energy can be reduced by at least 37% compared to that of conventional binary weighted capacitor array architecture [1].

III. Asynchronous Control and Comparator

1. Asynchronous Control

The operation of the proposed SAR is based on the asynchronous control. All the registers are not clocked concurrently in this asynchronous control. Since this asynchronous control is caused by event driven control sequences, we can reduce digital power consumption. In synchronous ADC, we have three steps for one bit decision: new bit set in DAC, comparison, and final results determination and storage. These three steps are processed with sub-divided (oversampled) clocks in synchronous system. But in this asynchronous system, three steps are consecutively processed with the event of self-synchronization process as illustrated in Fig. 4 [3]. The self-synchronization of the ADC is initiated by the start-signal to activate comparator in the first step (1). Step control unit ignites the set signal to DAC control

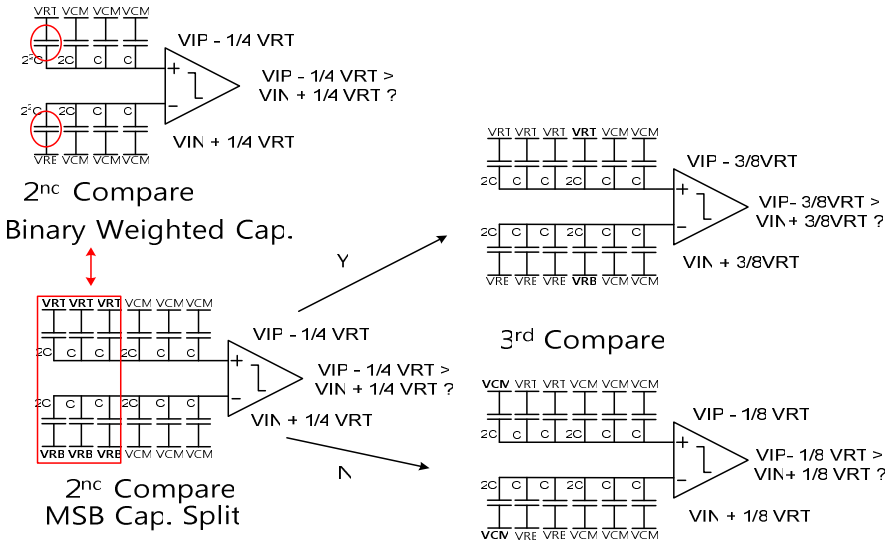

Fig. 3. Switching with the capacitor split of MSB.

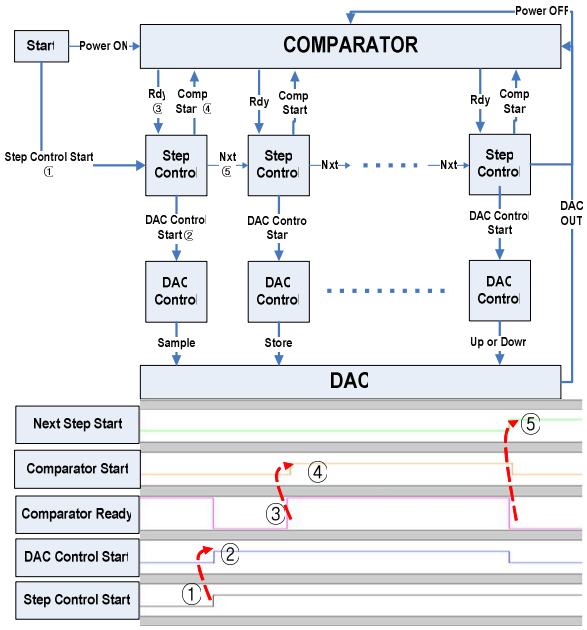

Fig. 4. Asynchronous control process.

unit which sends a sample signal to the DAC in the second step (2). The MSB output of the DAC drives comparator. Comparator sends current state to the step control unit. If the current state of comparator is in reset mode, the step control block sends a start signal to the comparator in the fourth step (4). If the comparator stays active, the step control unit proceeds to the next step (5). After finishing the SAR algorithm, the comparator and the step control unit stop their operation until a next start signal appears. This asynchronous control can be implemented with asynchronous dynamic CMOS logic instead of standard CMOS logic [3]. Delay circuits are also required during asynchronous operations. This delay circuits are easily implemented by using the series of inverters that have long length transistors and small loading capacitors.

2. Comparator

The dynamic latched comparator with output offset cancellation is exploited to prevent degradations from the DAC capacitor array and pre amplifier. Fig. 5 shows the architecture of the output offset cancelled comparator. It consists of two pre amplifiers, capacitors and a latch. To improve the accuracy, 2-stage amplifier was used and to remove the offset of the pre amplifier, the output offset storage method is employed.

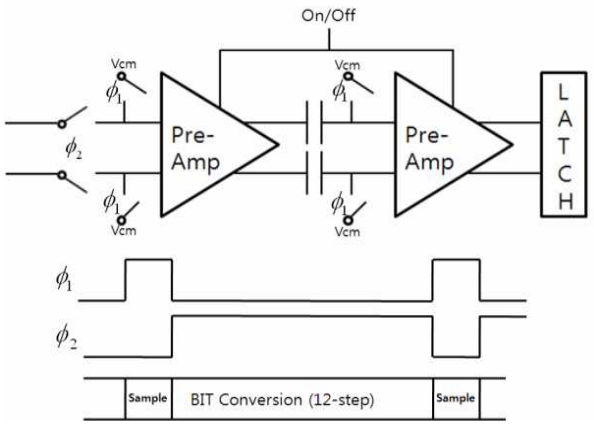

Fig. 5. Block diagram of comparator.

The circuit diagram of the pre-amplifier1 and pre-amplifier2 is shown in Fig. 6(a) while that of the dynamic latch is shown in Fig. 6(b). The gain of pre amplifier is 18dB. Both the clock rate and supply voltage have effects on power consumption. We used the double-tail latch type comparator as shown in Fig. 6(b) [7]. During the reset (CLK=0V), the D+ and D- nodes are pre-charged to VDD. And this in turn discharged output nodes to ground. If the CLK becomes high (VDD), tail current is supplied to the input transistors and input dependent differential voltages are generated at the D+ and D- nodes. This in turn produces output voltages (OUT+, OUT-) through the three transistors that were connected to the D+ and D- nodes. These three transistors connected to the D+ and D- nodes provide additional gain to the cross-coupled inverters with less kick back noises and hence provide improved sensitivity with low power consumption.

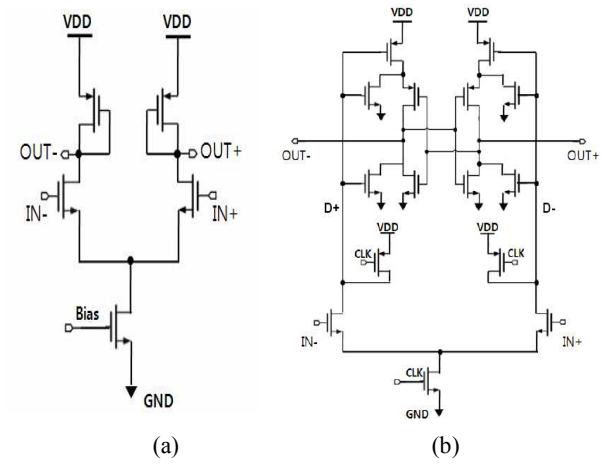

Fig. 6. Circuits of comparator (a) preamp, (b) latch.

IV. Measurement Results

The chip was implemented and fabricated with a 0.35 μm CMOS technology. The core area, as shown in Fig. 7, is 947 μm×756 μm excluding pads. The test setup with Analog Device's capture board and device under test (DUT) is demonstrated in Fig. 8. The measured spectral results with the 4 KHz input signal are shown in Fig. 9 at the sampling rate of 99 KHz. The measurement result illustrates that the proposed ADC achieves the SNDR of 68.32 dB, the SFDR of 79dB and the ENOB (effective number of bits) of 11.05 bits. The DNL and INL are measured to be 1.5/-0.9 LSBs and 1.9/-1.3 LSBs, respectively, as shown in Fig. 10. The INL which becomes more than +/- 1LSB is due to the inaccuracy of attenuation capacitor C. The power consumption including all the digital circuits is 6.8 μW at the sampling frequency of 99 KHz under the supply voltage of 3.3V. Therefore the resultant FoM (Figure of Merit) is 49 fJ/conversion-step. The measured performance is summarized in Table 1.

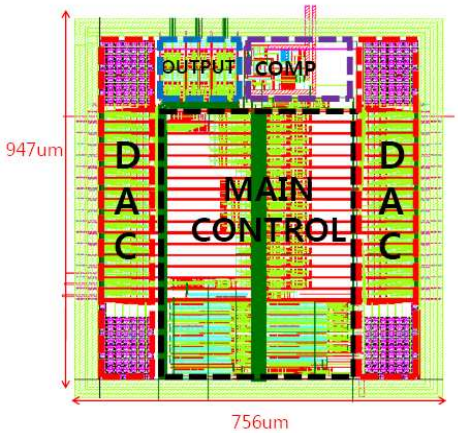

Fig. 7. Chip layout.

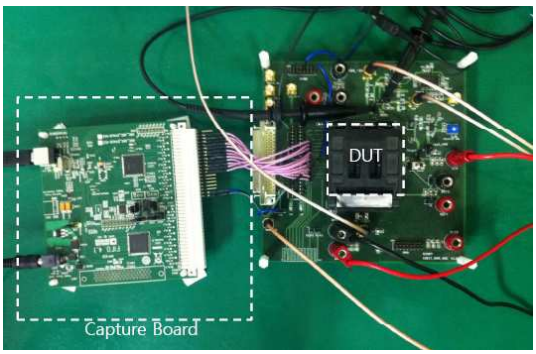

Fig. 8. DUT and test setup.

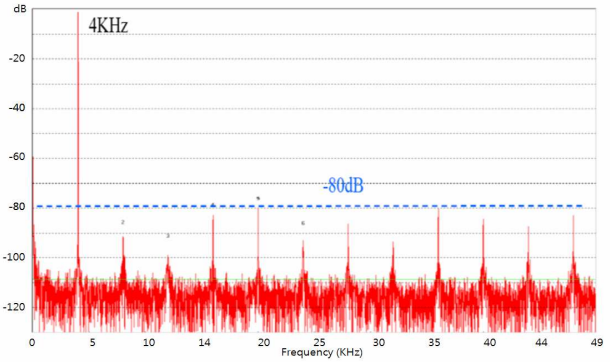

Fig. 9. FFT measured results.

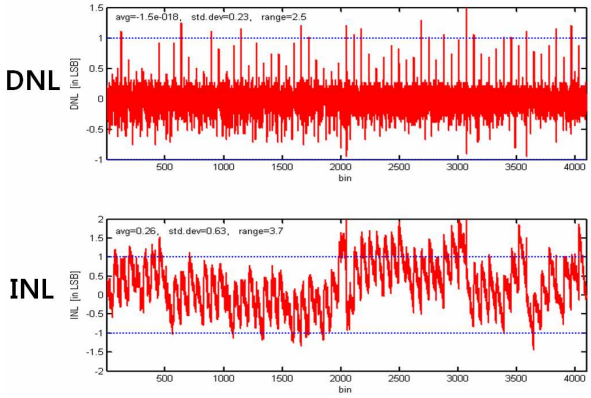

Fig. 10. The measured DNL and INL.

Table 1. Performance summary (measurements)

Technology	Magna 0.35㎛ CMOS
Resolution	12 Bit
Power Supply	3.3 V
Sampling Rate	99KHz
Input Signal Full Scale	3.3 V_{pp_diff}
Power Consumptions	6.73㎼ Digital = 5.53㎼, Analog = 1.20㎼
SNDR, SFDR	68.32dB , 79dB
ENOB	11.05 b
FOM	49fJ/conversion step
Layout	947㎛*756㎛

V. Conclusions

The 12-b SAR CMOS ADC with asynchronous control was implemented for biomedical applications. The asynchronous control and MSB splitting array techniques allowed the proposed ADC to lower power consumption. In order to reduce switching power dissipation, two 5-b sub-capacitor arrays in 6b MSB array were employed.

The latched comparator with the offset cancellation was used to maintain the high accuracy of the DAC.

ACKNOWLEDGMENTS

This work was partially supported by Key Research Institute Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2010-0020163) and also partially supported by the MKE (The Ministry of Knowledge Economy), Korea, under the ITRC (Information Technology Research Center) support program supervised by the NIPA (National IT Industry Promotion Agency (NIPA-2013-(H0301-13-1013)).

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