Electromagnetic Susceptibility Analysis of I/O Buffers Using the Bulk Current Injection Method

SangKeun Kwak, Wansoo Nah, and SoYoung Kim

***Abstract*—In this paper, we present a set of methodologies to model the electromagnetic susceptibility (EMS) testing of I/O buffers for mobile system memory based on the bulk current injection (BCI) method. An efficient equivalent circuit model is developed for the current injection probe, line impedance stabilization network (LISN), printed circuit board (PCB), and package. The simulation results show good correlation with the measurements and thus, the work presented here will enable electromagnetic susceptibility analysis at the integrated circuit (IC) design stage.**

***Index Terms*—I/O buffer, bulk current injection (BCI), electromagnetic compatibility (EMC), electromagnetic susceptibility (EMS), injection probe, on-chip power grid, on-chip decoupling capacitor**

I. INTRODUCTION

As mobile systems that use multi-chip package (MCP) and system in package (SiP) technologies have become faster and more complex, many electromagnetic compatibility (EMC) issues have been encountered. In the presence of electromagnetic disturbances, cables or printed circuit boards in electronic systems can act as receiving antennas. Due to this electromagnetic interference (EMI), digital or analog circuits can malfunction or be permanently damaged. These electromagnetic susceptibility (EMS) issues can cause redesign of integrated circuits [1].

IC manufacturers and customers use standardized measurement methods to characterize the EMS or immunity of ICs during the product characterization stage. The immunity test method for ICs is well defined by the Institution of Engineering and Technology (IET) electrical measurement handbook [2] and the ISO 11452-4 standard [3]. These references have been applied to the EMC testing of automotive ICs. Recently, the criteria of automotive EMC test methods have been modified so as to develop EMC testing schemes for general purpose ICs [4, 5]. Immunity test procedures may be classified as bulk current injection, direct power injection, or field coupled methods [6]. Bulk current injection (BCI) test is a standard IC immunity test scheme by injecting magnetically induced current to IC package pin, and direct power injection (DPI) is by injecting RF interference through a capacitors. Both schemes are widely used for conducted susceptibility testing of electronic systems. The DPI testing and simulation results of PLL is reported in [7]. The BCI testing results and test setup modelling of general purpose IC are reported in [8]. But in this work, IC is simply modelled as passive network by extracting *S*-parameters of inactive circuit.

In IEC 62132-3, the BCI test setup requires an RF generator, a current injection probe, a line impedance stabilization network (LISN), a printed circuit board (PCB), and an IC [5]. A simplied conceptual diagram of BCI test is shown in Fig. 1. A current injection probe with a ferrite-core behaves as an RF transformer, where the secondary winding is the cable or wire under the probe. A simplified version of the injection probe model

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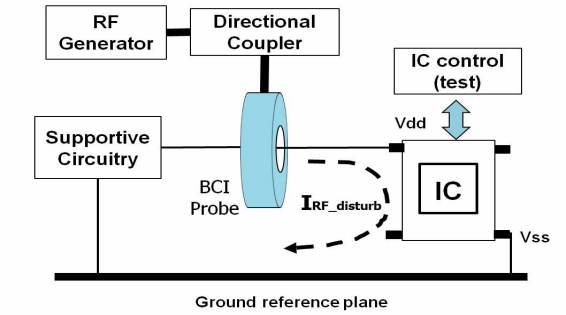


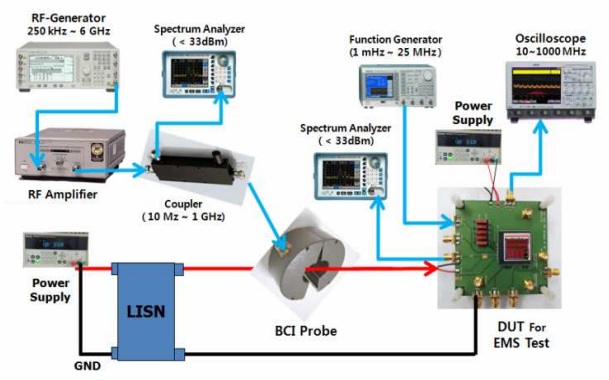
Fig. 1. Concept of BCI test of an IC [5].

was proposed in [9]. Specifically, a mutual coupling model valid in the low-frequency range was examined. Further research has been conducted to model the frequency-dependent permeability and loss of the ferrite core [10, 11]. The developed models are well suited for frequency domain analysis. However, IC design and performance evaluations are usually performed in the time domain. Other BCI test setup components, such as the LISN and PCBs, show frequency dependent behavior. EMS investigations are usually performed during the product characterization stage, but if the SPICE simulation models are available for time domain simulations, IC immunity can be evaluated during the IC design [12, 13].

This paper focuses on modeling of BCI test components for susceptibility simulation of ICs and the characterization of BCI test result of I/O buffers. This paper is organized as follows. Section II describes the experimental setup for susceptibility test of an IC using the BCI method. The I/O buffer failure criteria and the susceptibility test flows are discussed in Section III. Section IV presents the development process of the equivalent circuit models for the BCI test components. In Section V, the BCI simulation results of the I/O buffer circuits based on the proposed models are compared with measurement results. Finally, conclusions are given in Section VI.

II. Bulk Current Injection Experimental Setup

BCI test setup shown in Fig. 2(a) is based on the current IEC standard proposal for IEC 62132-3 [5]. The test setup includes the RF generator and amplifier to inject certain amount of RF power to the BCI probe. The



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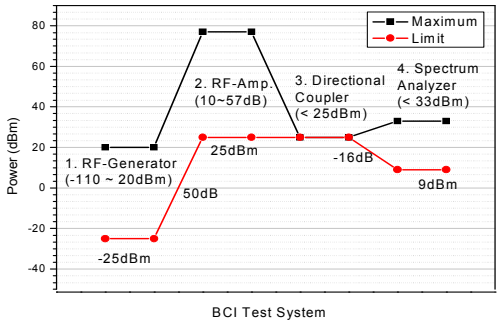


(b)

Fig. 2. The components of the BCI test (a) The system model for BCI testing of the I/O buffer chip, (b) the power limit defined for each step of the BCI test.

directional coupler is used to divide the power, so that the reduced portion of the injected power can be monitored using the spectrum analyzer. LISN is needed to block the BCI current from damaging the DC power supply. The operating power ranges allowed for RF-generator, RF-amplifier, directional coupler, and spectrum analyzer are shown in Fig. 2(b). The maximum allowed power limit is small in directional coupling and spectrum analyzer, so in order to prevent damage, the power limit should be predicted in the RF-generator and RF-amplifier. If the maximum allowed power of the directional coupler is 25 dBm, with the 50 dB gain of RF-amplifier, the power of the RF-generator cannot exceed -25 dBm.

III. Susceptibility Criteria and Test Flow

In the BCI test of I/O buffers, it is assumed that the design under test (DUT) is only perturbed by a sinusoidal RF noise current applied to the Vdd pin. The power

applied to BCI probe to produce RF noise is generated from an RF generator in the frequency range 10 MHz – 1 GHz, and up to 20 dBm forward power. The IC used for the susceptibility testing is 1.8 V I/O buffer. As susceptibility criteria of the testing of this circuit, Vdd fluctuation of 6% or 11% as shown in Fig. 3 is used. This criterion is defined by the requirement to settle only for external observations of the ICs and from the functional tolerances related to their use in the applications [14].

The flow chart of the immunity test is shown in Fig. 4. The RF generator frequency is increased from the starting frequency of 10 MHz up to 1 GHz. For each frequency, the amplitude of the RF generator is increased linearly until the susceptibility criteria, Vdd fluctuation of 6% or 11%, is reached [6]. The power of the RF-generator is recorded as the forward power at that frequency. The forward power is used as a measure of EMI immunity of ICs. Higher forward power means higher immunity and less susceptibility.

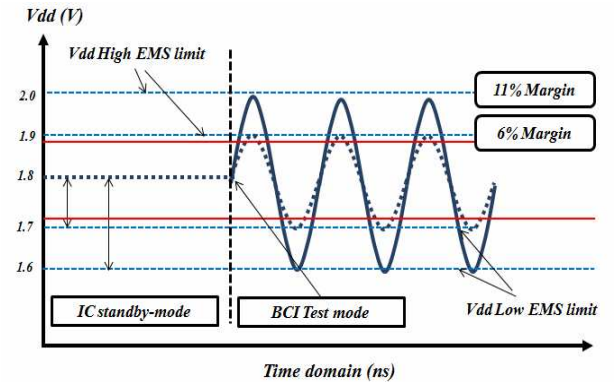


Fig. 3. Susceptibility criteria of 1.8 V I/O buffer for the BCI test.

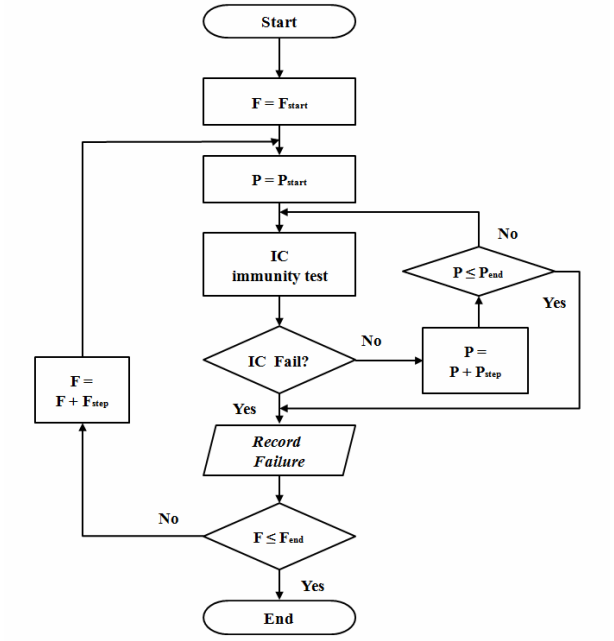


Fig. 4. Flow chart of the IC susceptibility test procedure.

IV. Simulation Model Development for BCI Test of IC

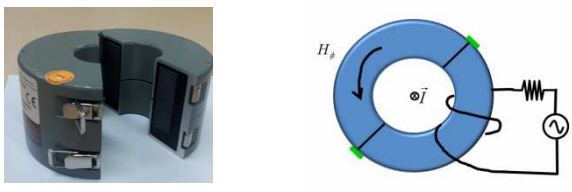
In this section, equivalent circuit models are developed for major components of the BCI test, BCI probe, LISN, PCB, package and IC. The proposed models will enable transient SPICE simulation of the BCI test to predict the electromagnetic susceptibility of IC.

1. Modeling of the Current Injection Probe

The equivalent circuit model of the BCI probe is developed based on the probe geometry and the measurement results of the two-port *S*-parameter over the valid frequency range of the BCI test. A current probe is constructed from a core of ferrite material that is separated into two halves, which are joined by a hinge and closed with a clip as shown in Fig. 5(a). The ferrite core is used to concentrate the magnetic flux as shown in Fig. 5(b). Its permeability has frequency dependent real and imaginary parts as in (1) [10, 15].

$$\mu_r = \mu_r'(f) - j\mu_r''(f). \tag{1}$$

When a RF-power is applied at port-1 of the BCI probe, as illustrated in Fig. 6, the conduction current and displacement current are induced, and a magnetic field is formed near the ferrite core cylinder. Thus the formed magnetic field can induce current when a conductor loop passes through the center of the BCI probe from port-2 to port-3.



(a) (b)

Fig. 5. The BCI probe (a) A photograph of BCI probe (F-140), (b) example of the current injection using the BCI probe.

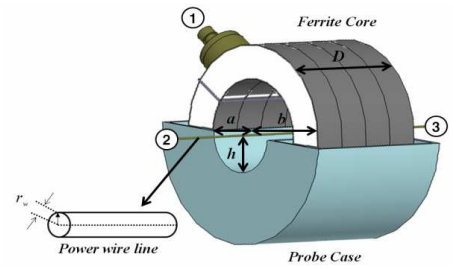
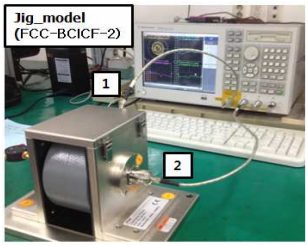


Fig. 6. Schematic model of the BCI probe with the dimensions shown.



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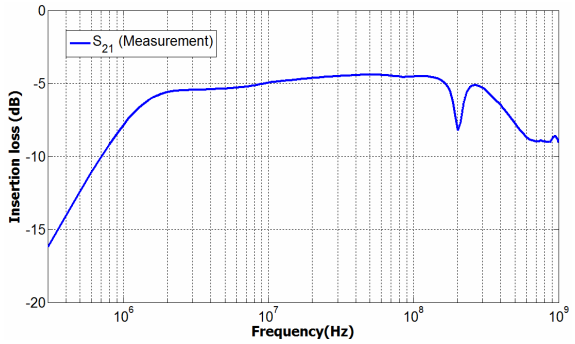

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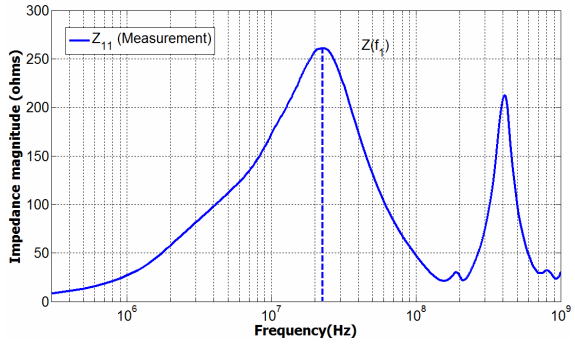


(c)

Fig. 7. The measurement results for the BCI probe using the calibration kit (a) Measurement of the BCI probe with a calibration kit, (b) The insertion loss S_{21}, (c) the impedance Z_{11}.

The calibration kit of the BCI probe is used to measure the reference *S*-parameter using a vector network analyzer (VNA) as shown in Fig. 7(a). The *S*-parameters are measured between port-2 and port-1 of the BCI probe with port-3 terminated with 50 ohms matching condition. Based on the *S*-parameters, impedance parameters are derived using the following relation with Z_0 of 50 ohm [16].

$$Z_{11} = Z_0 \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}, \quad (2)$$

$$Z_{12} = Z_0 \frac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}. \quad (3)$$

S_{21} and Z_{11} data shown in Fig. 7(b) and (c) are used to derive the equivalent circuit for BCI probe. Fig. 8 shows the proposed equivalent circuit model for the BCI probe. Some of the model parameters are determined by the physical dimensions of the BCI probe and the power line passing through the probe, and others are chosen to fit the measurement results.

The self inductance (L_0) value of the BCI probe is calculated using the physical dimensions shown in Fig. 6. An equation for estimating the self-inductance is given by

$$L_0 = \frac{\mu_0 \mu_r \times D \times n^2}{2\pi} \ln\frac{b}{a}[H], \quad (4)$$

where n is the number of turns of the primary winding, μ_0 is the free-space permeability, μ_r is the effective complex permeability, D is the thickness of the toroidal core, a is the internal radius of the toroidal core, and b is the external radius of the toroidal core, respectively [10].

The self inductance (L_1) and the stray capacitance (C_1) of the power line passing through the BCI probe are modeled as half the capacitance of the coaxial transmission line formed by a portion of the power wire

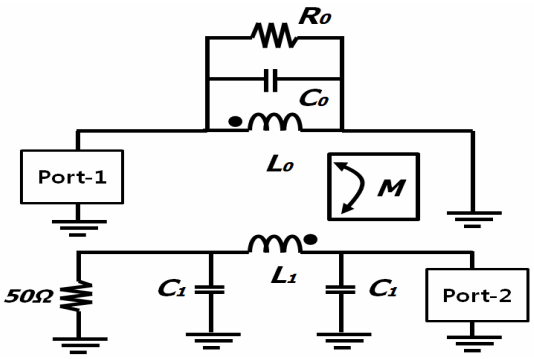


Fig. 8. The proposed equivalent circuit model of the BCI probe.

line and the inner surface of the probe frame [10].

$$L_1 = \frac{\mu_0}{2\pi}\left[\ln\left(\frac{2h}{r_w}\right)\right][H/m], \quad (5)$$

$$C_1 \cong \frac{2\pi\varepsilon_0}{\ln(2h/r_w)}[C/m], \quad (6)$$

where ε_0 is the free-space permittivity, r_w is the radius of the power wire line, and h is the distance between the power wire line and the inner surface of the probe frame.

The expression for Z_{11} for simplified equivalent circuit model for the probe in Fig. 8 is derived as follows.

$$Z_{11}(\omega) = \frac{j\omega R_0 L_T}{j\omega L_T + R_0 - \omega^2 C_0 R_0 L_T}, \quad (7)$$

where

$$L_T = L_0 + \frac{M^2}{L_1 + 2C_1}, \quad (8)$$

$$M = k\sqrt{L_0 L_1}. \quad (9)$$

In [10], the mutual inductance M is expressed in a closed form. However, in this paper, the mutual coupling factor, k, of Eq. (9) is determined to be 0.94 to fit measured S_{21} in Fig. 7(b).

The magnitude of $Z_{11}(\omega)$ becomes maximum at

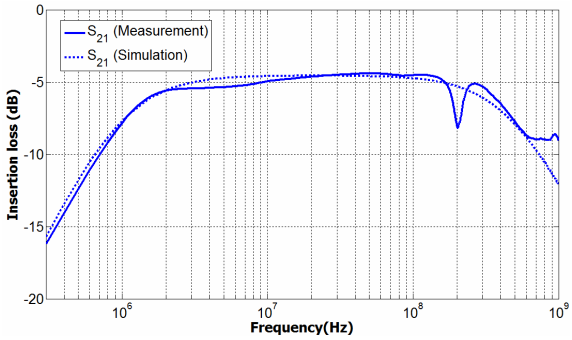
$$\omega_0 = \frac{1}{\sqrt{L_T C_0}}. \quad (10)$$

From Z_{11} measurement results of port-1 shown in Fig. 7(c), the anti-resonance frequency (ω_0) of the BCI probe is 20 MHz. From ω_0, the capacitance (C_0) of the BCI probe is calculated.

$$C_0 = \frac{1}{\omega_0^2 L_T}. \quad (11)$$

From Eq. (7), the magnitude of $Z_{11}(\omega)$ at the anti-resonance frequency (ω_0) is R_0, so it can be determined from the measured data shown in Fig. 7(c).

$$Z_{11}(\omega_0) = R_0. \quad (12)$$



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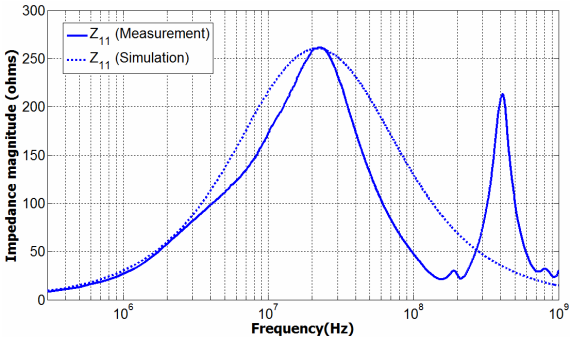


(b)

Fig. 9. Comparison of the measurement and simulation results from the proposed model of the BCI probe from Fig. 7 (a) The insertion loss (S_{21}) results, (b) the input impedance Z_{11} results.

The S_{21} and Z_{11} from the proposed model and measurement are compared in Fig. 9. By adding additional segments in the BCI circuit model, the second resonance peak of Z_{11} can be matched, however it does not help the accuracy of the overall BCI test prediction. Since the insertion loss (S_{21}) is significantly small in that frequency range, the injection noise does not reach the test IC.

2. PCB Design and Modeling

The magnetically induced current generated on the wire from the BCI probe is injected to IC through cable, connecter, PCB, and package. In this section, the design details of the PCB that enables the BCI test, and the development of the equivalent circuit model will be presented. The BCI current is injected through port-1 and the IC Vdd fluctuation is monitored through an oscilloscope connected at port-2 as shown in Fig. 10. Only certain portion of the power generated from the RF generator will arrive at the PCB-package-IC. The PCB fabricated for the BCI test is based on four layers, and

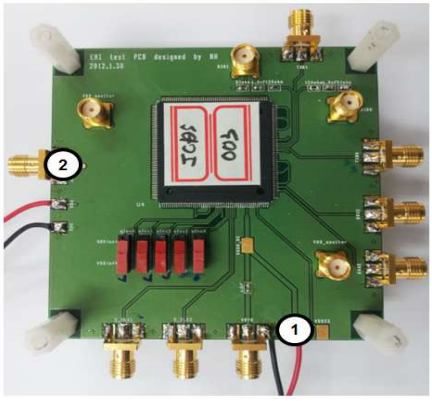
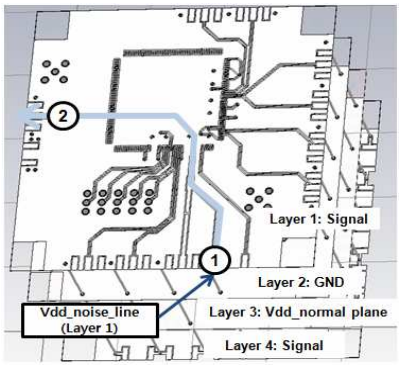


Fig. 10. A photograph of the PCB used in the EMS test.



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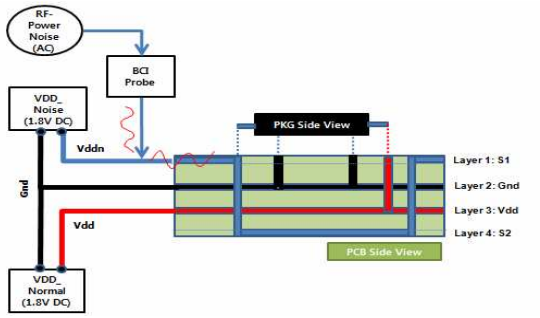

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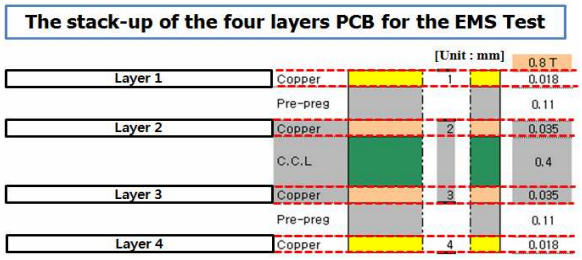
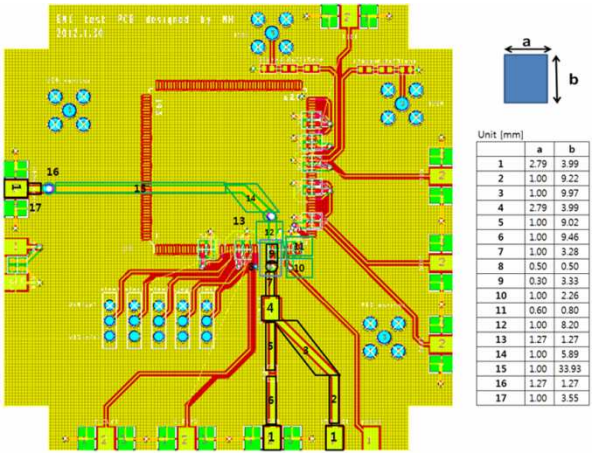


(c)

Fig. 11. PCB design layout with four layers for the BCI test (a) The definition of the PCB layer (Layer 1: signal, Layer 2: GND, Layer 3: Vdd normal, and Layer 4: signal), (b) the side view of the noise power injection path and normal power plane in the four layers PCB, (c) the stack up structure for the EMS test PCB in the 4-layer PCB.

the usage of each layer is shown in Fig. 11(a). The cross sectional view of the noise injection path is shown in Fig. 11(b) and the details of the PCB stack-up structure is shown in Fig. 11(c). This noise injection path consists of segments on the top PCB layer (Layer 1) and the bottom PCB layer (Layer 4).

Two types of power, noise power and normal power are supplied to the PCB, as shown in Fig. 11(b). The noise power line uses Layer 1 and Layer 4 of the PCB, while the normal power plane uses Layer 3 of the PCB. The normal power supply is employed to power the input clock circuitry, while the noise power is used to power the I/O buffers that are used for testing. Layer 2 is used for the ground plane. The BCI noise power trace and the noise power monitoring trace are composed of 17 segment cells from port-1 to port-2 is shown in Fig. 12(a). The equivalent circuit model of the PCB trace is employed with transmission line method (TLM) and is implemented using *RLGC* parameters, as shown in Fig. 12(b). The equivalent circuit *C*, *L*, *G*, and *R* values of segment cells are obtained as follows.



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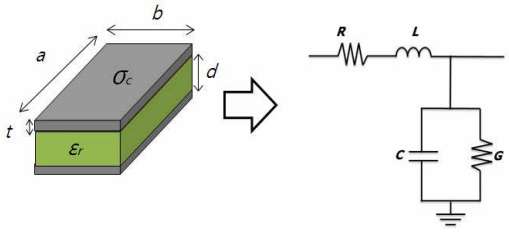


(b)

Fig. 12. Modeling of the noise injection trace on PCB (a) The noise injection trace consisting of 17 segments on top-layer, (b) transmission line based the equivalent circuit model for each segment.

$$C = \varepsilon_0 \varepsilon_r \frac{a \times b}{d},\ L = \mu_0 d\left(\frac{b}{a}\right),\ G = 2\pi f C \tan(\delta),$$
$$R = R_{dc} + R_{ac} = \frac{2}{\sigma_c t}\left(\frac{b}{a}\right) + 2\left(\frac{b}{a}\right)\sqrt{\frac{\pi f \mu_0}{\sigma_c}}. \quad (13)$$

where a is the vertical width of a segment cell, b is the horizontal width of a segment cell, d is the separation distance between ground planes, $tan\ (\delta)$ is the loss tangent of the dielectric, t is the metal thickness, σ_c is the conductivity of the metal, ε_0 is the permittivity of free space, μ_0 is the permeability of free space, ε_r is the relative permittivity of the dielectric, and f is the frequency [17].

After deriving the *RLGC* values of each segment, the equivalent circuit for the noise injection trace and the noise monitoring trace between port-1 and port-2 is constructed and shown in Fig. 13. A comparison of *S*-parameters between port-1 and port-2 extracted from the proposed model and the VNA measurement results is shown in Fig. 14 over the frequency range of the BCI test which is from 10 MHz to 1 GHz. Good agreement between the simulated and measured *S*-parameter (S_{11}, S_{21}) results is observed.

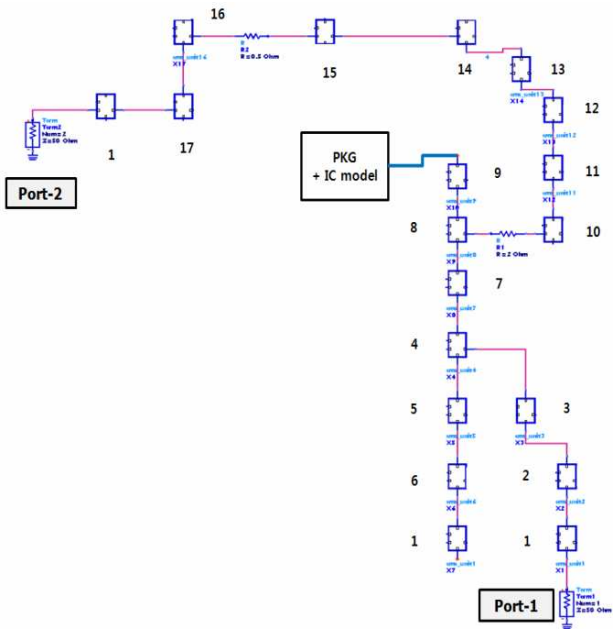


Fig. 13. The equivalent circuit model of the PCB trace used for noise injection and noise monitoring.

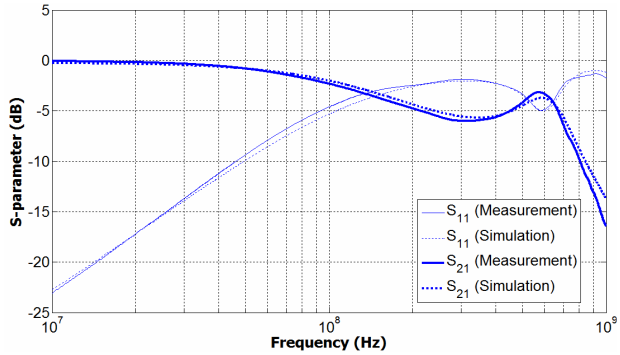
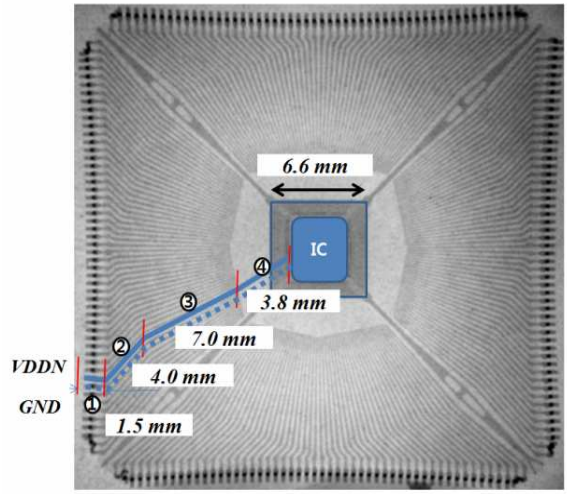


Fig. 14. The *S*-parameter simulation and measurement data of the PCB.



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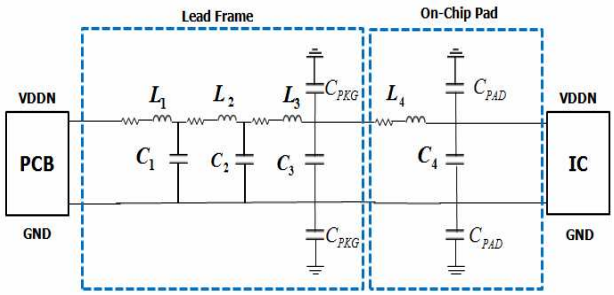


(b)

Fig. 15. The package and the equivalent circuit model of 208 LQFP package (a) The X-ray figure; (b) the equivalent circuit model.

3. Modeling of Package

In order to obtain the lead frame dimensions for equivalent circuit model construction, X-ray figure was generated for the 208 low-profile quad flat package (LQFP) package as shown in Fig. 15(a). From the X-ray

figure, the package lead frames were split to four segment lines. For each segment, the *RLC* values of each segment in the equivalent circuit model were constructed using the following expressions.

$$R=\frac{\rho\cdot l}{w\cdot t}, L=\frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{8h}{w+t}+1\right)\right],$$
$$C=\varepsilon_0\varepsilon_r\left[1.13\left(\frac{w}{h}\right)+1.44\left(\frac{w}{h}\right)^{0.11}+1.46\left(\frac{t}{h}\right)^{0.42}\right]. \quad (14)$$

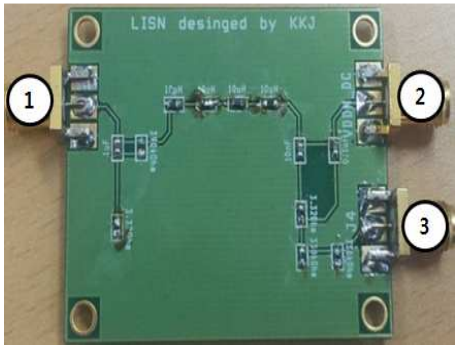
where t is the thickness, w is the width , h is the height, and l is the interconnect length [18]. The equivalent circuit model of the lead frame is displayed in Fig. 15(b).

4. Modeling of the LISN

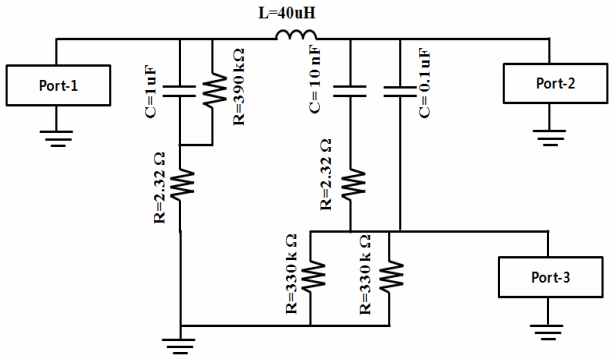
When a BCI test is conducted, both the DC power and the RF current generated from the BCI probe is supplied to the PCB-package-IC. Due to impedance mismatches, the RF power can reflect back, and the RF current generated from the BCI probe can also flow to the DC supply. These RF power can cause damage to the DC supply. To avoid damage that is caused by this interaction, LISN was employed. For our BCI test purpose, LISN is fabricated on PCB as shown in Fig. 16(a). LISN is placed between the DC power supply and the BCI probe. The DC power supply is connected at port-1, the BCI probe is connected at port-2. In order to pass DC and block RF, the insertion loss (S_{21}) between port-1 and port-2 should show low-pass filter characteristics. Port-3 can be used optionally to measure the reflected RF noise [19]. The circuit model of the LISN used in the simulation model of the BCI test is shown in Fig. 16(b). This is the standard equivalent circuit model for LISNs. The measured and simulated insertion loss (S_{21}) between port-1 and port-2 is displayed in Fig. 17.

5. Modeling of the IC

The IC model includes interconnections for power distribution networks and transistors for the switching I/O buffers used for BCI test. The test circuits were designed using a commercial 6 metal layer, 0.18 μm CMOS process. Power distribution grids are used to effectively provide power/ground voltages in IC



(a)



(b)

Fig. 16. The LISN and the equivalent circuit model (a) A photograph of the LISN implemented on PCB, (b) the equivalent circuit model [19].

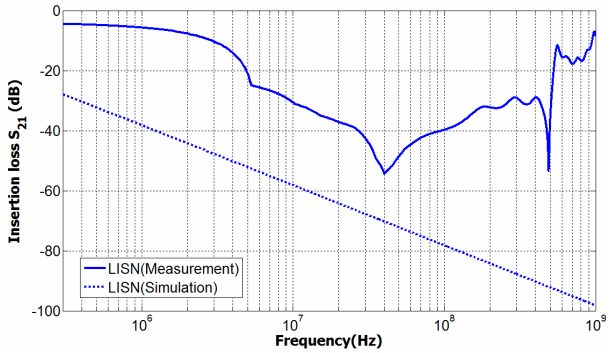
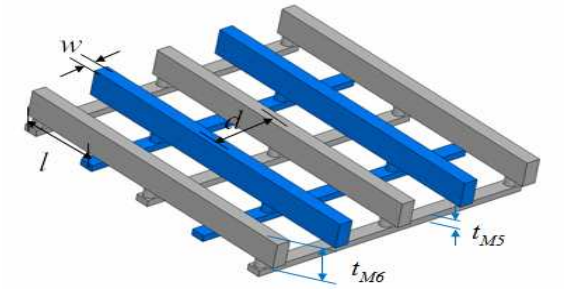
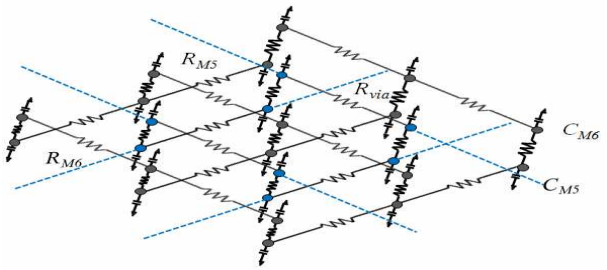


Fig. 17. Simulation and measurement results of the LISN.

networks. The interdigitated on-chip power delivery network (PDN) that is used in our test IC is shown in Fig. 18(a). The spacing between the power line and ground line is 50 μm, the widths of each line are 10 μm, and the power and ground line pitch is 100 μm. The equivalent RC circuit model of the grid structures is shown in Fig. 18(b). The RC network of the power/ground grid structures were constructed using the post layout extraction tool, Mentor Graphics' Calibre xRC [20].

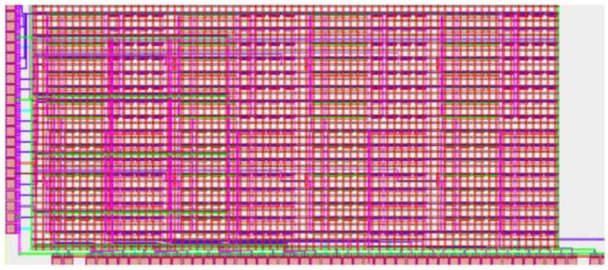


(a)

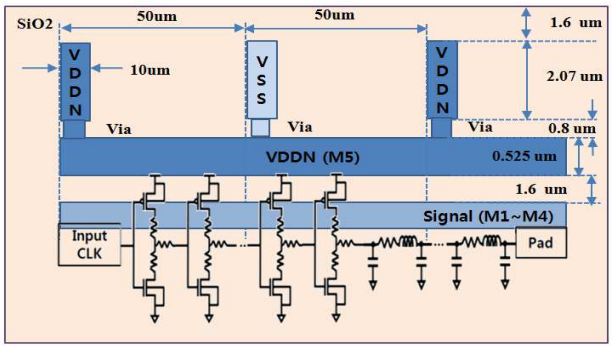


(b)

Fig. 18. The on-chip power distribution structure (a) Interdigitated grid structure, (b) the equivalent RC circuit of the power grid structure.



(a)



(b)

Fig. 19. A photograph of the I/O buffer chip (a) Top-view of the chip layout, (b) cross-sectional view of the on-chip PDN.

The layout of the I/O buffer chip and a side view of the on-chip PDN are shown in Fig. 19(a) and (b), respectively. On-chip power distribution grids are located on the top two metal layers. Under this PDN, there are I/O buffers connected with this power grid structure. The single I/O buffer circuit consists of four blocks, and each block inverter is composed of five inverters, as shown in Fig. 20. An external signal (S0~4, T0~4) was employed to control the amount of current to I/O switching buffers. The maximum switching current was 20 mA per I/O blocks and an even inverter with the same phase was constructed. The switching currents of I/O buffers make the simultaneous switching noise (SSN). When the injected RF noise is added on top of the SSN, the voltage fluctuation of power lines is critical to chip failure. To analyze the critical maximum noise of on-chip PDN, all I/O buffers was turned on for BCI tests.

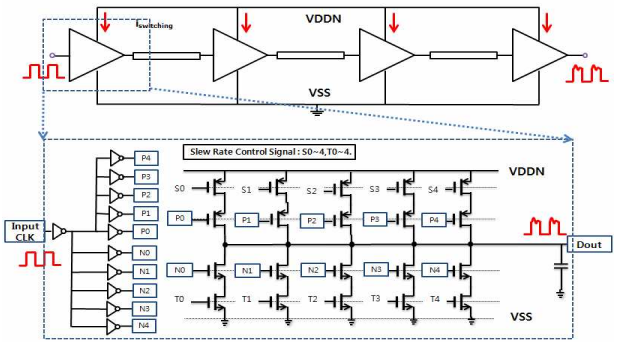


Fig. 20. Structure of a single I/O buffer circuit.

Table 1. The model summary of the BCI test components

Component	Data and method used to generate equivalent circuit model
BCI probe	Measured S-parameters and geometry information
PCB	Measured S-parameters and geometry information
Package	Geometry information
LISN	Measured S-parameters
On-chip interconnect	GDS file, interconnect technology information and layout parasitic extraction tool
I/O buffer	BSIM4 based SPICE netlist

6. Summary of the BCI Test Equivalent Circuit Model

The model summary of the proposed BCI test components explained in this section is shown in Table 1. Usually the off-chip test components have stronger frequency dependence because the size of the geometry is much longer than the wavelength. So for those components, the S-parameters were measured, the models were optimized to match them. The models of IC,

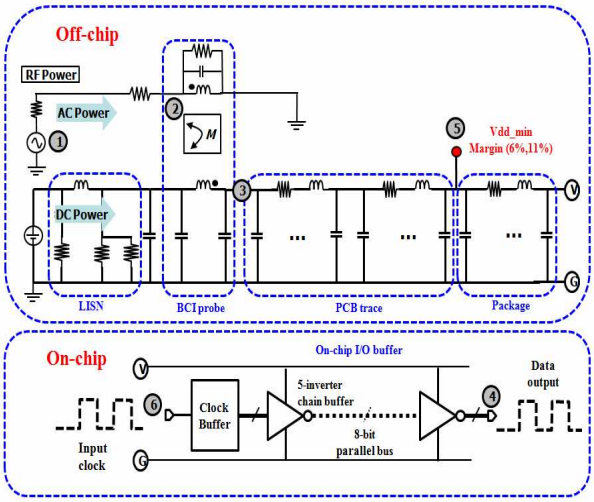


Fig. 21. The final model for the BCI test.

the switching I/O buffer transistors and on-chip interconnects are based on the circuit schematic netlist and layout information. The final simulation model structure is shown in Fig. 21. The off-chip BCI test component models are developed to accurately capture the frequency dependence.

V. Results and Discussion

To validate the proposed BCI test model for an I/O buffer chip, we constructed a BCI test system using an I/O buffer, as shown in Fig. 22. The input clock to I/O buffer is applied at node-6, and the output signal is monitored at node-4. The BCI probe generated RF noise is applied at node-3. The Vdd fluctuation is monitored at node-5 using oscilloscope.

The simulation and measurement results of the BCI test are compared in Fig. 23. For the failure criteria, Vdd fluctuation of 6% or 11% as previously shown in Fig. 3 is used. For each frequency of RF generator, the power is swept until the Vdd fluctuation exceeds the failure criteria. When the failure criteria are met, the power measured at RF generator, which is called the forward power, is recorded for simulation and measurement. So, smaller forward power means reduced immunity. The maximum forward power applied is limited to 20 dBm for IC and equipment safety. The measurement results show the reduced immunity at 40 MHz and 200 MHz. This is related to the resonance frequencies observed in transfer impedance Z_{21} of the power deliver network as

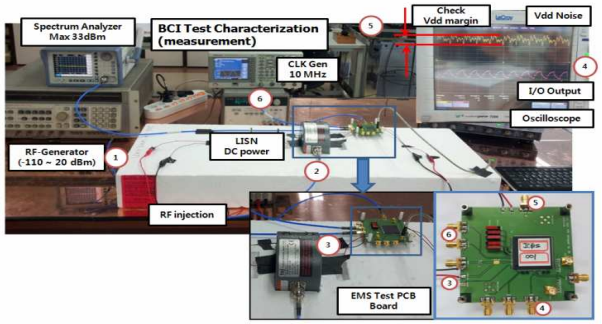
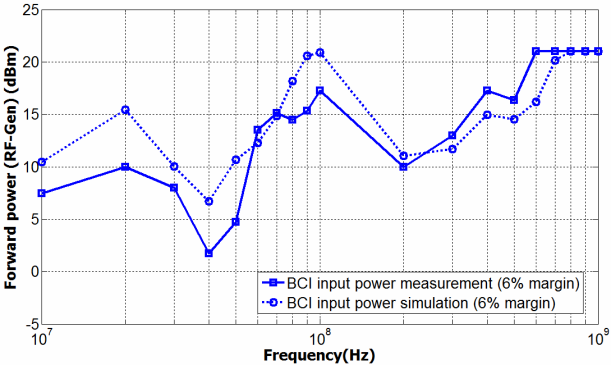
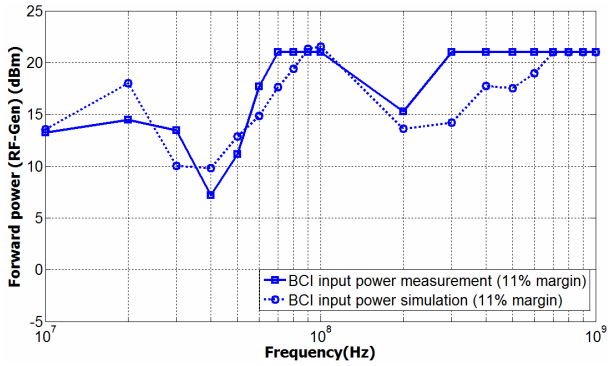


Fig. 22. The proposed BCI test system using the I/O buffer IC.



(a)



(b)

Fig. 23. Comparison of the simulation and measurement results for the BCI test (6%, 11% margin) (a) The results of a 6% Vdd margin for the typical voltage (1.8 V), (b) the results of an 11% Vdd margin for the typical voltage (1.8 V).

shown in Fig. 24. When the BCI injected RF frequencies increase beyond 400 MHz, the chip didn't fail even though the maximum power 20 dBm is applied. The high frequency components beyond did not pass through the BCI test in this frequency range. This can be a limitation of the BCI test itself.

On-chip decoupling capacitors were added in the on-chip power distribution network of the I/O buffers to see

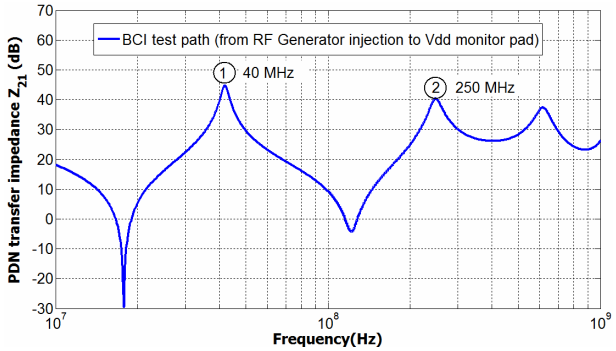


Fig. 24. Transfer impedance of power delivery network which is the BCI noise injection path.

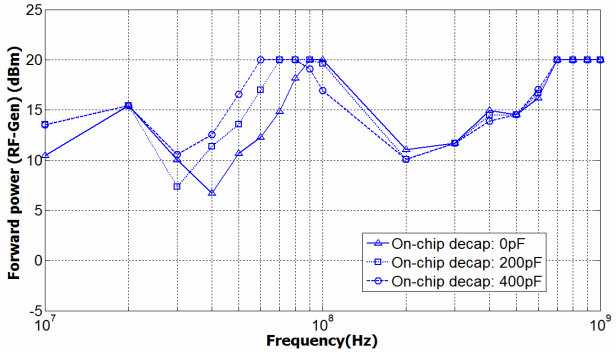


Fig. 25. Effect of on-chip decoupling capacitance on improving immunity (6% margin).

how it affects the IC immunity through simulations. Adding on-chip decoupling capacitors can improve the immunity between 40 MHz and 200 MHz as shown in Fig. 25. The high frequency characteristics beyond 400 MHz are limited by the BCI injection test setup, so adding on-chip decoupling capacitor did not help.

VI. CONCLUSIONS

In this paper, BCI immunity measurement and simulations were conducted for 1.8 V mobile I/O buffers. Equivalent circuit models were developed for BCI test components, such as BCI probe, LISN, PCB, PKG and IC. The simulated BCI test results are correlated with measurements for immunity criteria of two Vdd margins (6%, 11%). The forward power which indicates the immunity level of IC is related to the transfer impedance characteristics of the on- and off-chip power distribution network. Adding on-chip decoupling capacitors help improve immunity over certain frequency range. The equivalent circuit models developed for BCI test components can be reused to predict and improve the immunity level of the circuit at the IC design stage using circuit simulators.

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