An Accurate Gate-level Stress Estimation for NBTI

Sangwoo Han*, Junho Lee*, Byung-Su Kim, and Juho Kim***

Abstract—Negative bias temperature instability (NBTI) has become a major factor determining circuit reliability. The effect of the NBTI on the circuit performance depends on the duty cycle which represents the stress and recovery conditions of each device in a circuit. In this paper, we propose an analytical model to perform more accurate duty cycle estimation at the gate-level. The proposed model allows accurate (average error rate: 3%) computation of the duty cycle without the need for expensive transistor-level simulations Furthermore, our model estimates the waveforms at each node, allowing various aging effects to be applied for a reliable gate-level circuit aging analysis framework

***Index Terms*—NBTI, reliability, circuit aging**

I. INTRODUCTION

Continued miniaturization of the semiconductor process has opened up new problems that were not taken into account in the past. In particular, several reliability issues have come to the fore, such as hot carrier injection (HCI), bias-temperature instability (BTI) and electromigration (EM). The importance of such problems is gradually increasing with demand for the high-reliable complementary metal oxide semiconductor (CMOS) devices. In particular, reliability considerations can place significant constraints on product competitiveness at the early design stages since the time to market (TTM) in product development is reducing.

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* Department of Computer Science Engineering, Sogang University
** Samsung Electronics Co. Ltd.
E-mail: melren@sogang.ac.kr

Negative BTI (NBTI), that is, where the stress phase ($V_{gs}<0$) and recovery phase ($V_{gs}=0$) depend on the voltage applied a PMOS gate, can be modeled by the change in the threshold voltage as a function of time based on the reaction-diffusion (RD) model. For example, Bhardwaj et al. suggested a long-term model that accounts for the stress/recovery phase by using a duty cycle (α) (1) [1].

$$\Delta V_{th,t} = \left(\frac{\sqrt{K_v^2 \alpha T_{clk}}}{1-\beta_t^{1/2n}} \right)^{2n} \tag{1}$$

Exponent n is determined by the diffused substance; it is 1/4 for hydrogen atoms (H) and 1/6 for hydrogen molecules (H_2). T_{clk} denotes the clock period. See Ref. [1] for the definitions of the other parameters.

In recent NBTI-related work, the duty cycle (α) and T_{clk} have been used to account for the stress/recovery phenomenon of the NBTI [1-3]. The duty cycle represents the ratio between the on and the off time of the PMOS and can be calculated for each transistor in a circuit as follows:

$$\alpha = \frac{T_{Low}}{T_{High} + T_{Low}} \tag{2}$$

where T_{Low} and T_{High} denote the on and off times of a PMOS, respectively. T_{clk} can be expressed as the sum of T_{Low} and T_{High}.

In general, logic simulation and probabilistic methods are used to calculate the duty cycles at each gate input in a circuit [4]. As shown Fig. 1, however, the duty cycle calculated by the conventional methods can be different from the results of transistor-level simulations since the conventional methods ignore the input rising/falling transition times. Therefore, a more accurate stress estimation method at the gate-level that accounts for the

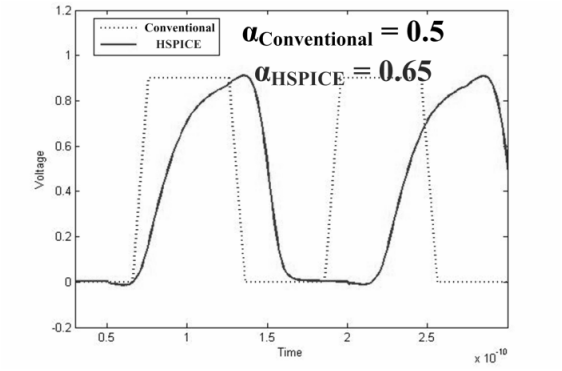


Fig. 1. Comparison the probabilistic method with HSPICE at the output of an inverter.

input transition times is required for accurate aging analysis.

Here, we propose an analytical model for more accurate duty cycle estimation at the gate- level. Our approach is to estimate the output waveform of each gate in a circuit by using a standard cell library and static timing analysis (STA). This approach does not incur the additional costs of constructing extra libraries and shows results similar to those of transistor-level simulations.

The rest of this paper is organized as follows. In Section II, we present our analytical model for accurate duty cycle estimation. The experimental results are then given Section III, and the concluding remarks are presented in Section IV.

II. STRESS ESTIMATION AT THE GATE- LEVEL

1. Conventional Stress Estimation

For the NBTI, as above mentioned, the duty cycle α and T_{clk} at the gate input are used to represent the stress condition of each transistor in a gate. To estimate the degradation of the circuit due to the NBTI, therefore, the duty cycles and T_{clk} at each gate input in a circuit should be calculated.

The simplest method to calculate the duty cycle of each node in a circuit is logic simulation. If the input vectors at the primary inputs of each transistor are known, then the entire circuit can be simulated. In logic simulation, therefore, the signal waveforms at each gate input can be obtained and used to compute the duty cycles at each gate input. However, this method is impractical because of the difficulty involved in determining the primary input waveforms in a circuit. This input pattern dependency was avoided in [4], where the duty cycles of each gate input were statistically estimated by logic simulations for randomly generated input vectors, with the specified duty cycles for the primary inputs. Although this approach is very accurate, it is quite time consuming since the logic simulation must be repeated until the mean value of the duty cycle at each gate input is within a confidence interval specified in advance. Another input pattern-independent method is the probabilistic method which propagates the statistical duty cycles directly from the primary inputs into the circuit. In the case of a two-input NAND gate, for example, when given α_A and α_B for each input, the duty cycle α_{Out} is equal to $(1-\alpha_A)(1-\alpha_B)$ since the output voltage of a two-input NAND is low when the input voltages at both inputs are high.

As mentioned earlier, the duty cycle calculated by the above methods can produce inaccurate aging analysis results because these conventional methods do not consider the falling/rising transition times.

2. PROPOSED METHOD

Our basic idea is prediction of the output waveforms at each gate in a circuit using the STA results collected when the device is fresh (not aged). Since our approach does not involve iterative simulations, the computational cost of our approach is less than the method in [4].Moreover, when compared with the probabilistic method, the additional costs of our approach essentially equate to the cost of the STA in the fresh state, which is nevertheless essential for timing verification in that state.

Fig. 2 shows the output waveforms of an inverter when the input is falling. If the input to the inverter starts falling at time x with an input transition time IN_f, the start and end times of the rise at the output node of the inverter can be calculated using the rising delay D_r and the output transition time Out_r as follows:

$$Start_{Rise} = x + \frac{1}{2} IN_f - \frac{1}{2} Out_r + D_r , \quad (3)$$

$$End_{Rise} = x + \frac{1}{2} IN_f + \frac{1}{2} Out_r + D_r . \quad (4)$$

Similarly, the falling waveform at the output node can

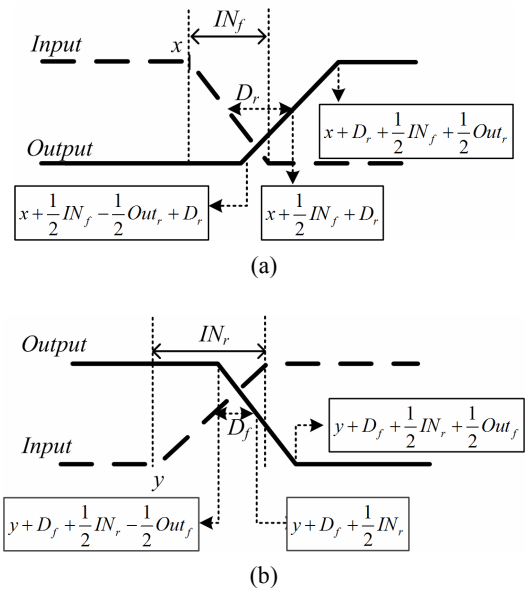


Fig. 2. Input/output waveforms of inverter when input is (a) falling, (b) rising.

be obtained using (5) and (6) when the input of the inverter starts rising at time *y*.

$$Start_{Fall} = y+\frac{1}{2}IN_r-\frac{1}{2}Out_f+D_f\,, \tag{5}$$

$$End_{Fall} = y+\frac{1}{2}IN_r+\frac{1}{2}Out_f+D_f\,. \tag{6}$$

where IN_r is the input rising transition time. Out_f and D_f denote the output falling transition time and the falling delay of the inverter, respectively. The values of D_r, D_f, Out_r and Out_f for the gates can be obtained from a conventional standard cell library. By using the above equations, therefore, the output waveforms of the gates can be predicted more accurately without the additional cost of constructing an extra library.

Fig. 3 shows the input stress waveform of an inverter when given the duty cycle α, stress cycle time T_{clk}, and input rising and falling transition times IN_r and IN_f respectively. As shown in Fig. 3, the start times for the rise and fall are represented by α, T_{clk}, IN_r and IN_f. Therefore, the duration of high output, T_{High}, can be calculated by subtracting End_{Rise} from $Start_{Fall}$. If we substitute $-IN_f$ and $\alpha_{IN}T_{clk}$ for *x* and *y* respectively after subtracting (4) from (5), we can obtain T_{high} as follows:

$$T_{High} = \left(\alpha_{IN}\times T_{clk}\right)-D_r+D_f+\beta\,, \tag{7}$$

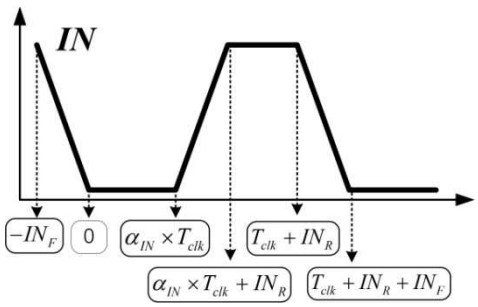


Fig. 3. Input waveform of inverter when given α, T_{clk}, IN_R and IN_F.

$$\beta = \frac{IN_r+IN_f-Out_r-Out_f}{2}\,. \tag{8}$$

The duration of the low output, T_{Low}, can be obtained similarly by subtracting (6) from (3). It should be note that *x* in (3) is substituted by (T_{clk}+IN_r), and not by -IN_f.

$$T_{Low} = \left(\left(1-\alpha_{IN}\right)\times T_{clk}\right)+D_r-D_f+\beta \tag{9}$$

Using (7) and (9), the duty cycle at an output α_{Out} can be calculated by (2).

In the case of multiple input gates such as in a two-input NAND and NOR gates, α_{Out} can be represented by the average duty cycle, which can be calculated for each input as follows:

$$\alpha_{Out} = \frac{1}{N}\sum_{i=1}^{N}\sum_{j=1}^{2^{N-1}}p_{i,j}\alpha_{i,j} \tag{10}$$

where N is the number of inputs of the gate. $p_{i,j}$ denotes the probability of the j^{th} other inputs' combination for the i^{th} input. In the case of a two-input NAND gate with α_A and α_B at each input, for example, a transition at input A can be propagated to the output when input B is high. Therefore, $p_{A,1}$ is equal to (1-α_B) and $\alpha_{A,1}$ is equal to $\alpha_{Out,A}$ which can be obtained from the above equations. When input B is low, however, the output of a two-input NAND gate is always high regardless of input A (see Table 1). Thus, $\alpha_{A,2}$ is zero and $p_{A,2}$ is equal to α_B. For a two-input NOR gate, in contrast, $p_{A,1}$ is equal to α_B since a transition at input A is propagated to the output when input B is low. When input B is high, in addition, the output of a two-input NOR gate is always low and so $\alpha_{A,2}$ is one.

In this paper, we only consider negative-unate-function-type gates such as inverters, NAND and NOR gates.

Table 1. Truth tables of 2-input gates

Inputs		Output	
A	B	NAND	NOR
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	0

Positive-unate-function-type gates, however, can be easily calculated by switching x and y in (3), (4), (5), and (6). With the proposed method, in addition, we can predict the rising and falling transition times at the output node. Therefore, the proposed method can also be used to analyze other aging effects such as HCI at the gate-level. In the future, applications of the proposed model could extend to the study of various aging effects.

III. EXPERIMENTAL RESULTS

To verify the accuracy of the proposed model, it was compared with transistor-level simulations performed using HSPICE with an inverter from the Nangate Generic Open Cell Library and two- and three-input NAND/NOR gates [5]. The 16 nm predictive technology model (PTM) was used for the HSPICE model parameters [6], and T_{clk} was set to 1E-9 s. The duty cycle of the proposed model was obtained using MATLAB with a pre-characterized standard cell library.

Fig. 4 shows the comparison results of the probabilistic method and the proposed model with the HSPICE results for an inverter. The rising and falling transition times at the input were set to 3E-11 s. As can be seen in the graph, while a distinction is seen between the results of the probabilistic method and HSPICE, the proposed model

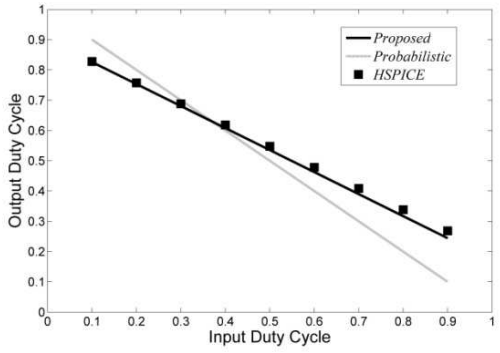


Fig. 4. Comparison of the probabilistic method and the proposed model with HSPICE.

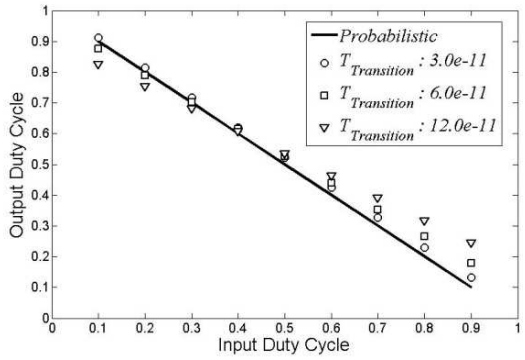
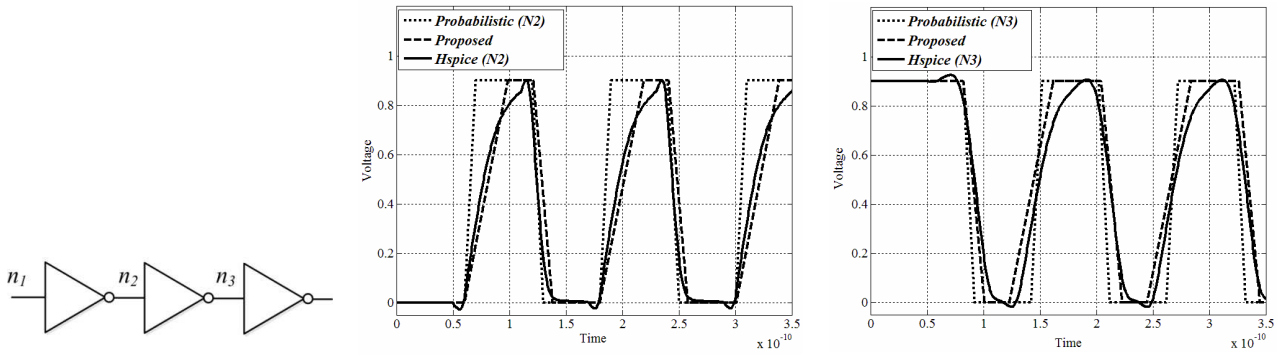


Fig. 5. The impact of the input transition time on the output duty cycle for an inverter.

shows results similar to those of HSPICE. The differences between the probabilistic method and HSPICE increase with the rising and falling transition times at the input (Fig. 5). This phenomenon results from the impact of the input transition times on the output waveform. For the probabilistic method, the ideal waveform with no transition times is generally assumed for the input stress condition. As the transition time increases, therefore, this assumption used in the probabilistic method can lead to inaccurate results in gate-level aging analysis.

Fig. 6 shows the three-stage inverter chain (a) and output waveforms at n_2 (b) and n_3 (c). We used the input rising and falling times (at n_1) for the rising and falling times of the probabilistic method to equalize cycle times (T_{clk}+Out_r+Out_f) with those of Hspice and the proposed method. When given a duty cycle of 0.5 at n_1, the probabilistic method produced a value of 0.5 for the duty cycle at both nodes n_2 and n_3. As shown in Fig. 6(b) and (c), however, the results of HSPICE are markedly different from those of the probabilistic method, especially T_{High} at n_2 and T_{Low} at n_3. The proposed model, in contrast, accurately predicted the output waveforms at both nodes.

We compared the probabilistic method and the proposed model with HSIPICE to verify their accuracies for multi-input gates (Table 2). α_{IN} denotes the duty cycle at the first input; the duty cycles at other inputs were set to 0.5. The rising/falling transition times were set to 0.12E-9s. While the probabilistic method has an error of 11% on an average, the proposed model shows an error of less than 3% on an average. In addition, the maximum error of the proposed model is less than 10%, whereas the probabilistic method has a maximum error of 47%.



(a) (b) (c)

Fig. 6. (a) 3-stages inverter chain, (b) the waveforms at n_2, (c) the waveforms at n_3.

Table 2. Comparison results for multiple-input gates

	α_{IN}=0.1					α_{IN}=0.5					α_{IN}=0.9				
	Hspice	Probabilistic		Proposed		Hspice	Probabilistic		Proposed		Hspice	Probabilistic		Proposed	
	α_{Out}	α_{Out}	Err	α_{Out}	Err	α_{Out}	α_{Out}	Err	α_{Out}	Err	α_{Out}	α_{Out}	Err	α_{Out}	Err
2NAND	0.459	0.450	2%	0.453	1%	0.276	0.250	10%	0.270	2%	0.094	0.050	47%	0.088	7%
3NAND	0.239	0.225	6%	0.235	2%	0.140	0.125	10%	0.137	2%	0.041	0.025	39%	0.038	6%
2NOR	0.945	0.950	1%	0.939	1%	0.787	0.750	5%	0.774	2%	0.630	0.550	13%	0.608	4%
3NOR	0.979	0.975	0%	0.974	1%	0.902	0.875	3%	0.890	1%	0.825	0.775	6%	0.806	2%
Average error	-	2%		1%		-	7%		2%		-	26%		5%	

IV. CONCLUSIONS

To estimate the impact of the NBTI on each device in a circuit, this paper proposes a gate-level stress estimation model that is based on the STA. The proposed model is used to examine the duty cycle for several types of gates in this paper. An important observation is that conventional stress estimation methods based on the probabilistic method can produce inaccurate gate-level aging analysis results, and more accurate stress estimation is required for precise circuit aging analysis. The proposed model allows accurate prediction of the output waveform at the gate-level; therefore, it can be used to perform gate-level analysis of circuit aging for different types of aging effects.

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Sangwoo Han received the BS degree in Physics and Computer Science from Sogang University in 2005. He also received the MS degree in Computer Science and Engineering from Sogang University in 2008. He is currently pursuing a Ph.D. degree in computer engineering at Sogang University. His research interests are variation-aware timing analysis, a robust design for process variation, and design for reliability enhancement.

Junho Lee received the B.S. degree in computer engineering from Sogang University, Korea in 2011. He is currently pursuing a M.S. degree in computer engineering at Sogang University, Korea. His research interests are variation-aware timing analysis, Monte-Carlo analysis, and design for reliability enhancement.

Byung-Su Kim received the B.S. and M.S. degrees from Sogang University, Korea, in 2003, 2005, respectively, all in computer science. From 2005 to 2012, he was with Samsung Semiconductor Inc., Giheung, Korea, working as a CAE Engineer. His research work included process variation aware timing analysis in ASIC/SOC design, and test design for process monitoring.

Juho Kim received B.S degree and Ph.D degree in Computer and Information Science from University of Minnesota in 1987 and 1995, respectively. After getting Ph.D degree, he worked as a senior member of technical staff at Cadence Design System until 1997. Professor Kim joined the department of computer science and engineering in Sogang University, Seoul, Korea in 1997, and he was a department chair from 2005 to 2008.