A 0.5–2.0 GHz Dual-Loop SAR-controlled Duty-Cycle Corrector Using a Mixed Search Algorithm

Sangwoo Han and Jongsun Kim

Abstract—**This paper presents a fast-lock dual-loop successive approximation register-controlled duty-cycle corrector (SARDCC) circuit using a mixed (binary+sequential) search algorithm. A wider duty-cycle correction range, higher operating frequency, and higher duty-cycle correction accuracy have been achieved by utilizing the dual-loop architecture and the binary search SAR that achieves the fast duty-cycle correcting property. By transforming the binary search SAR into a sequential search counter after the first DCC lock-in, the proposed dual-loop SARDCC keeps the closed-loop characteristic and tracks variations in process, voltage, and temperature (PVT). The measured duty cycle error is less than ±0.86 % for a wide input duty-cycle range of 15–85 % over a wide frequency range of 0.5–2.0 GHz. The proposed dual-loop SARDCC is fabricated in a 0.18-μm, 1.8-V CMOS process and occupies an active area of 0.075 mm^2.**

Index Terms—**Duty-cycle corrector (DCC), successive approximation register (SAR), clock duty, clock tree, duty cycle**

I. INTRODUCTION

The duty cycle of an on-chip clock signal can be distorted due to integrated circuit (IC) process errors such as device mismatches in transistors. Therefore, duty-cycle correction (DCC) circuits [1-5], capable of correcting a clock with an arbitrary duty-cycle to a 50% duty-cycle clock, are widely used in high-speed digital circuits such as microprocessors, memories, and clock recovery applications to improve performance by using both the rising and falling edges of a clock signal. Among non-feedback [1] and feedback DCCs [2-5], the non-feedback DCCs cannot track PVT variations due to their open-loop characteristic, which causes low performance and limited applications. Feedback DCCs can be classified into three categories: analog [2], digital [3], and mixed-mode [4, 5]. Analog feedback DCCs usually require a long wake-up time and digital feedback DCCs usually have limited duty-cycle correction range and a relatively large error in duty cycle. In [5], a mixed-mode feedback DCC using a successive approximation resistor (SAR) was introduced to achieve both fast duty-cycle correction and low-power consumption. However, [5] achieved limited duty-cycle correction range of only 40–60 % over a narrow frequency range of 0.3125–1.0 GHz due to the limited resolution of the delay line based duty-cycle adjuster. In this paper, we propose a novel fast-lock dual-loop SAR-controlled DCC [7], shown in Fig. 1(a), to achieve a wider duty-cycle correction range, higher operating frequency, and higher duty-cycle correction accuracy.

II. PROPOSED DUAL-LOOP SAR-CONTROLLED DCC ARCHITECTURE

Fig. 1(a) shows the block diagram of the proposed fast-lock dual-loop SARDCC. It consists of a duty amplifier (DA), a level converter in the forward path. The feedback path includes a dual-loop: analog feedback loop and digital feedback loop. In the analog feedback loop, the charge pump (CP) generates the analog control

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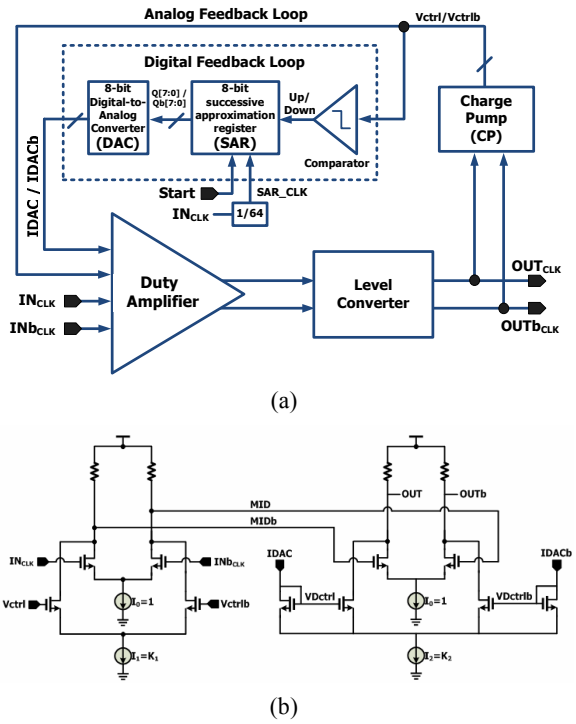


Fig. 1. (a) Proposed fast-lock dual-loop SARDCC, (b) Duty amplifier.

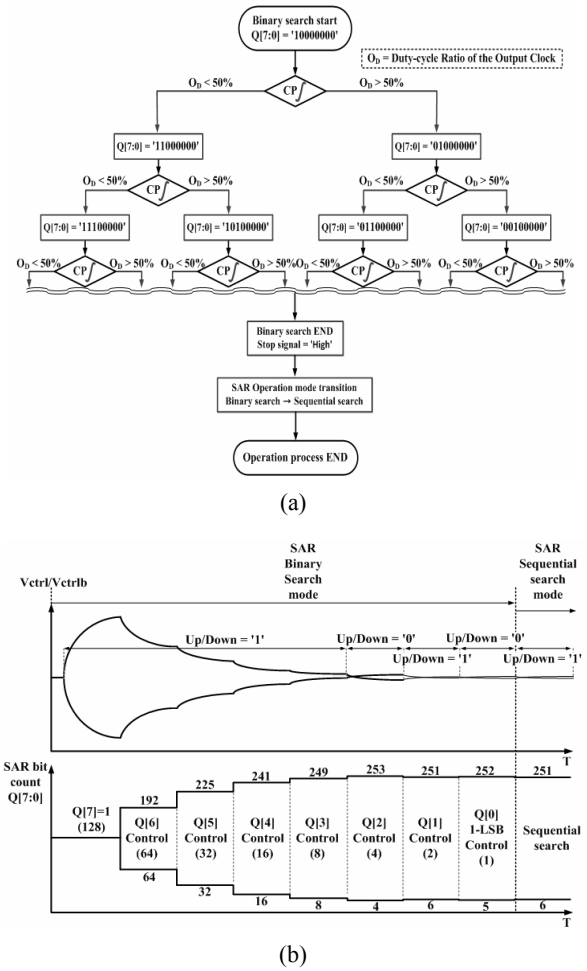


Fig. 2. (a) Flowchart of the proposed dual-loop SARDCC using mixed search (binary+sequential) algorithm, (b) Locking process of the dual-loop structure.

voltage Vctrl/Vctrlb proportional to the clock duty-cycle of the output clock (OUT_{CLK}/$OUTb_{CLK}$). The Vctrl/Vctrlb voltage is also used in the digital feedback loop to generate the digital control voltage VDctrl/VDctrlb. The digital feedback loop consists of a comparator, an 8-bit SAR, and an 8-bit digital-to-analog converter (DAC). The comparator generates the up or down signals depending on the CP outputs. The SAR has an operating clock (SAR_CLK) frequency that is 1/64 of the input clock frequency. This slow SAR using binary search scheme gives enough timing margin for the analog charge pump and DAC operation, resulting in wider duty-cycle correction range and minimized integrated errors in duty-cycle without increasing the lock time. By adapting binary search algorithm, the digital output Q[7:0] of the SAR is then used for the DAC input. The 8-bit DAC provides the quantized bias current IDAC/IDACb to generate VDctrl/VDctrlb. The two control voltages, Vctrl/Vctrlb and VDctrl/VDctrlb, are then used for the DA to correct the clock duty-cycle of the input clock, IN_{CLK}/INb_{CLK}. The DA shown in Fig. 1(b) is a two-stage duty amplifier that consists of two-cascaded differential pairs. The DA corrects external differential input clock signals with duty-cycle distortions and generates a small-swing 50% duty-cycle clock. Finally, the level converter, which acts as a small-swing to full-swing converter, produces a full-swing output clock signal, OUT_{CLK}/$OUTb_{CLK}$. When the DCC is enabled, the analog and digital feedback block starts together at the same time. Since the analog feedback block has a fast duty-correction capability by increasing the gain of the CP, the output clock duty-cycle is corrected to 50% in about only 40 clock cycles in this design. Then the digital feedback block with an initial value of the 8-bit SAR Q[7:0]=[10000000] slowly replaces the analog feedback block. This replacement process is described in Fig. 2.

Fig. 2(a) shows the flowchart of the proposed mixed search (binary+sequential) algorithm to replace the analog feedback loop with the digital feedback loop. Fig. 2(b) shows the locking process of the proposed dual-loop

structure. At the end of the binary search mode, the DCC enters into the sequential search mode automatically. By transforming the binary search SAR into a sequential search counter after the first DCC lock-in, the proposed dual-loop SARDCC keeps the closed-loop characteristic and tracks variations in PVT. This mixed search algorithm allows slow operation of the SAR, resulting in higher operating frequency and higher duty-cycle correction accuracy due to the increased timing margin for the analog CP and DAC operation. With a SAR operating frequency that is 1/64 of the input clock frequency, the replacement time of the proposed N-bit (i.e. N=8) SARDCC utilizing binary search scheme is only N-1=7 cycles, which is 64×7=448 input clock cycles. However, the replacement time of the conventional DCC using 8-bit sequential search scheme is 64×2(N-1)=8192 cycles, which is eighteen times longer than that of the proposed dual-loop mixed search SARDCC. The proposed 8-bit SAR structure [6] is shown in Fig. 3. When the binary search is done, this SAR is transformed into a counter by setting the Senable signal high.

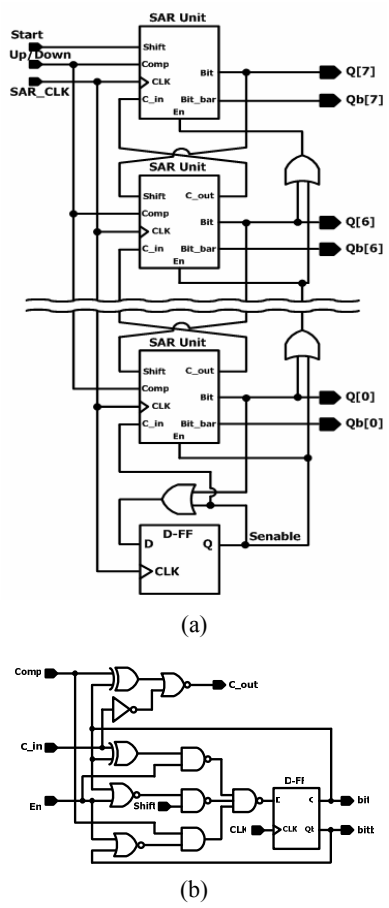


Fig. 3. (a) 8-bit SAR structure, (b) SAR unit.

III. Experimental Results

Fig. 4 shows the HSPICE simulated operation of the proposed fast-lock dual-loop SARDCC with an input duty cycle of 80% at 1GHz. The analog feedback block first achieves a 50% duty-cycle clock within the analog DCC locking period of about 40 clock cycles (= 40 ns at 1 GHz). Then the digital feedback block starts binary search to replace the analog feedback block without duty-cycle distortions during the digital DCC locking period. This dual-loop structure makes it possible to turn off the DCC without losing duty-cycle lock information.

Fig. 5 shows the measured input and output clocks of the SARDCC at 1 GHz and 2 GHz, when the input clock duty-cycle changes from 15 to 85%. The proposed DCC achieved a maximum duty-cycle error of ±0.86 % for an input duty-cycle range of 15–85% over a frequency range of 0.5–2.0 GHz. As shown in Fig. 6, the proposed DCC achieves a measured peak-to-peak jitter of 16 ps at 1 GHz. Fig. 7(a) shows the chip layout and die microphotograph of the proposed dual-loop SARDCC. It occupies an active area of 0.075 mm^2 and consumes 3.8 mW at 1.0 GHz. The SARDCC has been tested in a chip-on-board (COB), shown in Fig. 7(b), assembly. A comparison of performance between the proposed dual-loop SARDCC and other DCCs is given in Table 1.

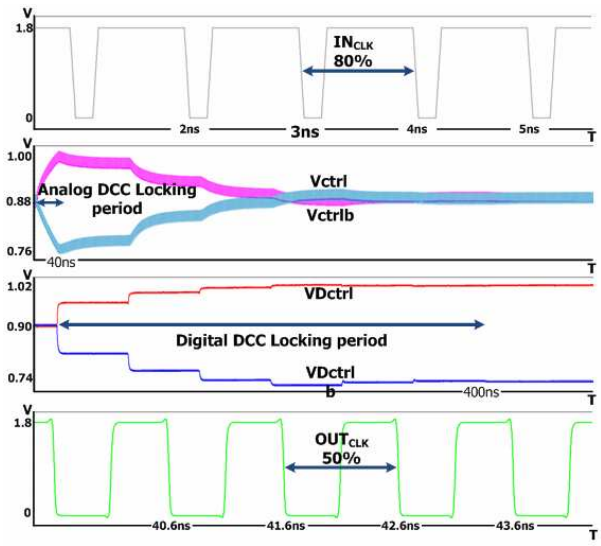
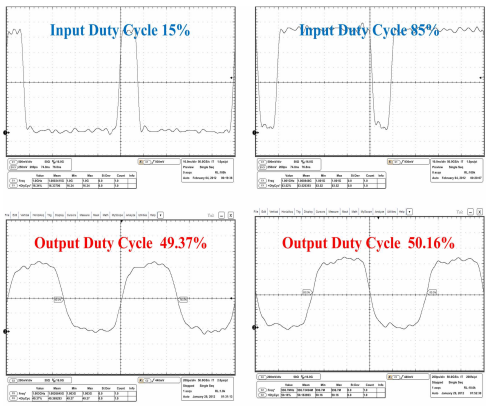
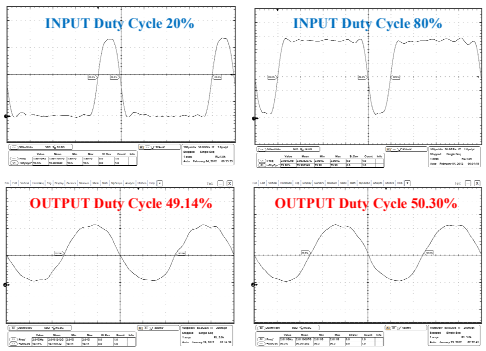


Fig. 4. Simulated operation of the proposed fast-lock dual-loop SARDCC.



(a)



(b)

Fig. 5. Measured input and output clocks at (a) 1 GHz, (b) 2 GHz.

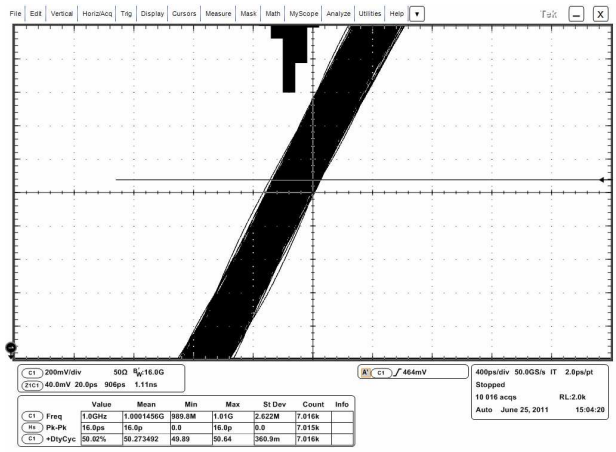
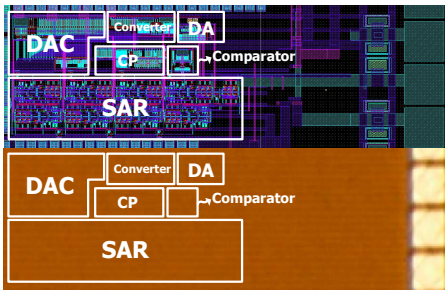


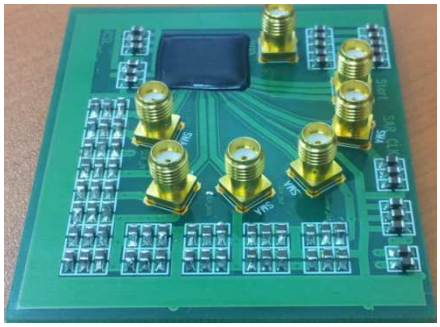
Fig. 6. Measured peak-to-peak jitter at 1 GHz.

IV. CONCLUSIONS

We propose a novel dual-loop SAR-controlled DCC to achieve wide duty-cycle correction range and to minimize integrated errors in duty-cycle without increasing the lock time. A wider duty-cycle correction range and higher duty-cycle correction accuracy have been achieved by utilizing the mixed search (binary+ sequential) SAR that gives enough timing margin for the analog charge pump and DAC operation. The proposed dual-loop SARDCC, fabricated using a 0.18-μm 1.8-V CMOS process, occupies an active area of 0.075 mm^2 and dissipates 3.8 mW of power at 1.0 GHz. The measured duty cycle error is less than ±0.86 % for a wide input duty-cycle range of 15–85% over a wide frequency range of 0.5–2.0 GHz.



(a)



(b)

Fig. 7. (a) Chip layout and die microphotograph, (b) test COB.

Table 1. Performance summary and comparison

	[1]	[2]	[5]	This work
Type	Digital / Feedback	Analog / Feedback	Mixed-mode / Feedback	Mixed-mode / Feedback
Low-power standby mode support	O	X	O	O
Process & Supply	0.18 μm 1.8V	0.13 μm 1.2V	0.13 μm 1.2V	0.18 μm 1.8V
Operation Frequency	0.8-1.2 GHz	140–780 MHz	0.312–1.0 GHz	0.5–2.0 GHz
Max. Duty-cycle Correction Range	±20% -	±25% @500 MHz	±20% -	±35% @1 GHz
Max. Duty-cycle Error	±1.4% -	±1.6% @500 MHz	±1% -	±0.86% @2.0 GHz
Chip Area	0.23 ㎟	-	0.048 ㎟	0.075 ㎟
Power	15 mW -	-	3.2 mW @1 GHz	3.8 mW @1 GHz

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