A Small-Area Solenoid Inductor Based Digitally Controlled Oscillator

Hyung-Gu Park, SoYoung Kim, and Kang-Yoon Lee

Abstract—**This paper presents a wide band, fine-resolution digitally controlled oscillator (DCO) with an on-chip 3-D solenoid inductor using the 0.13 μm digital CMOS process. The on-chip solenoid inductor is vertically constructed by using Metal and Via layers with a horizontal scalability. Compared to a spiral inductor, it has the advantage of occupying a small area and this is due to its 3-D structure. To control the frequency of the DCO, active capacitor and active inductor are tuned digitally. To cover the wide tuning range, a three-step coarse tuning scheme is used. In addition, the DCO gain needs to be calibrated digitally to compensate for gain variations. The DCO with solenoid inductor is fabricated in 0.13 μm process and the die area of the solenoid inductor is 0.013 mm^2. The DCO tuning range is about 54 % at 4.1 GHz, and the power consumption is 6.6 mW from a 1.2 V supply voltage. An effective frequency resolution is 0.14 kHz. The measured phase noise of the DCO output at 5.195 GHz is -110.61 dBc/Hz at 1 MHz offset.**

Index Terms—**Solenoid inductor, active capacitor, wide tuning range, automatic three-step coarse tuning, fine-resolution, DCO**

I. INTRODUCTION

The DCO (digitally controlled oscillator) is one of the most critical blocks in the digital PLL. Spiral inductors based on the RF process have been used in the DCOs. They occupy a large area and thereby, increasing the process cost. A solenoid inductor implementation has been studied in [1] and it mainly uses MEMS technology. By virtue of good conductivity of copper, the copper electroplated inductor has a high quality factor and it has an inductance of a tenth of nH [2]. However, post processing of the MEMS method requires an additional process cost. As the CMOS technology has started to adopt Cu instead of Al for its metal interconnection below the 0.13 μm process, it opens the possibility of implementing a low series resistance inductor in an LC DCO. However, planar spiral inductors are still being used for LC DCOs in the digital CMOS process. In this paper, a solenoid inductor using Metal stack is proposed to replace the spiral inductors which require RF CMOS process.

To overcome the limitation of the varactor capacitance, a sigma-delta modulator is used to implement the fine capacitance [3]. In this case, the dithering bits of the sigma-delta modulator need to be increased in order to implement a finer resolution. Therefore, the area and power consumption are also increased. In this paper, an active capacitor and inductor are used for the frequency control, overcoming the minimum frequency resolution problem.

Several techniques are used to cover the wide frequency range with a single LC-oscillator. The automatic coarse tuning scheme is typically used to widen the tuning range. The variation of the DCO gain (KDCO) is large in wide range applications. The automatic calibration of the DCO

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gain is necessary to guarantee the same loop bandwidth for the phase noise and lock-time performances regardless of the channel frequency.

This paper presents a wide band, fine-resolution DCO with an on-chip 3-D solenoid inductor using an automatic three-step coarse tuning loop and gain tuning loop. Electrical characteristics of solenoid inductor are evaluated in terms of inductance and its quality factor by using 3D-EM simulation in order to reduce the LC DCO area in the digital CMOS process.

Section II shows the structure of the on-chip solenoid inductor and Section III explains wide range DCO with on-chip solenoid inductor. Section IV shows the measurement results of the proposed DCO. Section V concludes this paper.

II. ON-CHIP SOLENOID INDUCTOR

Generally, a spiral structure is fabricated by using the planar CMOS process. On the other hand, the solenoid inductor shown in Fig. 1(a) is built by using Metal and Via interconnection. Moreover, the axis of the inductor is parallel to the substrate. This makes it less susceptible to substrate losses. In the structure shown in Fig. 1(b), the bottom plates are represented by M1 and the top plates by M6. Posts are connected between the top plates and the bottom plates by Vias (V1-V5). The solenoid inductance is determined by the number of turns (N), the cross-sectional area (A) that the magnetic flux is crossing, and the pitch between the turns (P). The cross sectional area (A) is given as W x H and the height is fixed by the process. Also, inductance is proportional to the width (W) and the number of turns (N).

To estimate the exact performance, when the solenoid is built into an LC DCO, a 3-D finite element electromagnetic (EM) simulator has been used to perform a precise analysis of the proposed solenoid inductor.

Fig. 2 shows the simulated inductance of the solenoid inductor with respect to the number of turns (N). The inductance values are proportional to the number of turns.

Fig. 3 shows the simulated inductance of the solenoid inductor with respect to the space between turns (N). The inductance values are inverse proportional to the space between turns.

Fig. 4 shows the simulated inductance of the solenoid inductor with respect to the metal width (W). The

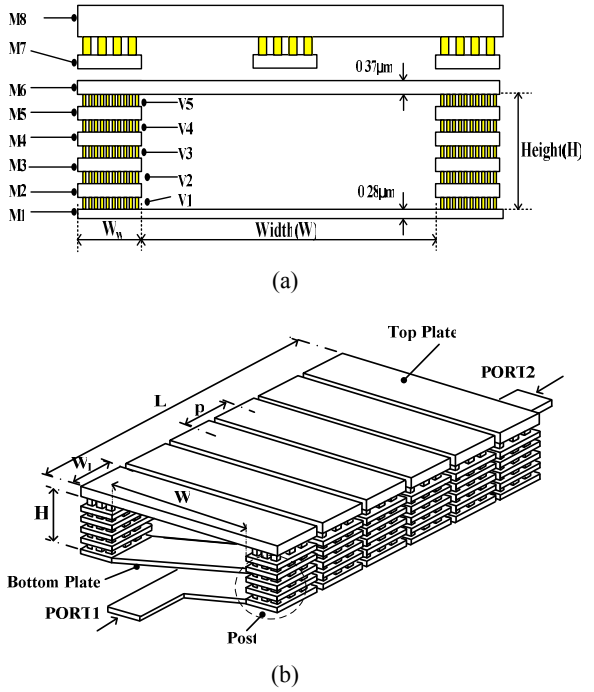

Fig. 1. (a) Cross sectional view, (b) top view of solenoid inductor.

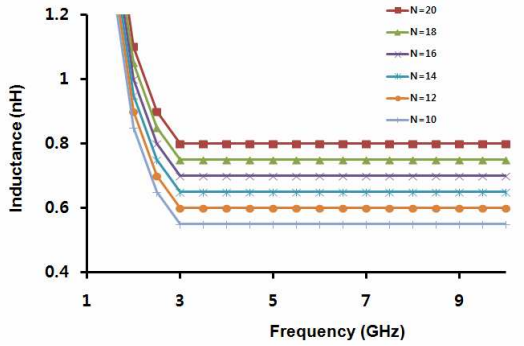

Fig. 2. Simulated inductance of the solenoid inductor with respect to the number of turns (N).

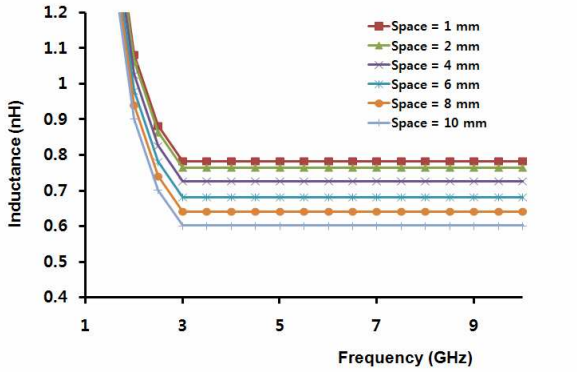

Fig. 3. Simulated inductance of the solenoid inductor with respect to the space between turns.

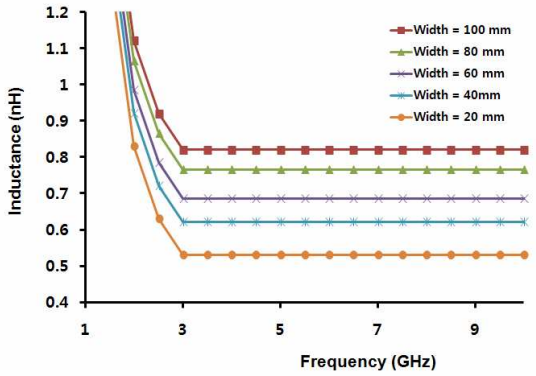

Fig. 4. Simulated inductance of the solenoid inductor with respect to the metal width (W).

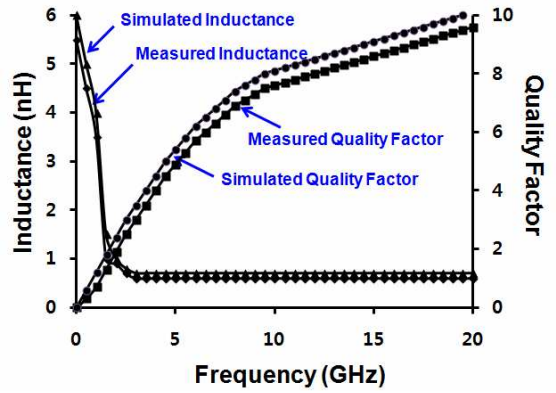

Fig. 5. Inductance and quality factor of the solenoid inductor.

inductance values are proportional to the metal width.

The measured inductance and the quality factor from de-embedding are shown along with the simulation results in Fig. 5. Both the simulated and the measured inductances are almost the same from 0.6 to 0.9 nH and it is as shown in Fig. 5. The measured quality factor is lower than that of the simulated result as shown in Fig. 5. However, the two results are almost the same over the range of interest around 5 GHz. Measurement results still show that the self-resonance frequency (SRF) is over 20 GHz.

Fig. 6 shows the quality factors of the solenoid inductor and the spiral inductor when the inductance values are both 0.6 nH. The highest thick metal is not used to form the solenoid inductor, while it is used in the spiral inductor. The quality factors of the solenoid inductor and the spiral inductor are around 6 and 12 at the frequency of 5 GHz, respectively.

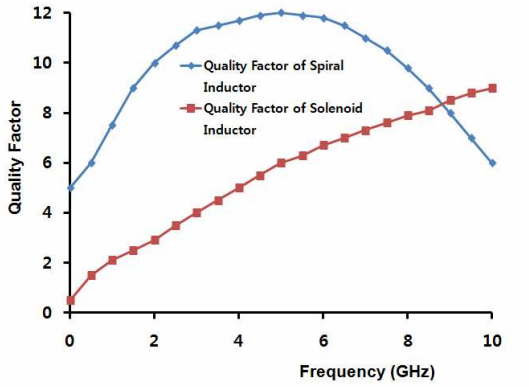

Fig. 6. Quality factors of the solenoid inductor and spiral inductor.

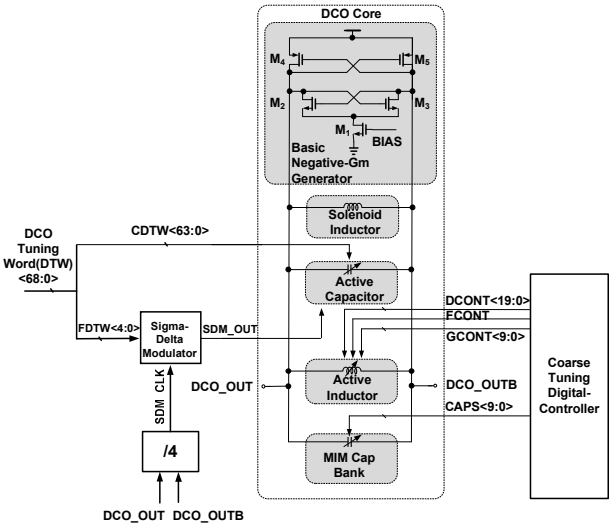

Fig. 7. The block diagram of the proposed DCO with a solenoid inductor.

III. Wide Range DCO with On-Chip Solenoid Inductor

Fig. 7 shows the block diagram of the proposed DCO with an on-chip solenoid inductor. It is composed of the DCO core, a sigma-delta modulator, and a coarse tuning digital controller. A 3rd order MASH type sigma-delta modulator is used with five dithering bits (FDTW<4:0>).

The DCO Core consists of a solenoid inductor, an active inductor, and an active capacitor, a MIM cap bank, and a negative-Gm generator. The on-chip solenoid inductor shown in Fig. 1 is used to provide the fixed inductance value and meet the phase noise performance requirements. The active inductor is used for the wide-frequency range tuning and narrow-frequency range tuning control. The

cap bank, which is composed of switches and MIM capacitors, provides the mid-frequency tuning range of the DCO. The quality factor can be increased resulting in the improvement of the phase noise performance by using the solenoid inductor in parallel with the active inductor.

Fig. 8 shows the active capacitor circuit and C-V characteristic graph. Active capacitor is also used for the fine frequency tuning. Fine capacitance can be effectively implemented by using the capacitance difference in accumulation mode and inversion mode of active capacitor [4].

When the oscillation amplitude is A_0, the total capacitance (ΔC) is given by Eq. (1)

$$\Delta C = (C_A + C_B) - (C_C + C_D) \quad (1)$$

where, C_A and C_D are capacitance in inversion mode, C_B and C_C are capacitance in accumulation mode.

Input tuning code word, CDTW<63:0>, finely controls the frequency of the DCO by adjusting the value of active capacitance. Also, the dithering output (SDM_O(2:0)) of second-order sigma-delta modulator (SDM) is applied to the Active Cap in order to increase the resolution of the DCO.

Coarse tuning controller in Fig. 7 selects the optimum capacitance values, CAPS<9:0>, to cover the target frequency closely against the PVT variations of the inductor or capacitances. In addition, active inductor control bits, DCONT<19:0>, adjust the frequency of the DCO by the middle frequency amount between the wide range coarse tuning and fine tuning.

Fig. 9 shows the schematic of the active inductor. It is a differentially configured gyrator-C active inductor [5]. The inductance (L_{eq}) of the active inductor can be tuned by varying G_{ds5}, G_{ds7}, G_{ds9}, G_{ds11}, and G_{dsGCB}, where G_{ds5}, G_{ds7}, G_{ds9} and G_{ds11} are the drain conductances of M_5, M_7, M_9 and M_{11} in Fig. 9, respectively. G_{dsGCB} is the PMOS(M_1) drain conductance of the DCO gain control cell in the DCO gain control bank in Fig. 10 and G_{ds7} is controlled by I_{D7}. As mentioned above, G_{ds9}, G_{ds11}, and G_{dsGCB} are also controlled by I_{D9}, I_{D11}, and I_{DGCB}, respectively. I_D is dependent on the gate voltage and the size of the MOS (W/L). Among transistors in Active Ind Control Block of Fig. 9, M_9 has the largest size for the wide tuning range, M_{11} has the medium size for the narrow tuning range, and M_7 has the smallest size for the fine tuning step.

Thus, the method for the inductance tuning is to control the drain conductance G_{ds7}, G_{ds9}, G_{ds11}, and G_{dsGCB} except G_{ds5} by the gate voltage and the size of the MOS. I_{D7}, I_{D9}, and I_{D11} are controlled by the FCDTW<64:0>, FCONT and DCONT<19:0> in the active inductor control bank, respectively. I_{DGCB} is controlled by the DCONT<19:0> in the DCO gain control bank.

Fig. 10 shows the complete schematic of the gain control bank of the proposed DCO. It is composed of the ten DCO gain control cell arrays which are controlled by the signals from the GCONT<9:0>. When the GCONT<N> is HIGH, the gate of the PMOS (M_1, M_2) is connected to the FCDTW<64:0>. However, if the GCONT<N> is LOW, the gate of PMOS (M_1, M_2) is connected to the VDD to disable the corresponding DCO gain control cell. The switches in the gain control cell are connected to the gate of the PMOS in order to reduce the degradation of the parasitic capacitance of the switches.

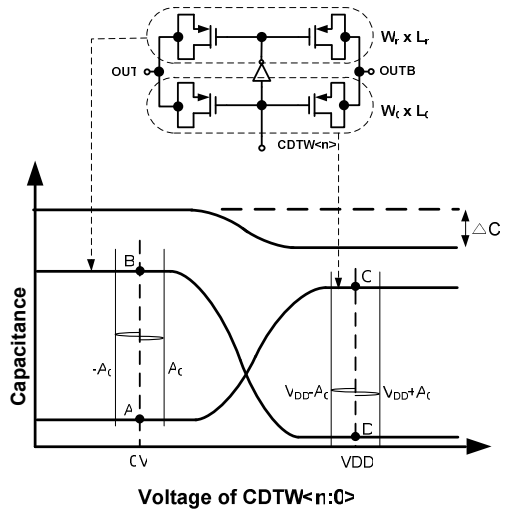

Fig. 8. The schematic of the proposed the active capacitor.

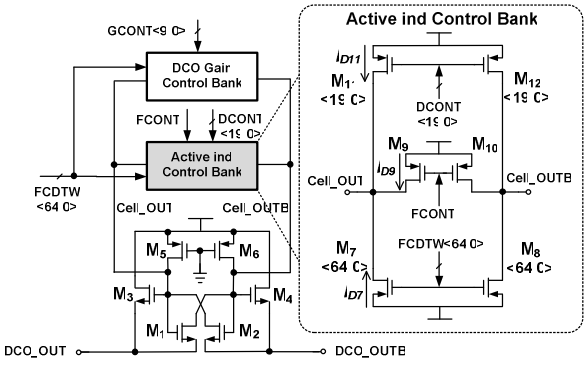

Fig. 9. The schematic of the proposed the active inductor.

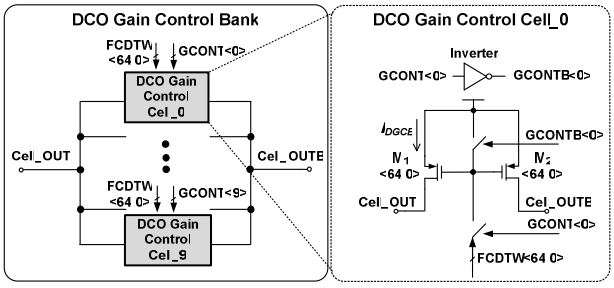

Fig. 10. The schematic of the DCO gain control bank.

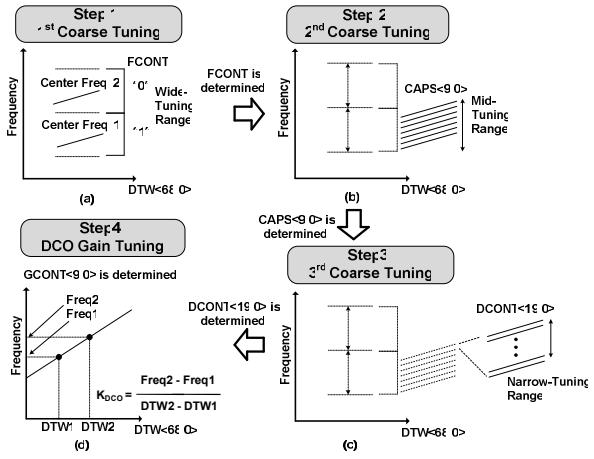

Fig. 11. The concept of proposed three-step coarse and gain tuning.

The automatic three-step coarse and gain tuning procedure are as follows. Its principle is shown in Figs. 11(a)-(d).

Step 1: The 1st coarse tuning is the wide-frequency range tuning. The DCO frequency is measured through the coarse tuning digital-controller, as seen in Fig. 11. The optimum center frequency is selected by the FCONT adjusting the large value inductance of the active inductor as shown in Fig. 11(a).

Step 2: The 2nd coarse tuning is the mid-frequency range tuning. The optimum MIM capacitances are selected through the 2nd coarse tuning process after the 1st coarse tuning is completed as shown in Fig. 11(b).

Step 3: The 3rd coarse tuning is the narrow-frequency range tuning. Because the difference between the frequency curves at the 2nd coarse tuning is several MHz, additional tuning is required. The tuning procedure is processed by adjusting the inductance of the active inductor as shown in Fig. 11(c).

Step 4: The DCO gain tuning begins when the three-step coarse tuning is completed. When the frequency of the DCO is high in the tuning range, the DCO gain (K_{DCO}) is higher than that of the center frequency. Thus, the DCO gain should be decreased by increasing the number of active gain control block in Fig. 10. On the other hand, when the frequency of the DCO is low in the tuning range, the DCO gain should be increased by decreasing the number of active gain control block in Fig. 10.

The K_{DCO}, which is defined as the frequency deviation of the DCO with respect to a 1-LSB change, is equal to the frequency resolution. Thus, the K_{DCO} is controlled by the value of the signal, GCONT<9:0>, which adjust the frequency resolution.

As shown in Fig. 11(d), the K_{DCO} can be estimated by dividing the difference of Freq2 and Freq1 by the difference of DTW2 and DTW1. It is measured and calculated though the coarse tuning digital-controller. And then GCONT<9:0> are adjusted so the K_{DCO} can reach its reference boundary.

Fig. 12 shows the automatic three-step coarse and gain tuning loop. When frequency tuning range of the DCO is wide, the variation of the DCO gain (K_{DCO}) is very large depending on the frequency. Thus, the DCO gain control bank in Fig. 9 is required for the automatic DCO gain tuning loop. The K_{DCO} can be calculated with 15-bit counter and digital blocks that can be shared with the three-step coarse tuning block. The frequency of DCO is detected through the 15-bit counter and is compared with the reference value. In the each step coarse and gain tuning control signals (FCONT, CAPS<9:0>, DCONT<19:0>,

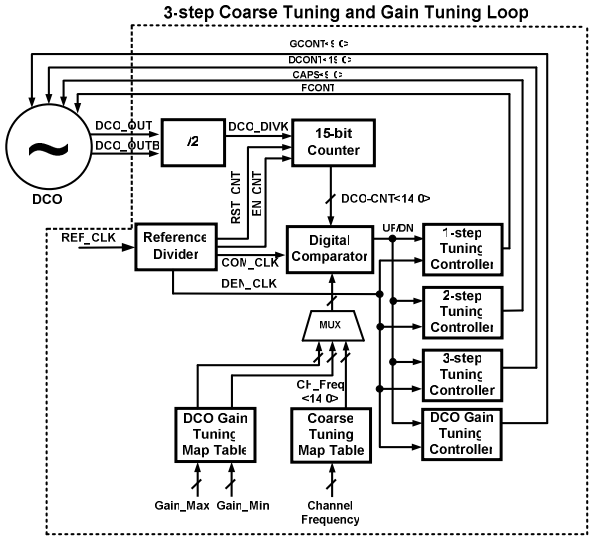

Fig. 12. The automatic three-step coarse and gain tuning loop of the proposed DCO.

and GCONT<9:0>) are determined digitally based on the comparison result. The phase difference between the external reference clock and DCO is detected at the phase frequency detector in the all-digital PLL (ADPLL). Then, it is converted into the digital tuning word, DTW<68:0>, through the digital filter. The DTW<68:0> is adjusted to finely tune the phase and frequency of the DCO at the fine tuning stage after the three-step coarse and gain tuning.

IV. Experimental Results

This chip is fabricated using the digital CMOS process with 0.13 μm technology, a single poly layer, six layers of metal, the option of metal-insulator-metal (MIM) capacitors, and high sheet resistance poly resistors. Die area of the solenoid inductor and DCO are 0.013 mm^2 and 0.034 mm^2, respectively. Fig. 13 shows the chip microphotograph of the DCO.

The LC DCO with the on-chip solenoid inductor (W=60 μm, N=18) is measured using a spectrum analyzer (HP E4440A).

Table 1 shows the measured tuning range and step of the DCO. The frequency tuning range that can be achieved with only capacitance tuning is 1.2 GHz. As a three-step coarse tuning scheme is used, the tuning range can be widened by 1 GHz under the same capacitance value. This has the effect of widening the tuning range without using extra capacitance. As a result, measured total tuning range is about 54% by coarse and fine tuning from 3 GHz to 5.2 GHz.

Figs. 14(a) and (b) show the transient simulation results of the DCO when the output frequency is 3.0 GHz and 5.2 GHz, respectively. The voltage swing is reduced as the output frequency is lower because the effective capacitance at the output of the DCO is increased. Thus, DCO current is controlled by the BIAS voltage in the DCO core in order to guarantee the oscillation in the wide range.

Fig. 15 shows the measured output spectrum of the DCO when the output frequency is 5.15 GHz. Its power level is around -17 dBm when measured through the test buffer inside the chip.

Fig. 16 shows the PVT corner simulation results of the DCO. The typical condition for the DCO is that Process, Voltage, and Temperature are TT, 1.2 V, and 27°C, respectively. The voltage swing of the DCO at the slow corner condition (SS, 1.08 V, 27°C) is reduced compared with that at the typical condition. On the other hand, the voltage swing at the fast corner condition (FF, 1.32 V, -

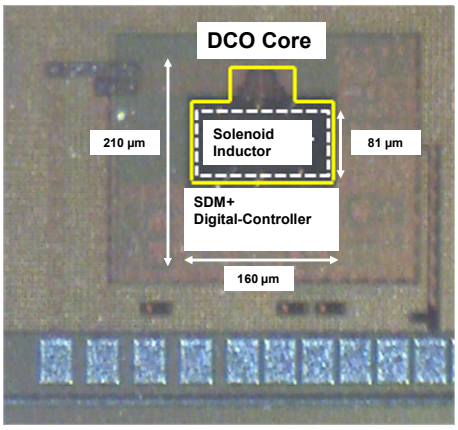

Fig. 13. Chip microphotograph.

Table 1. Measured Tuning Range and Step of the DCO.

	1st Coarse Tuning	2nd Coarse Tuning	3rd Coarse Tuning	Fine Tuning (Integer/Fractional)
Control Signal	FCONT	CAPS<9:0>	DCONT <9:0>	CDTW<63:0>/ FDTW<4:0>
Tuning Range	2.2 GHz	1.2 GHz	2.7 MHz	294 kHz/ 4.6 kHz
Tuning Step	1.1 GHz	1.2 MHz	2.6 kHz	4.6 kHz/ 0.14 kHz

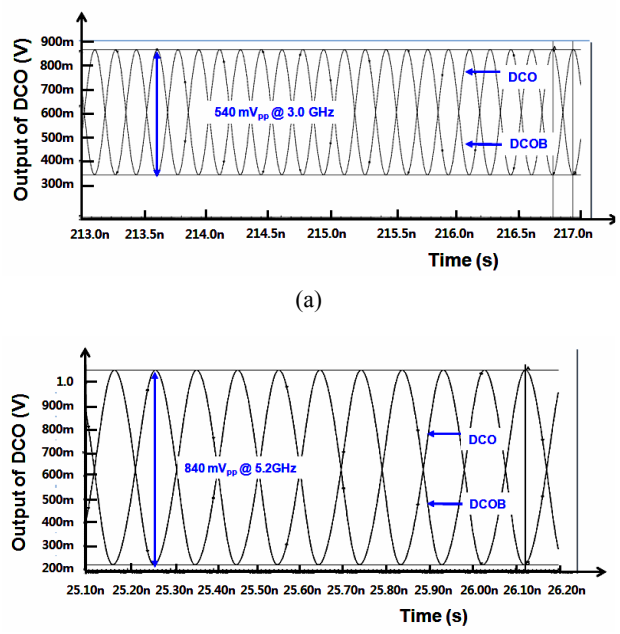

Fig. 14. Transient simulation results of the DCO when the output frequency is (a) 3.0 GHz, (b) 5.2 GHz.

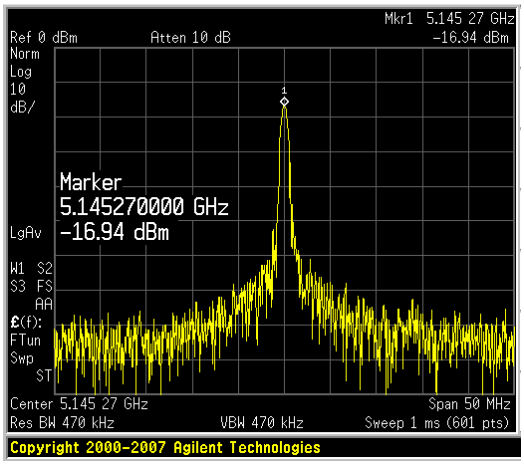

Fig. 15. Measured spectrum of the DCO.

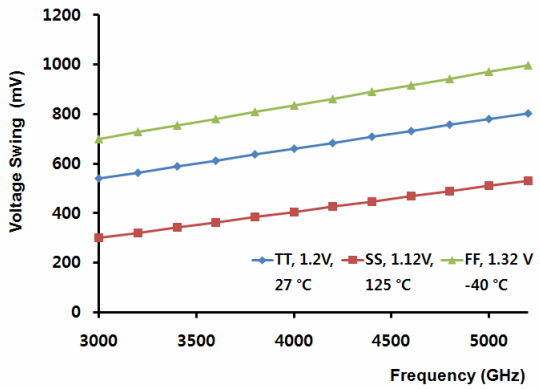

Fig. 16. PVT corner simulation results of the DCO.

40 °C) is increased compared with that at the typical condition. The BIAS level in the DCO Core can be controlled in order to adjust the voltage swing at corner cases.

The frequency resolution for the 1-LSB of the CDTW<63:0> is 4.6 kHz. Thus, the effective time-averaged frequency resolution done by the 5-bit SDM can be calculated as Eq. (2)

$$\Delta f^{\Delta\Sigma} = 4.6\,kHz/2^5 = 0.14\,kHz \tag{2}$$

From (2), the K_{DCO} is about 0.14 kHz/LSB because the frequency resolution for the 1-LSB of the DTW<68:0> is 0.14 kHz.

Fig. 17 shows that the measured phase noise is -110.61 dBc/Hz at 1 MHz offset from the carrier.

The FoM_T (figure of merit with the frequency tuning range) for the DCO can be calculated using Eq. (3).

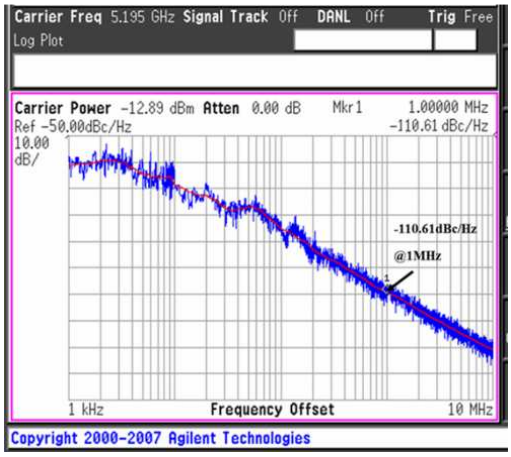

Fig. 17. The measured DCO phase noise.

Table 2. Performance Summary of the DCO.

Parameters	[3]	[6]	[7]	This work
Process	0.13 μm CMOS	0.18 μm CMOS	65 nm CMOS	0.13 μm CMOS
Inductor Type	Sprial	Sprial	Sprial	Solenoid
DCO Area (mm^2)	0.073	N/A	0.32	0.034
Supply Voltage (V)	1.5	1.8	1.8	1.2
Power Consumption (mW)	3.45	5	28.8	6.6
Center Frequency (GHz)	2.4	3.8	3	4.1
Tuning Range (%)	20.8	26.3	26	54
Frequency Resolution (kHz)	0.718	20	0.15	0.14
Phase Noise @1 MHz (dBc/Hz)	-117.0	-123	-127.5	-110.61
FoM_T (dBc/Hz)	-185.6	-194.4	-190.2	-193.1

$$FOM_T = PN\left(f_{offset}\right) - 20\log\left(\frac{f_o}{f_{offset}}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right) - 20\log\left(\frac{FDR}{10}\right) \tag{3}$$

where f_{offset} is the offset frequency, f_o is the oscillation frequency, $PN\ (f_{offset})$ is the phase noise at the f_{offset}, P_{DC} is the DC power consumption and the FDR is the frequency tuning range in a percentage.

The performance of the proposed DCO is summarized in Table 2.

The FoM_T of this work is smallest except [6], which adopted the spiral inductor for the LC DCO core, respectively. As can be seen in Fig. 6, the quality factor of the solenoid inductor is smaller than that of the spiral inductor. Also, it is smaller than that of the active inductor in [5]. Thus, the phase noise performance of this work is inferior to those of [5] and [6]. According to our

simulation, the phase noise of the DCO with the proposed solenoid inductor at the output frequency of 5 GHz is degraded by about 4 dB and 2 dB compared with those using the spiral inductor and active inductor, respectively. However, the main target of this work is to reduce the die size with small area solenoid inductor. The phase noise performance can be further improved with more die area. The proposed DCO has the smallest size thanks to the proposed solenoid inductor with the small area.

V. CONCLUSIONS

A wide band, small-area DCO with an solenoid inductor using an automatic three-step coarse and gain tuning loop is fabricated using the 0.13 μm digital CMOS process without any additional RF options. Due to the Metal stacked solenoid inductor, the chip area is remarkably reduced compared to those using a conventional spiral inductor. The tuning range of the DCO is 3 GHz - 5.2 GHz with the effective frequency resolution of 0.14 kHz. The power consumption is 6.6 mW from a 1.2 V supply. The phase noise of the DCO output at 5.195 GHz is -110.61 dBc/Hz at 1 MHz offset. Moreover, this small area LC DCO is suitable for low cost wireless PLLs.

ACKNOWLEDGMENTS

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MEST) (No. 2011-0027658).

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