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# An Analytical Model for the Threshold Voltage of Short-Channel Double-Material-Gate (DMG) MOSFETs with a Strained-Silicon (s-Si) Channel on Silicon-Germanium (SiGe) Substrates

**Shiv Bhushan[*], Santunu Sarangi[*], Gopi Krishna S.[*], Abirmoya Santra[*], Sarvesh Dubey[**], and Pramod Kumar Tiwari[*]**

*Abstract*—**In this paper, an analytical threshold voltage model is developed for a short-channel double-material-gate (DMG) strained-silicon ($\mathrm{s-Si}$) on silicon-germanium ($\mathrm{Si_{1-X}Ge_X}$) MOSFET structure. The proposed threshold voltage model is based on the so called virtual-cathode potential formulation. The virtual-cathode potential is taken as minimum channel potential along the transverse direction of the channel and is derived from two-dimensional (2D) potential distribution of channel region. The 2D channel potential is formulated by solving the 2D Poisson's equation with suitable boundary conditions in both the strained-Si layer and relaxed $\mathrm{Si_{1-X}Ge_X}$ layer. The effects of a number of device parameters like the Ge mole fraction, Si film thickness and gate-length ratio have been considered on threshold voltage. Further, the drain induced barrier lowering (DIBL) has also been analyzed for gate-length ratio and amount of strain variations. The validity of the present 2D analytical model is verified with ATLAS™, a 2D device simulator from Silvaco Inc.**

*Index Terms*—**Double-material-gate (DMG), hot carrier effect (HCE), drain induced barrier lowering (DIBL), strained-silicon ($\mathrm{s-Si}$) on silicon-germanium ($\mathrm{Si_{1-X}Ge_X}$) MOSFETs**

## I. INTRODUCTION

As the conventional MOSFET dimensions are approaching its physical limit, the acute short-channel-effects (SCE) are posing a serious threat to further scaling and following the ITRS roadmap [1, 2]. Following the rules of scaling, for a planar bulk MOSFET, continuous scaling requires continuous increase in the channel doping ($N_a$). This is because it is desired to have a lower junction electric field in the channel region [3]. Also higher doping ensures non-overlap of the source and drain depletion in the channel. But a serious effect of mobility degradation due to the impurity scattering comes in play with higher amount of channel doping [4]. Also the threshold voltage variations take place due to random dopant fluctuations inside the channel. To counter this problem, many ingenious techniques have been devised [5-8]. For example, the mobility of the charge carriers is enhanced through such a concept known as the strain technology.

In strain technology, a silicon epitaxial layer is pseudomorphically grown over the silicon-germanium layer ($\mathrm{Si_{1-X}Ge_X}$ where $\mathrm{X}$ is germanium mole fraction) which results in lattice mismatch and tensile biaxial

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[*] Department of Electronics and Communication Engineering, National Institute of Technology, Rourkela-967008, India
[**] Department of Electronics Engineering, IIT(BHU), Varanasi-221005, India
E-mail : tiwarip@nitrkl.ac.in

strain in the silicon epitaxial layer [9]. In strained Si film, the 6-fold degenerate valley in the conduction band splits into a 2-fold non planar and a 4-fold planar degenerate valleys [9]. In the same way, the valence band also splits into two band each consisting of light and heavy holes [9]. The carriers then prefer the lower energy valley while occupying them resulting in the reduction of intervalley scattering and effective mass of the carrier [9]. To sum it all, the benefits achieved are firstly a modified lattice constant of the material; second a modified energy band structure to trap carriers through well formation and finally an enhanced mobility [10]. By increasing the Ge concentration of the relaxed $Si_{1-X}Ge_X$ substrate, the amount of biaxial strain and therefore higher magnitude of the mobility enhancement can be achieved. Oberhuber *et al.* [11] *has* confirmed a mobility enhancement factor of 2.3 for a 30% Ge concentration. However, as the Ge content is increased, the critical thickness; which is the thickness to which the strained silicon can be grown without inducing misfit dislocations to alleviate strain; is reduced [12]. When strain is included in the Si channel of the MOSFET it offers better performance than the conventional MOSFETs due to its higher electron and hole mobility, high field velocity and velocity overshoot of carriers as discussed in literature [9-12]. However, the enhanced carrier mobility when coupled with high fields as in further scaled strained bulk MOSFET results in highly energetic and accelerated carriers known as the "Hot Carriers" [13, 14]. These hot carriers under the influence of the transverse field collide with the oxide, damaging the interface while itself getting trapped in the oxide region. Recently, we have analysed such a damaged strained-Si MOSFET using a two-dimensional (2D) analytical model [15].

One of the prominent means to get rid of hot carrier effect (HCE) is the gate engineering technique in which the cascaded gate structure consisting of two metals of different work functions is used. This structure is commonly known as Double-Material-Gate (DMG) structure as proposed in 1999 by Long *et al.* [16]. The two gate metals are so cascaded that the gate near the source is a metal ($M_1$) with higher work-function and the drain side metal ($M_2$) is of relatively lower workfunction. As a result of this, the electron velocity and the lateral electric field along the channel increases sharply at the interface of the two gate material which further results in the increased gate transport efficiency [17]. Li Jin et al. described how reduction of the HCE may be achieved by decreasing the control gate to screen gate ratio in a DMG strained-Si on insulator MOSFET [18, 19]. Further, the structure creates a step-like surface potential profile in the channel and thereby ensures screening of the minimum potential point from drain voltage variations. The metal gate M1 is thus rightfully known as the Control Gate and the metal M2 as the Screen Gate. Fabrication techniques for DMG CMOS [20-23] structure are reported in literature. DMG CMOS device with gate length of 55nm is already fabricated [21]. So, considering the development of the process technology over the years, the 30nm DMG MOSFET can also be fabricated in near future.

In this work, the concept of Double-Material-Gate (DMG) is incorporated in strained-silicon ( $s-Si$ ) on silicon-germanium ( $Si_{1-X}Ge_X$ ) MOSFET in order to overcome HCE and other SCEs in strained-Si MOSFET. An analytical 2D surface potential model and thereby a threshold voltage model is also developed for the proposed device. For this purpose, the 2D Poisson's equation is solved in strained-Si and relaxed $Si_{1-X}Ge_X$ using the appropriate boundary conditions along with the parabolic approximation of the channel potential profile. An extensive analysis was carried out on the surface potential and threshold voltage by various device parameters like strain, oxide and silicon thickness, gate length ratio and gate metal variations. Also, the DIBL effect on the device is well analyzed. The developed model is sufficiently backed by the simulation results obtained from the numerical simulator ATLAS™ from Silvaco Inc [24]. The simulations claim the high accuracy of the analytical model.

## II. The Modified Band Structure

Fig. 1 displays the change in silicon energy band structure because of strain in the silicon channel.

The device simulator model library of ATLAS™, thus, has been modified according to the effects of strain on Si band structure. The effects of strain on Si band structure can be modeled as [26]

$$(\Delta E_C)_{s-Si} = 0.57X \qquad (1)$$

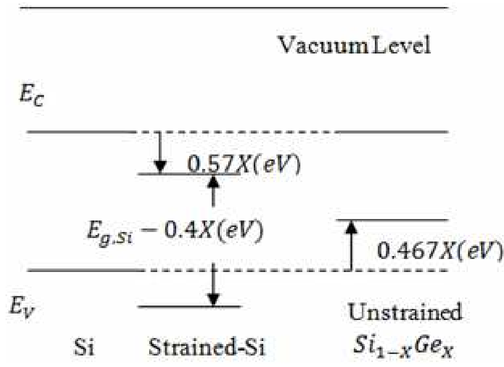


**Fig. 1.** Alternation of Band structure due to strain in $s-\mathrm{Si}$ on $\mathrm{Si_{1-X}Ge_X}$ substrate [25].

$$(\Delta E_g)_{s-Si} = 0.40X \tag{2}$$

$$V_T \ln\left(\frac{N_{v,Si}}{N_{v,s-Si}}\right) = V_T \ln\left(\frac{m^*_{h,Si}}{m^*_{h,s-Si}}\right)^{\frac{3}{2}} \approx 0.075X \tag{3}$$

where, $(\Delta E_C)_{s-Si}$ is the increase in electron affinity of silicon due to strain; $(\Delta E_g)_{s-Si}$ is the decrease in the band gap of silicon due to strain; $V_T$ is the thermal voltage ; $N_{v,Si}$ and $N_{v,s-Si}$ are the density of states in the valence band in unstrained and strained-silicon; $m^*_{h,Si}$ and $m^*_{h,s-Si}$ are the hole density of states (DOS) effective masses in unstrained and strained silicon, respectively. It should be noted that whole lump of Eq. (3) is a result of $(\phi_{f,Si} - E_{v,Si}) - (\phi_{f,s-Si} - E_{v,s-Si})$ [27], where $(\phi_{f,Si} - E_{v,Si})$ is the difference of Fermi energy level and valance band energy level of unstrained silicon and $(\phi_{f,s-Si} - E_{v,s-Si})$ is the difference of Fermi energy level and valance band energy level of strained Si; $\phi_{f,Si}$ , $E_{v,Si}$ , $\phi_{f,s-Si}$ and $E_{v,s-Si}$ are Fermi level of unstrained Si; valance band energy level of unstrained Si, Fermi level of strained Si and valance band energy level of strained Si respectively.

The energy band parameters for $\mathrm{Si_{1-X}Ge_X}$ substrate have been estimated as follows [26]

$$(\Delta E_g)_{SiGe} = 0.467X \tag{4}$$

$$N_{v,SiGe} = \left(0.6x + 1.04(1-X)\right) \times 10^{19}\,\mathrm{cm^{-3}} \tag{5}$$

$$\varepsilon_{SiGe} = 11.8 + 4.2\mathrm{X} \tag{6}$$

where, $(\Delta E_g)_{\mathrm{SiGe}}$ is the decrease in the band gap of $\mathrm{Si_{1-X}Ge_X}$; $N_{v,\mathrm{SiGe}}$ the density of states in the valence band of the relaxed $\mathrm{Si_{1-X}Ge_X}$ film and $\varepsilon_{SiGe}$ is the permittivity of the $\mathrm{Si_{1-X}Ge_X}$.

The effect of strain on front-channel flat-band voltage can be modeled as

$$\left(V_{FB,f}\right)_{\mathrm{s-Si}} = \left(V_{FB,f}\right)_{Si} + \Delta V_{FB,f} \tag{7}$$

where,
$$\left(V_{FB,f}\right)_{Si} = \varphi_M - \phi_{(Si)} \tag{8}$$

$$\Delta V_{FB,f} = -\frac{(\Delta E_C)_{s-Si}}{q} - \frac{(\Delta E_g)_{s-Si}}{q} - V_T \ln\frac{N_{V,Si}}{N_{V,s-Si}} \tag{9}$$

$\varphi_M$ and $q$ are the metal work function and electronic charge of the silicon, respectively; $\left(V_{FB,f}\right)_{Si}$ represents the flat band voltage for a bulk MOSFET; $\left(V_{FB,f}\right)_{s-Si}$ represents the flat band voltage for the strained bulk MOSFET and $\Delta V_{FB,f}$ represents the amount of change in the bulk flat band voltage due to strain.

$$\phi_{(Si)} = \frac{\chi_{Si}}{q} + \frac{E_{g,Si}}{2q} + \phi_{f,Si} \tag{10}$$

$$\phi_{f,Si} = V_T \ln\left(\frac{N_a}{n_{i,\mathrm{Si}}}\right) \tag{11}$$

where, $\phi_{(Si)}$ is the unstrained Si work function; $\chi_{Si}$ is electron affinity of the silicon; $E_{g,Si}$ is the band gap of unstrained Si; $\phi_{f,Si}$ is the Fermi potential in unstrained Si; $N_a$ is the body doping concentration; and $n_{i,Si}$ is the intrinsic carrier concentration in unstrained Si.

The built-in voltage across the source-body and drain-body junctions in the strained-Si thin film is also affected by strain as

$$V_{bi,s-Si} = V_{bi,Si} + \left(\Delta V_{bi}\right)_{s-Si} \tag{12}$$

where,
$$V_{bi,Si} = \frac{E_{g,Si}}{2q} + \phi_{f,Si} \tag{13}$$

$$\left(\Delta V_{bi}\right)_{\mathrm{s-Si}} = \frac{-(\Delta E_g)_{s-Si}}{q} - V_T \ln\frac{N_{V,Si}}{N_{V,s-Si}} \tag{14}$$

where, $V_{bi,Si}$ is the unstrained Si built in potential and $(\Delta V_{bi})_{s-Si}$ is the change in built in potential due to strain in the strained channel and source (drain) interface.

The built-in voltage across the source-body and drain-body junctions in the relaxed $Si_{1-X}Ge_X$ substrate can be written as,

$$V_{bi,SiGe} = V_{bi,Si} + (\Delta V_{bi})_{SiGe} \tag{15}$$

$$V_{bi,Si} = \frac{E_{g,Si}}{2q} + \phi_{f,Si} \tag{16}$$

$$(\Delta V_{bi})_{SiGe} = \frac{-(\Delta E_g)_{SiGe}}{q} - V_T \ln \frac{N_{V,Si}}{N_{V,s-Si}} \tag{17}$$

where, $(\Delta V_{bi})_{SiGe}$ is the change in built potential due to strain in $Si_{1-X}Ge_X$ substrate and source (drain) interface.

## III. Device Structure

Fig. 2(a) shows the cross-section of a short channel DMG strained-Si on $Si_{1-X}Ge_X$ MOSFET along with the depletion region of the device. Device dimensions, doping and other parameters are defined in Table 1.

As shown in Fig. 2(a), the depletion region under the gate is non-uniform caused by the lateral source-body and drain-body depletion widths $x_{dl}$ .

In such a case, the development of an analytical model through the exact solution of the 2D Poisson equation will be highly challenging and would require employment of numerical methods and iterations. To develop a simple analytical solution, device structure of Fig. 2(a) is altered into a box type approximation of the depletion region as shown in Fig. 2(b) consisting of a uniform depletion thickness of $x_d$ and a uniform doping density of $N_{a,eff}$ .

J. Kumar *et al.* [26] have used some geometric approximations to find the effective channel doping and the depletion thickness of the channel in the MOSFET. Following the same approach, the effective doping concentration due to the box approximation can be written as

$$N_{a,eff} = N_a \left[ 1 - \left( \left( 1 + \frac{2x_{dv}}{r_j} \right)^{\frac{1}{2}} - 1 \right) \frac{r_j}{L} \right] \tag{18}$$

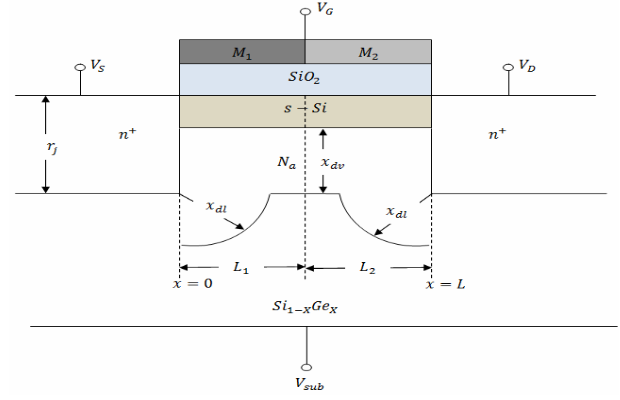


**Fig. 2(a).** Cross sectional view of DMG MOSFET with $s-Si$ channel on $Si_{1-X}Ge_X$ substrate.

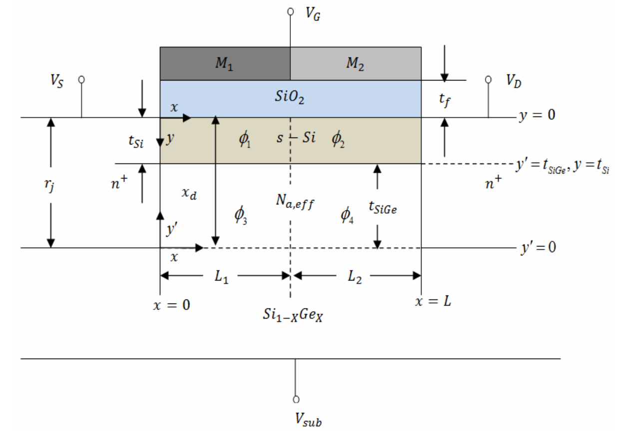


**Fig. 2(b).** Box approximation of the depletion region of DMG MOSFET with $s-Si$ channel on $Si_{1-X}Ge_X$ substrate.

where,

$$x_{dv} = \sqrt{\frac{2\varepsilon_{SiGe}(\phi_{th} - V_{sub})}{qN_a}} \tag{19}$$

$$\phi_{th} = 2\phi_{f,Si} + \Delta\phi_{(s-Si)} \tag{20}$$

$$\Delta\phi_{(s-Si)} = \frac{-(\Delta E_g)_{s-Si}}{q} - V_T \ln \frac{N_{V,Si}}{N_{V,s-Si}} \tag{21}$$

where, $x_{dv}$ is vertical depletion widths: $\phi_{th}$ is that value of surface potential at which the inversion charge density in the strained-Si device is same as that in the unstrained-Si at threshold; $\Delta\phi_{(s-Si)}$ is change in unstrained Si workfunction due to strain and $V_{sub}$ is substrate bias voltage.

The depletion region thickness is given as

**Table 1.** Symbols description used in the device structure

| | |
|---|---|
| Gate Oxide Thickness | $t_f$ |
| Strained Silicon layer Thickness | $t_{Si}$ |
| Effective $Si_{1-X}Ge_X$ Thickness | $t_{SiGe}$ |
| Control Gate Length | $L_1$ |
| Screen Gate Length | $L_2$ |
| Gate Length | $L = L_1 + L_2$ |
| Source/Drain junction depth | $r_j$ |
| Depletion Depth | $x_d$ |
| Work function of Control Gate | $\varphi_{M1}$ |
| Work function of Screen Gate | $\varphi_{M2}$ |
| Control Gate Potential | $\phi_1, \phi_3$ |
| Screen Gate Potential | $\phi_2, \phi_4$ |
| Ge Mole fraction in $Si_{1-x}Ge_x$ Layer | $X$ |
| Source and Drain Doping | $N_d$ |
| Body Doping | $N_a$ |
| Substrate Bias | $V_{sub}$ |
| Gate to Source Voltage | $V_{gs}$ |
| Drain to Source Voltage | $V_{ds}$ |
| Substrate | $Si_{1-X}Ge_X$ |

$$x_d \cong \frac{2x_{dl}\left(r_j + \frac{\pi}{4}x_{dl}\right) + \left(L - 2x_{dl}\right)x_{dv}}{L} \quad \text{for} \quad L \geq 2x_{dl} \tag{22}$$

and

$$x_d \cong r_j + \left(x_{dl}^2 - \frac{L^2}{4}\right)^{\frac{1}{2}} + \frac{\theta}{2}x_{dl} \quad \text{for} \quad L \leq 2x_{dl} \tag{23}$$

where, $\theta = \sin^{-1}\left(\frac{L}{2x_{dl}}\right)$ and $x_{dl} = \sqrt{\frac{2\varepsilon_{SiGe}V_{bi,SiGe}}{qN_a}}$ (24)

where, $x_{dl}$ is the lateral depletion widths; $r_j$ is the source and drain depth and $L$ is total channel length.

Considering all the above approximations, the modified device structure is shown in Fig. 2(b). As shown, the depletion region is divided into four regions represented by regions 1 and 3 under metal $M_1$ and regions 2 and 4 under metal $M_2$. Regions 1 and 2 represent the s-Si layer whereas regions 3 and 4 represent the relaxed $Si_{1-X}Ge_X$ layer.

## IV. SURFACE POTENTIAL MODELING

To find out the potential distribution $\phi_i(x, y)$ in the channel region, the following 2D Poisson's equations have been solved in all the four regions of strained-Si and the relaxed $Si_{1-X}Ge_X$ layers

$$\frac{\partial^2\phi_i(x,y)}{\partial x^2} + \frac{\partial^2\phi_i(x,y)}{\partial y^2} = \frac{qN_{a,eff}}{\varepsilon_{Si}} \quad \text{with} \quad i = 1,2 \tag{25}$$

$$\frac{\partial^2\phi_i(x,y)}{\partial x^2} + \frac{\partial^2\phi_i(x,y)}{\partial y^2} = \frac{qN_{a,eff}}{\varepsilon_{SiGe}} \quad \text{with} \quad i = 3,4\,. \tag{26}$$

For the $s-Si$ layer the y co-ordinate points downwards whereas for $Si_{1-X}Ge_X$ layer, $y$ -coordinate is considered at $y'$ pointing upwards as shown in Fig. 2(b). The subscript $i$ in the Eqs. (25) and (26) denotes the respective channel regions as $i$ takes the numerical values 1, 2 3 and 4; $N_{a,eff}$ is the effective body doping concentration; $q$ is the electronic charge; $\varepsilon_{Si}$ and $\varepsilon_{SiGe}$ are the permittivity of strained-Si film and relaxed $Si_{1-X}Ge_X$. The potential distributions in all the four regions are approximated by parabolic polynomials as [28]

$$\phi_i(x,y) = \phi_{si}(x) + C_{i1}(x)y + C_{i2}(x)y^2 \quad i = 1,2 \tag{27}$$

$$\phi_i(x,y') = V_{sub} + C_{i1}(x)y' + C_{i2}(x)y'^2 \quad i = 3,4 \tag{28}$$

Here, $\phi_{si}(x)$ is the surface potential at $SiO_2/s-Si$ interface under both metals $M_1$ and $M_2$. The coefficients $C_i$ are the functions of $x$ only. $V_{sub}$ is the substrate bias usually taken to be zero [26]. The continuity of potential and electric field across the interface of regions 1 and 2 are:

$$\phi_1(L_1, 0) = \phi_2(L_1, 0) \tag{29}$$

$$\phi_3(L_1, 0) = \phi_4(L_1, 0) \tag{30}$$

$$\left[\frac{\partial \phi_1(x,y)}{\partial x}\right]_{x=L_1} = \left[\frac{\partial \phi_2(x,y)}{\partial x}\right]_{x=L_1} \quad (31)$$

$$\left[\frac{\partial \phi_3(x,y')}{\partial x}\right]_{x=L_1} = \left[\frac{\partial \phi_4(x,y')}{\partial x}\right]_{x=L_1} \quad (32)$$

The electric flux at $SiO_2$/s-Si interface should be continuous in both regions 1 and 2:

$$\left[\frac{\partial \phi_1(x,y)}{\partial y}\right]_{y=0} = \frac{\varepsilon_f}{\varepsilon_{Si}} \frac{\phi_{s1}(x) - V_{g1}}{t_f} \quad (33)$$

$$\left[\frac{\partial \phi_2(x,y)}{\partial y}\right]_{y=0} = \frac{\varepsilon_f}{\varepsilon_{Si}} \frac{\phi_{s1}(x) - V_{g2}}{t_f} \quad (34)$$

where $\varepsilon_f$ the permittivity of the $SiO_2$, $t_f$ is the thickness of front gate oxide.

$$V_{g1} = V_{gs} - (V_{FB1,f})_{s-Si} \quad \text{where} \quad (V_{FB1,f})_{s-Si} = \varphi_{M1} - \phi_{(Si)} \quad (35)$$

$$V_{g2} = V_{gs} - (V_{FB2,f})_{s-Si} \quad \text{where} \quad (V_{FB2,f})_{s-Si} = \varphi_{M2} - \phi_{(Si)} \quad (36)$$

where, $V_{gs}$ as the gate to source voltage; $V_{g1}$ and $V_{g2}$ are the effective gate voltage of control gate and the screen gate at the $s-Si/SiO_2$ interface; $(V_{FB1,f})_{s-Si}$ is the flat-band voltage for control gate and $(V_{FB2,f})_{s-Si}$ is the flat-band voltage for screen gate. $\varphi_{M1}$ and $\varphi_{M2}$ represents the metal work functions of the control gate and the screen gate.

Electric field at the bottom edge of depletion region (in regions 3 and 4) is zero and can be written as

$$\left[\frac{\partial \phi_3(x,y')}{\partial y'}\right]_{y'=0} = 0 \quad (37)$$

$$\left[\frac{\partial \phi_4(x,y')}{\partial y'}\right]_{y'=0} = 0 \quad (38)$$

The potential and electric field at the $s-Si$ / $Si_{1-X}Ge_X$ interface should be equal and continuous, respectively, as

$$\phi_1(x, t_{Si}) = \phi_3(x, t_{SiGe}) \quad (39)$$

$$\left[\frac{\partial \phi_1(x,y)}{\partial y}\right]_{y=t_{Si}} = -\frac{\varepsilon_{SiGe}}{\varepsilon_{Si}} \left[\frac{\partial \phi_3(x,y')}{\partial y'}\right]_{y'=t_{SiGe}} \quad (40)$$

$$\phi_2(x, t_{Si}) = \phi_4(x, t_{SiGe}) \quad (41)$$

$$\left[\frac{\partial \phi_2(x,y)}{\partial y}\right]_{y=t_{Si}} = -\frac{\varepsilon_{SiGe}}{\varepsilon_{Si}} \left[\frac{\partial \phi_4(x,y')}{\partial y'}\right]_{y'=t_{SiGe}} \quad (42)$$

The potentials at the source and drain end can be given by

$$\phi_1(0,0) = V_{bi,s-Si} \quad (43)$$

$$\phi_2(0,L) = V_{bi,s-Si} + V_{ds} \quad (44)$$

$$\phi_3(0,0) = V_{bi,SiGe} \quad (45)$$

$$\phi_4(0,L) = V_{bi,SiGe} + V_{ds} \quad (46)$$

where, $V_{ds}$ is drain-to-source voltage.

The coefficients $C_{i1}(x)$ and $C_{i2}(x)$ appeared in Eqs. (27) and (28) has been obtained by using the boundary conditions from Eqs. (29) to (46):

$$C_{11}(x) = \frac{C_f}{\varepsilon_{Si}}(\phi_{s1}(x) - V_{g1}) \quad (47)$$

$$C_{12}(x) = -\frac{1}{2(C_{SiGe}+C_{Si})t_{Si}^2}\left[\phi_{s1}(x)\frac{\left(C_f C_{Si} + 2C_{Si}C_{SiGe} + 2C_f C_{SiGe}\right)}{C_{Si}} - 2\phi_{s3}(x)C_{SiGe} - \frac{(2C_f C_{SiGe} + C_f C_{Si})}{C_{Si}}V_{g1}\right] \quad (48)$$

$$C_{21}(x) = \frac{C_f}{\varepsilon_{Si}}(\phi_{s2}(x) - V_{g2}) \quad (49)$$

$$C_{22}(x) = -\frac{1}{2(C_{SiGe}+C_{Si})t_{Si}^2}\left[\phi_{s2}(x)\frac{\left(C_f C_{Si} + 2C_{Si}C_{SiGe} + 2C_f C_{SiGe}\right)}{C_{Si}} - 2\phi_{s4}(x)C_{SiGe} - \frac{(2C_f C_{SiGe} + C_f C_{Si})}{C_{Si}}V_{g2}\right] \quad (50)$$

$$C_{31}(x) = 0 \quad (51)$$

$$C_{32}(x) = -\frac{C_{Si}}{2(C_{SiGe}+C_{Si})t_{SiGe}^2}\left[2\phi_{s3}(x) - \frac{(2C_{Si}+C_f)}{C_{Si}}\phi_{s1}(x) + \frac{C_f}{C_{Si}}V_{g1}\right] \quad (52)$$

$$C_{41}(x) = 0 \quad (53)$$

$$C_{42}(x) = -\frac{C_{Si}}{2(C_{SiGe}+C_{Si})t_{SiGe}^2}\left[2\phi_{s4}(x) - \frac{(2C_{Si}+C_f)}{C_{Si}}\phi_{s2}(x) + \frac{C_f}{C_{Si}}V_{g2}\right] \quad (54)$$

where, $C_f = \frac{\varepsilon_{ox}}{t_f}$, $C_{Si} = \frac{\varepsilon_{Si}}{t_{Si}}$, $C_{SiGe} = \frac{\varepsilon_{SiGe}}{t_{SiGe}}$ are front gate oxide, strained-Si, relaxed $Si_{1-X}Ge_X$ layer capacitances respectively.

Utilizing Eq. (27), (28) and boundary conditions of Eq. (29)-(46) into Eq. (25) and (26), one dimensional

differential equation for surface potential, $\phi_{si}(x)$, can be written as

$$\frac{\partial^2 \phi_{si}(x)}{\partial x^2} - P\phi_{si}(x) = Q_i \tag{55}$$

where, $P = \dfrac{\alpha_1\alpha_2 - \beta_1\beta_2}{\alpha_1 + \alpha_2}$ (56)

$$Q_1 = \frac{\alpha_2\gamma_1 + \beta_1\gamma_3}{\alpha_1 + \alpha_2} \tag{57}$$

$$Q_2 = \frac{\alpha_2\gamma_2 + \beta_1\gamma_4}{\alpha_1 + \alpha_2} \tag{58}$$

$$\alpha_1 = \alpha_2 = \frac{2C_{SiGe}C_{Si} + 2C_f C_{SiGe} + C_f C_{Si}}{C_{Si}(C_{SiGe} + C_{Si})t_{Si}^2} \tag{59}$$

$$\beta_1 = \beta_2 = \frac{2C_{SiGe}}{\left(C_{SiGe} + C_{si}\right)t_{si}^2} \tag{60}$$

$$\gamma_1 = \frac{qN_a}{\varepsilon_{Si}} - \frac{C_f(2C_{Sige} + C_{Si})V_{g1}}{C_{Si}(C_{Sige} + C_{Si})t_{Si}^2} \tag{61}$$

$$\gamma_2 = \frac{qN_a}{\varepsilon_{Si}} - \frac{C_f(2C_{SiGe} + C_{Si})V_{g2}}{C_{Si}(C_{SiGe} + C_{Si})t_{Si}^2} \tag{62}$$

$$\alpha_3 = \alpha_4 = \frac{2C_{Si}}{\left(C_{SiGe} + C_{Si}\right)t_{SiGe}^2} \tag{63}$$

$$\beta_3 = \beta_4 = \frac{2C_{Si} + C_f}{\left(C_{SiGe} + C_{Si}\right)t_{SiGe}^2} \tag{64}$$

$$\gamma_3 = \frac{qN_a}{\varepsilon_{SiGe}} + \frac{C_f C_{SiGe} V_{g1}}{C_{SiGe}(C_{SiGe} + C_{Si})t_{SiGe}^2} \tag{65}$$

$$\gamma_4 = \frac{qN_a}{\varepsilon_{SiGe}} + \frac{C_f C_{SiGe} V_{g2}}{C_{SiGe}(C_{SiGe} + C_{Si})t_{SiGe}^2} \tag{66}$$

Solution of Eq. (55) yields following expression for surface potential, $\phi_{si}(x)$ [29]

$$\phi_{s1} = \frac{\psi_{d1}\sinh(\lambda x) - \psi_{s1}\sinh\left(\lambda(x - L_1)\right)}{\sinh(\lambda L_1)} - \sigma_1 \tag{67}$$

$$\phi_{s2} = \frac{\psi_{d2}\sinh\left(\lambda(x - L_1)\right) - \psi_{s2}\sinh\left(\lambda(x - L)\right)}{\sinh(\lambda L_2)} - \sigma_2 \tag{68}$$

$$\lambda = \sqrt{P} \tag{69}$$

$$\sigma_i = \frac{Q_i}{P} \tag{70}$$

$$\psi_{s1} = V_{bi,s\text{-}Si} + \sigma_1 \tag{71}$$

$$\psi_{d2} = V_{bi,s\text{-}Si} + V_{ds} + \sigma_2 \tag{72}$$

$$\psi_{d1} = V_p + \sigma_1 \tag{73}$$

$$\psi_{s2} = V_p + \sigma_2 \tag{74}$$

$$V_p = \frac{\psi_{d2}\operatorname{cosech}(\lambda L_1) + \psi_{s1}\operatorname{cosech}(\lambda L_1) - \sigma_1\coth(\lambda L_1) - \sigma_2\coth(\lambda L_2)}{\coth(\lambda L_1) + \coth(\lambda L_2)} \tag{75}$$

where, $\psi_{s1}, \psi_{s2}, \psi_{d1}, \psi_{d2}, \sigma_1$ and $\sigma_2$ are the constants and $\lambda$ is the characteristic length associated with the surface potential.

The position $x_{\min}$ of the so called virtual cathode (the minimum surface potential) lies under the control gate [30] is estimated by solving $\left(\dfrac{\partial\phi_{s1}(x)}{\partial x}\right)_{x=x_{\min}} = 0$ and is determined as

$$x_{\min} = \frac{1}{2\alpha}\ln\left(\frac{b_1}{a_1}\right) \tag{76}$$

where, $a_1 = \dfrac{-1}{2\sinh(\lambda L_1)}\left[\psi_{s1}e^{-\lambda L_1} - \psi_{d1}\right]$ (77)

and $b_1 = \dfrac{-1}{2\sinh(\lambda L_1)}\left[-e^{\lambda L_1}\psi_{s1} + \psi_{d1}\right]$ (78)

Now, the minimum surface potential or virtual cathode potential, $\phi_{s1,\min}$ under the control gate region can be obtained by putting Eq. (76) into Eq. (67) as

$$\phi_{s1,\min} = 2\sqrt{a_1 b_1} - \sigma_1 \tag{79}$$

## V. Threshold Voltage Modeling

For an unstrained-Si MOSFET, the threshold voltage $V_{th}$ is defined as that value of the gate voltage $V_{gs}$ at which a conduction channel is induced under the gate oxide. Therefore, in a conventional unstrained-Si MOSFET, the threshold voltage is taken to be that value of the gate-source voltage at which the virtual cathode potential equals twice the difference between the extrinsic Fermi level in the bulk and the intrinsic Fermi level of silicon (i.e. $\phi_{s,\min} = 2\phi_{f,Si}$ where, $\phi_{s,\min}$ is minimum surface potential ) [30].

For the DMG strained-Si on $Si_{1-X}Ge_X$ MOSFET, the threshold condition is modified as in [27]

$$\phi_{s1,\min} = 2\phi_{f,Si} + \Delta\phi_{(s-Si)} = \phi_{th} \quad (80)$$

Hence, we can determine the value of the threshold voltage ($V_{th}$) by substituting Eq. (79) into Eq. (80) and solving for $V_{gs} = V_{th}$ as

$$V_{th} = \frac{-\eta + \sqrt{\eta^2 - 4\text{P}\xi}}{2\text{P}} \quad (81)$$

$$\text{P} = V_1 V_2 - n^2 \quad (82)$$

$$\eta = U_2 V_1 + U_1 V_2 - 2nl \quad (83)$$

$$\xi = U_1 U_2 - l^2 \quad (84)$$

$$U_1 = \frac{(V_{P11} + m_1 - (V_{bi,s-Si} + m_1)\exp(-\lambda L_1))}{\sinh(\lambda L_1)} \quad (85)$$

$$V_1 = \frac{(V_{P12} + n(1 - \exp(-\lambda L_1))}{\sinh(\lambda L_1)} \quad (86)$$

$$U_2 = \frac{(V_{bi,s-Si} + m_1)\exp(\lambda L_1) - (V_{P11} + m_1)}{\sinh(\lambda L_1)} \quad (87)$$

$$V_2 = \frac{n(\exp(\lambda L_1) - 1) - V_{P12}}{\sinh(\lambda L_1)} \quad (88)$$

$$l = \phi_{th} + m_1 \quad (89)$$

$$V_{P11} = \frac{1}{U_3}\left[\begin{matrix}(\cos ech(\lambda L_1) - \coth(\lambda L_1))m_1 + (\cos ech(\lambda L_2) - \coth(\lambda L_2))m_2 \\ + \cos ech(\lambda L_1)V_{bi,s-Si} + (V_{bi,s-Si} + V_{ds})\cos ech(\lambda L_2)\end{matrix}\right] \quad (90)$$

$$V_{P12} = \frac{n}{U_3}\left[\cos ech(\lambda L_1) + \cos ech(\lambda L_2) - \coth(\lambda L_2) - \coth(\lambda L_1)\right] \quad (91)$$

$$U_3 = \coth(\lambda L_1) + \coth(\lambda L_2) \quad (92)$$

$$m_1 = \frac{\alpha_2 A_1 + \beta_1 C_1}{\alpha^2 - \beta^2} \quad (93)$$

$$m_2 = \frac{\alpha_2 A_2 + \beta_1 C_2}{\alpha^2 - \beta^2} \quad (94)$$

$$n = \frac{\beta_1 D - \alpha_2 B}{\alpha^2 - \beta^2} \quad (95)$$

$$B = \frac{C_f(2C_{SiGe} + C_{Si})}{C_{Si}(C_{SiGe} + C_{Si})t_{Si}^2} \quad (96)$$

$$D = \frac{C_f}{(C_{SiGe} + C_{Si})t_{SiGe}^2} \quad (97)$$

$$A_1 = \frac{qN_a}{\varepsilon_{Si}} + \frac{C_f(2C_{SiGe} + C_{Si})(V_{FB1,f})_{s-Si}}{C_{Si}(C_{SiGe} + C_{Si})t_{Si}^2} \quad (98)$$

$$A_2 = \frac{qN_a}{\varepsilon_{Si}} + \frac{C_f(2C_{SiGe} + C_{Si})(V_{FB2,f})_{s-Si}}{C_{Si}(C_{SiGe} + C_{Si})t_{Si}^2} \quad (99)$$

$$C_1 = \frac{qN_a}{\varepsilon_{SiGe}} - \frac{C_f(V_{FB1,f})_{s-Si}}{(C_{SiGe} + C_{Si})t_{SiGe}^2} \quad (100)$$

$$C_2 = \frac{qN_a}{\varepsilon_{SiGe}} - \frac{C_f(V_{FB2,f})_{s-Si}}{(C_{SiGe} + C_{Si})t_{SiGe}^2} \quad (101)$$

## VI. Simulation Method and Models

The numerical simulations are carried out by a 2D numerical simulator named ATLAS™ from Silvaco Inc [24]. The drift-diffusion model (DD) model has been used for carrier transportation because of its validity in the subthreshold regime even for channel length less than 30 nm [31-33]. The CVT mobility model is used as it is a complete mobility model in which mobility depends on doping density, temperature, parallel electric field and vertical electric field. Following [33], ATLAS default model parameter *beta* and *vsat.n* have also been modified by setting *beta*=1 and $vsat.n = \frac{1.5L + 21.6}{L + 2.7} \times 10^7$ cm/s (where $L$ is in nanometer). Fermi-Dirac carrier statistical model is employed to minimize carrier concentrations in the heavily doped regions [24]. To incorporate the effects of strain in Si, model parameters of silicon are modified according to Ref. [26]. The modified parameters for different mole fraction (X) are given in Table 2.

Following the constant current method of threshold voltage extraction, $V_{th}$ is obtained from the drain current-gate voltage curve by considering the value of the gate voltage at drain current magnitude given by $I_d = \frac{W}{L} \times 10^{-7}$ A/μm, where $W$ and $L$ are width and length of the channel, respectively [34]. The work function for the control gate is $\varphi_{M1} = 4.71$ eV (Rh:

**Table 2.** Modified parameter values of silicon due to strain (x). Eg (300) represents energy bandgap of Si at 300 K; NC (300) represents the conduction band density of states of Si at 300 K and Nv (300) represents the valence band density of states of Si at 300 K

| Parameter | $X = 0$ | $X = 0.1$ | $X = 0.2$ | $X = 0.3$ |
|---|---|---|---|---|
| $E_g$300 (eV) | 1.08 | 1.04 | 1.00 | 0.96 |
| Nc300 (cm$^{-3}$) | 2.80 x $10^{19}$ | 2.25 x $10^{19}$ | 1.98 x $10^{19}$ | 1.95 x $10^{19}$ |
| NV300 (cm$^{-3}$) | 1.04 x $10^{19}$ | 7.80 x $10^{18}$ | 5.85 x $10^{18}$ | 4.39 x $10^{18}$ |
| Permittivity | 11.8 | 11.8 | 11.8 | 11.8 |
| Mobility (cm$^2$/V.sec) | 1400 | 1800 | 2250 | 2305 |
| Affinity (eV) | 4.17 | 4.23 | 4.28 | 4.34 |
| ni (cm$^{-3}$) | 1.45 x $10^{10}$ | 2.44 x $10^{10}$ | 4.29 x $10^{10}$ | 7.99 x $10^{10}$ |

Rhenium). In different cases, three different metals are taken with work functions $\varphi_{M2} = 4.6$ eV (Mo: Molybdenum), 4.4 eV (W: Tungsten) and 4.2 eV (Al: Aluminium) for the screen gate.

## VII. Result and Discussion

In this section, results obtained from theoretical models of surface potential and threshold voltage are compared with the numerical simulation results. Fig. 3 shows the surface potential profiles for single-material-gate (SMG) $s-Si$ and DMG $s-Si$ on $Si_{1-X}Ge_X$ MOSFETs structures. For the DMG structure, the screen gate workfunction is varied keeping the control gate workfunction same for all the cases. As the screen gate work function decreases, the minimum surface potential increases, reducing the source-channel barrier height and thereby decreasing the threshold voltage. Also, as the screen gate work function decreases the minimum surface potential shifts towards the source-side which then increasingly becomes immune to the drain voltage changes (i.e. lower drain induced barrier lowering (DIBL)). So, for $\varphi_{M2} = 4.2$ eV , the source-channel barrier height is minimum but is highly immune to DIBL when compared to SMG structure. For $\varphi_{M2} = 4.6$ eV , the barrier height is more compared to the case when $\varphi_{M2}$ was 4.2 eV but device is susceptible to DIBL.

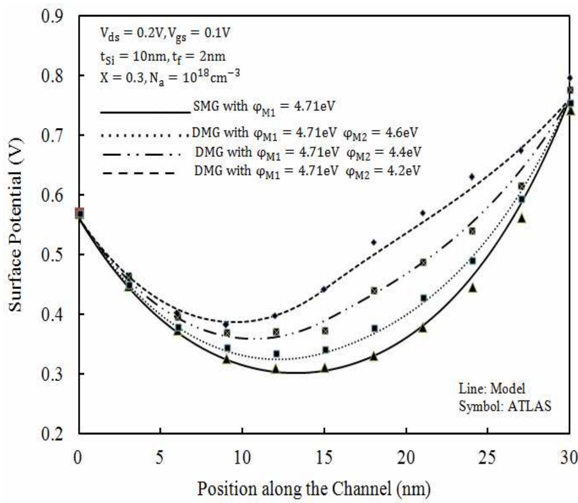


**Fig. 3.** Comparison of surface potential of Single Material Gate(SMG), and DMG (with different metal work function) strained MOSFETS against position along the channel length. Parameters used: $X = 0.3$, $V_{ds} = 0.2$ V, $V_{gs} = 0.1$ V, $V_{sub} = 0$ V, $L = 30$ nm, $t_{Si} = 10$ nm, $N_a = 1\times10^{18}$ cm$^{-3}$, $t_f = 2$ nm.

Fig. 4 shows surface potential variations along the channel length ($L$) for different control-to-screen gate length ratios ($L_1 : L_2$). The step profile in the surface potential of the DMG $s-Si$ on $Si_{1-X}Ge_X$ MOSFET enhances the immunity of the device against undesired variations in the drain-to-source voltage ($V_{ds}$) by screening it effectively. It is observed that as the screen gate length increases, the minimum surface potential increases leading to decrease in the channel barrier height. Also, the minimum surface potential point shifts towards the source side decreasing the influence of the drain on it. In other words, the device with equal control and screen gate length will be the optimized device in terms of $V_{ds}$ immunity and barrier height.

Li Jin *et. al* [18] showed that as $L_2$ increases, the point of peak electric field in the channel shifts toward the source end causing more uniformity of the electric field in the channel and improving carrier drift velocity and device speed. The increased carrier transport efficiency with decreasing $L_1$ causes lower HCE and improved DIBL.

Fig. 5 shows the channel potential variation along the channel length for different values of $V_{ds}$ and Ge mole

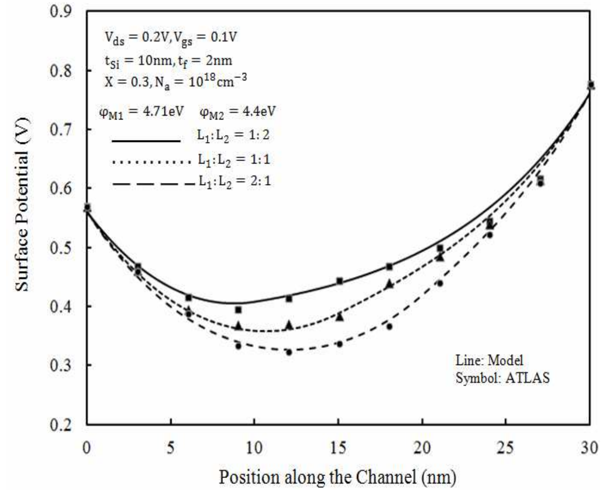


**Fig. 4.** Comparison of surface potential of DMG strained MOSFET against position along the channel length for different gate length ratios $(L_1 : L_2)$. Parameters used: $X = 0.3$, $V_{ds} = 0.2$ V, $V_{gs} = 0.1$ V, $V_{sub} = 0$ V, $L = 30$ nm, $N_a = 1\times 10^{18}$ cm$^{-3}$, $t_f = 2$ nm, $t_{Si} = 10$ nm, $\varphi_{M1} = 4.71$eV and $\varphi_{M2} = 4.4$eV.

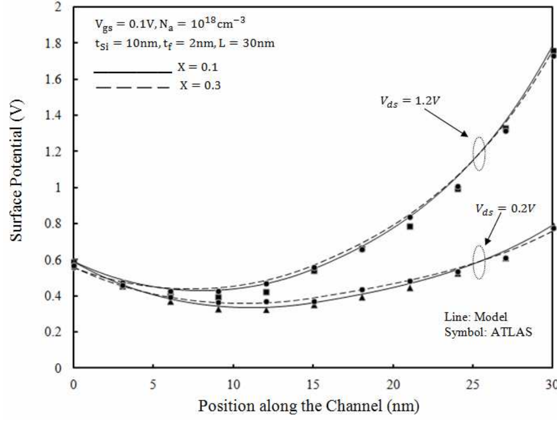


**Fig. 5.** Surface potential variation along the channel length for fixed gate length ratios $(L_1 : L_2) = 1:1$ for different Ge mole fractions X and for different $V_{ds}$ in the $Si_{1-X}Ge_X$ layer. Parameters used: $V_{gs} = 0.1$V, $V_{sub} = 0$V, $L = 30$ nm, $N_a = 1\times 10^{18}$ cm$^{-3}$, $t_f = 2$ nm, $t_{Si} = 10$ nm, $\varphi_{M1} = 4.71$eV and $\varphi_{M2} = 4.4$eV.

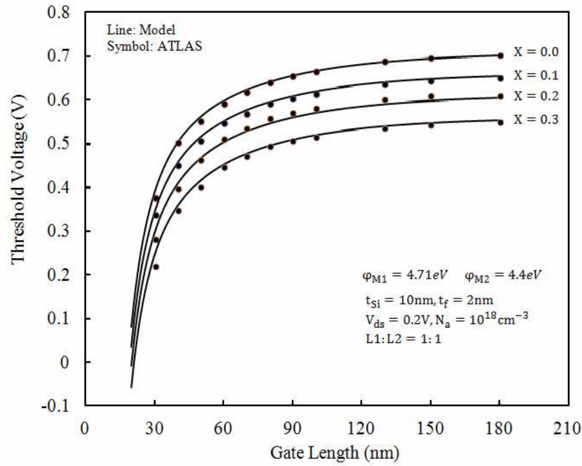


**Fig. 6.** Threshold voltage against device channel length $(L)$ for different Ge mole fraction $X$ in the $Si_{1-X}Ge_X$ layer, Parameters used: $V_{ds} = 0.2$V, $V_{sub} = 0$V, $N_{a,eff} = 1\times 10^{18}$ cm$^{-3}$, $t_f = 2$ nm, $t_{Si} = 10$ nm, $L_1 : L_2 = 1:1$, $\varphi_{M1} = 4.71$eV and $\varphi_{M2} = 4.4$eV.

fraction ( X ). For a fixed amount of mole fraction, the minimum potential rises with the rise in $V_{ds}$ showing the drain influence over it at a short channel length.

Fig. 6 shows the threshold voltage variations against different gate length for different values of Ge mole fraction. As evident from the curves, the magnitude of the threshold voltage decreases due to with increasing Ge content ( X ) because of decrease in flatband voltage (Eq. (7)), decrease in source-body/ drain-body built-in potential barrier (Eq. (12))and earlier onset of inversion due to decrease in $\phi_{th}$ (Eq. (79)). Now for the sub 75 nm channel length, the threshold falls steeply displaying the short channel behaviour. This is due to the charge sharing in the gate-S/D and also the built-in potential barrier lowering of the source-body/drain-body due to significant overlap of the lateral source-body and drain-body depletion regions ( $x_{dl}$ as in Fig. 2(a)) at such short channel lengths.

Fig. 7 shows the threshold voltage variation against channel length for different gate length ratios ( $L_1 : L_2$ ) and Ge mole fractions ( X ). It is observed that the threshold voltage is higher for the higher control gate length. This may be due to the higher channel barrier height for higher gate length ratio $(L_1 : L_2 = 2:1)$ as predicted in the Fig. 5. Further, the roll-off in the threshold curve is higher for the smaller gate length ratio of the device. This is attributed to the fact that the control gate loses its control over the channel at smaller length ratios. At smaller gate length ratio, the channel barrier height gets reduced giving rise to greater short channel effects.

The only advantage in reducing the gate length ratio is in DIBL as discussed later. In addition, the decrease in the threshold voltage is observed with increasing strain

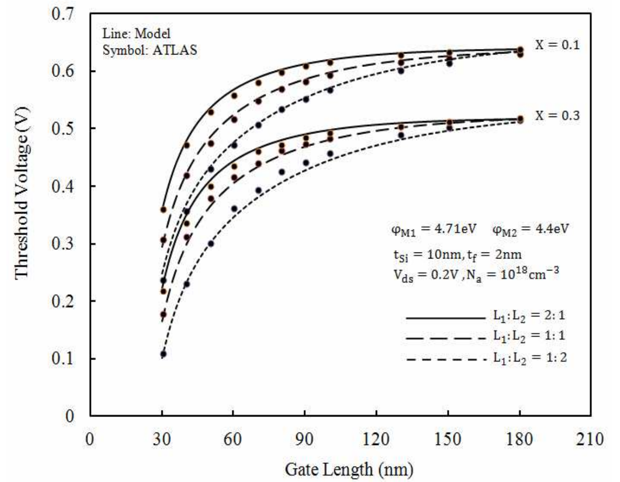


**Fig. 7.** Threshold voltage against device channel length ( $L$ ) with different gate length ratios $(L_1 : L_2)$ for different Ge mole fraction (x) in the $Si_{1-X}Ge_X$ layer, Parameters used: $V_{ds} = 0.2$V, $V_{sub} = 0$V, $N_a = 1\times 10^{18}$ cm$^{-3}$, $t_f = 2$ nm, $t_{Si} = 10$ nm, $\varphi_{M1} = 4.71$eV and $\varphi_{M2} = 4.4$eV.

( X ) which is already discussed in Fig. 7.

Fig. 8 shows the threshold voltage variations with Ge mole fraction variations at different Si film thickness. As seen from the diagram, the threshold voltage is lower for higher strain at the same gate length. It is observed that the threshold voltage reduces considerably in a linear manner with increasing strain.

Fig. 9 shows the variation of the DIBL with gate length for different gate length ratios. The DIBL for a short-channel $s-Si$ on $Si_{1-X}Ge_X$ MOSFET is computed as the difference between the linear ($V_{ds}$ = 0.2 V) and saturation ($V_{ds}$ = 1.2 V) threshold voltages [12]. The threshold voltage is extracted from simulated $I_D - V_{gs}$ curve as mentioned in simulation method and model section of the present manuscript. It is observed that the DIBL is negligible for longer channel lengths (above 100 nm), but is significant for smaller channel lengths (below 60-70 nm). As seen from the Fig. 9, the DIBL increases sharply as the length of the control gate increases. This may be attributed to the shift of the minimum surface potential point towards the drain side when the length of control gate increases for fixed channel length as shown in Fig. 4. It should be noted that if the surface potential point is more close to the drain side, the source channel barrier height will have strong affinity with drain voltage and hence more DIBL will be observed in the device.

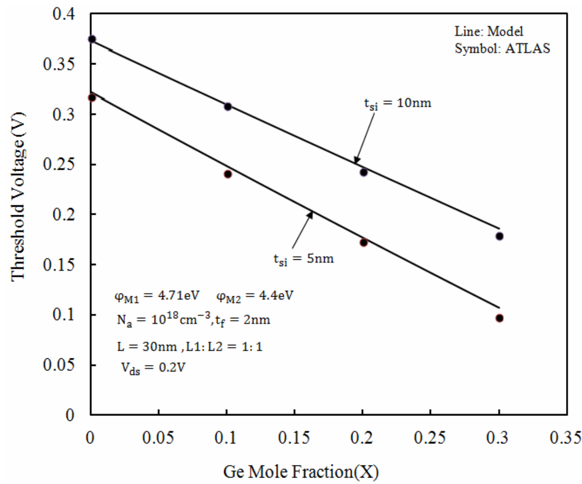


**Fig. 8** Threshold voltage against Ge mole fraction (x) in the $Si_{1-X}Ge_X$ layer for different strained silicon layer thickness ($t_{Si}$). Parameters used: $V_{ds} = 0.2$V, $V_{sub} = 0$V, $L = 30$ nm, $N_a = 1\times10^{18}$ cm$^{-3}$, $L_1 : L_2 = 1:1$, $t_f = 2$ nm, $\varphi_{M1} = 4.71$eV and $\varphi_{M2} = 4.4$eV.

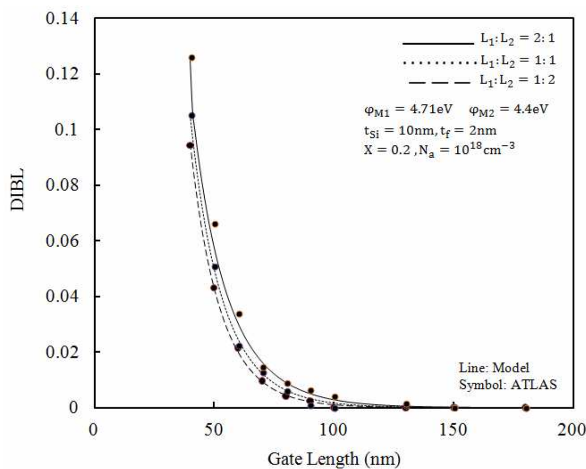


**Fig. 9.** Drain induced barrier lowering (DIBL) against device channel length ($L$) for different gate length ratios ($L_1 : L_2$). Parameters used: X = 0.2, $V_{sub} = 0$V, $L = 30$ nm, $t_f$ = 2 nm, $t_{Si} = 10$ nm, $N_a = 1\times10^{18}$ cm$^{-3}$, $\varphi_{M1} = 4.71$eV and $\varphi_{M2} = 4.4$eV.

## VIII. CONCLUSIONS

The developed 2-D analytical model for surface potential and threshold voltage analyses the effectiveness of DMG structure in an $s-Si$ on $Si_{1-X}Ge_X$ substrate to suppress the hot carrier effects (HCEs) and drain induced barrier lowering (DIBL). The suppression of HCE and DIBL by the introduction of the dual material gate is attributed to the creation of a step-function in the channel potential profile which is verified by the simulations.A extensive analysis of the impact of numerous device parameters on the threshold voltage has been carried out. It may be concluded that the depreciation in the threshold voltage with increasing strain is improved by increasing the length of control gate for the given channel length and increasing the $s-Si$ thickness. Also, modifying the Ge mole fraction and the gate length ratio, DIBL can be controlled effectively. The derived 2-D analytical model is found to be in excellent agreement with the simulation results obtained from ATLAS™ from Silvaco. The developed model may prove to a useful tool to optimize the desired performance of the device parameters.

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**Shiv Bhushan** obtained B.E. in Electronics and Telecommunication Engineering from R.C. Patel Institute of Technology, North Maharashtra University in 2009. He is currently pursuing M.Tech in VLSI and Embedded Systems in NIT Rourkela. His areas of interest are modeling and simulation of strained devices.

**Santunu Sarangi** obtained B.Tech. in Electronics and Telecommunication Engineering from Institute of Technical Education and Research, Biju Patnaik University of Technology, Odisha in 2008. He is currently pursuing M.Tech in VLSI and Embedded Systems in NIT Rourkela. His areas of interest are modeling and simulation of nanoscale devices.

**Gopi Saramekala** obtained B.Tech. in Electronics and Communication Engineering from JNTU, Kakinada, Andhra Pradesh in 2009 and M.Tech from NIT Rourkela in 2012. He is currently working towards his Ph.D at NIT Rourkela in micro-electronics and nanotechnology, area of interest being device modeling and simulation.

**Abirmoya Santra** obtained B.E. in Electronics and Telecommunication Engineering from University of Mumbai in 2011. He is currently pursuing M.Tech in VLSI and Embedded Systems in NIT Rourkela. His areas of interest are Gate-All-Around and Strained MOSFETs.

**Sarvesh Dubey** was born in Varanasi district, Uttar Pradesh (U.P.), India, on September 16, 1985. He received the M.Sc. degree in Physics (Electronics) from U. P. Autonomous College, Varanasi (P.U., Jaunpur) in 2006. Currently, he is pursuing the Ph.D. degree in the Department of Electronics Engineering, Indian Institute of Technology (Banaras Hindu University), Varanasi. He has been the recipient of Junior Research Fellowship (JRF) and Senior Research Fellowship (SRF). His present research interests are modeling and simulation of nanoscale DG MOSFETs and strained MOSFETs. He has published more than 30 papers in various international journals and conferences.

**Dr. P. K. Tiwari** was born in Deoria district, Uttar Pradesh, India in 1981. He received his B.E. degree in Electronics and Telecommunication from CCS University, Meerut in 2002, M.Tech. degree in Electronics Engineering from Aligarh Muslim University, Aligarh in 2007 and Ph.D. degree in Microelectronics Engineering from Indian Institute of Technology (Banaras Hindu University) Varanasi in 2012. While with the BHU, he did an extensive research on the double gate MOSFETs and has pioneered many novel devices and their analysis. He joined the Department of Electronics and Communication Engineering, National Institute of Technology, Rourkela, India, as an Assistant Professor in July 2011 after submitting his Ph. D thesis. His research interests are on VLSI device modeling and simulation for nanoscale applications. He has published extensively in the above area with more than 45 publications in refereed journals and international conferences including one book chapter.