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A New Resistance Model for a Schottky Barrier Diode in CMOS Including N-well Thickness Effect

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Abstract—**A new resistance model for a Schottky Barrier Diode (SBD) in CMOS technology is proposed in this paper. The proposed model includes the n-well thickness as a variable to explain the operational behavior of a planar SBD which is firstly introduced in this paper. The model is verified using the simulation methodology ATLAS. For verification of the analyzed model and the ATLAS simulation results, SBD prototypes are fabricated using a 0.13μm CMOS process. It is demonstrated that the model and simulation results are consistent with measurement results of fabricated SBD.**

Index Terms—**CMOS, capacitance, cut-off frequency, n-well thickness, resistance, Schottky barrier diodes**

I. INTRODUCTION

As research interest in RF circuits extends to higher frequency, up to even terahertz range, high speed operation of RF circuit becomes a critical factor in amplifier, mixer, oscillator, detector, etc. CMOS technology is a good choice in terms of cost and the integration. However, the switching speed of CMOS transistors limits the high frequency performance. To overcome the speed limitation, researches on Schottky barrier diode (SBD) in CMOS technology has recently been carried out [1, 2]. The SBD which has a Schottky barrier junction formed by a metal and a lowly-doped semiconductor is a fast device. Since the SBD is a majority carrier device, its switching speed is fast and also its resistance and capacitance values are small due to its simple structure. The SBD therefore can have relatively high cut-off frequency (f_T) which is an index to evaluate the high frequency performance of a device.

In the GaAs planar SBD, a decrease in the thickness of the n-type-layer results in a decrease of the cut-off frequency [3]. On the other hand, in the SiGe planar SBD, a decrease in the thickness of the n-type-layer results in a decrease of the resistance, which leads to an increase of the cut-off frequency [4]. The thickness of the n-type-layer thus is an important parameter that affects the cut-off frequency of the SBD. Although the CMOS SBDs presented in [1, 2] show good performance, the authors did not explain how process selects parameters and did not conduct simulations based on a theoretical analysis. With technology scaling, an accurate model that incorporates the layer thickness is needed for the CMOS SBD design.

In this paper, a new resistance model for a CMOS SBD that takes into account the n-well thickness effect is analyzed and verified with the ATLAS device simulator. Several prototypes are fabricated in a 0.13μm CMOS process and evaluated to verify the proposed model and the simulation results.

II. RESISTANCE MODEL FOR A CMOS SBD

Fig. 1 shows a basic SBD structure: a Dot-matrix SBD [5]. In Fig. 1, R_1 is the vertical spreading resistance, R_2 is the horizontal spreading resistance of the undepleted n-layer, R_3 is the sidewall resistance. At the metal-n-layer junction, junction capacitance C_{j0} exists. Among the

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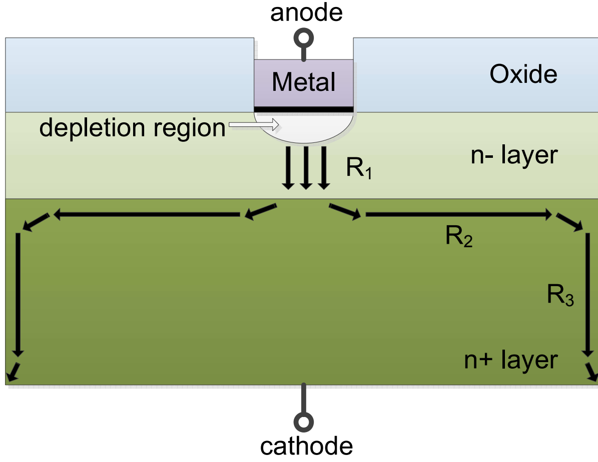


Fig. 1. Current distribution in the Dot-matrix Schottky barrier diode.

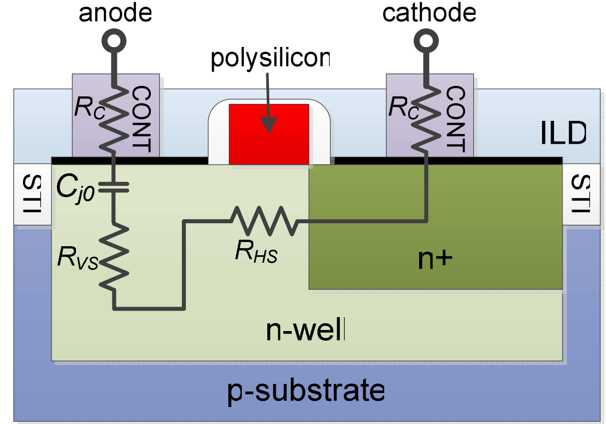


Fig. 2. Cross section of a planar Schottky barrier diode.

resistance components indicated in Fig. 1, R_1 is the most significant factors related to the cut-off frequency. The cut-off frequency is expressed as

$$f_T = \frac{1}{2\pi R C_{j0}} \quad . \tag{1}$$

In Eq. (1), R is the sum of R_1, R_2, and R_3, and they are respectively defined as [5];

$$\begin{aligned} R_1 &= \frac{4(t-d)}{\pi a^2 q \mu_n N_d} \;, \\ R_2 &= \frac{ln(b/a)}{2\pi\delta q \mu_n N_d} \;, \\ R_3 &= \frac{h}{\pi b \delta q \mu_n N_d} \;, \end{aligned} \tag{2}$$

and

$$C_{j0} = \frac{\pi a^2}{4}\sqrt{q\varepsilon_s N_D/2\phi_{bi}} \;.. \tag{3}$$

Here, a is the diameter of the anode, b is the diameter of the cathode, q is the electron charge, μ_n is the mobility of n- layer, N_d is the doping concentration of the n- layer, t is the thickness of the n-layer, d is the thickness of the depleted n-layer, δ is the skin depth of the n- layer, ε_s is the permittivity of the n-layer, and φ_{bi} is the Schottky barrier height. The previously reported SBD model expressed in (2) and (3), however, is not suitable to CMOS SBD, because it can only be realized in a planar structure where the anode and the cathode should be positioned on the same surface, contrary to the structure illustrated in Fig. 1.

Fig. 2 shows the structure and equivalent circuit of a planar SBD in CMOS technology. Planar SBD has rectangular structure while dot-matrix diode has circular structure. In Fig. 2, the polysilicon separates the anode and cathode of the SBD. This structure offers a minimum spreading resistance [2]. In this structure, the R of the SBD can be described by the combination of the vertical spreading resistance (R_{VS}) and horizontal spreading resistance (R_{HS}) in the n-well region and the contact resistances (R_C) as follows:

$$\begin{aligned} R &= \sqrt{R_{VS}^2 + R_{HS}^2} + R_C \\ &= \sqrt{\left(\frac{t-d}{wlq\mu_n N_d}\right)^2 + \left(\frac{s+\frac{l}{n}}{wtq\mu_n N_d}\right)^2} + R_C \\ &= \frac{1}{wq\mu_n N_d}\sqrt{\left(\frac{t-d}{l}\right)^2 + \left(\frac{s+l/n}{t}\right)^2} + R_c \,. \end{aligned} \tag{4}$$

In Eq. (4), t is the thickness of the n-well region, d is the thickness of the depleted n-well region, s is the minimum distance between the anode and cathode, l is the anode length, w is the anode width, and n is the current spreading factor, which has a value of 2~3 [6]. R_{VS} which corresponds to R_1 is inversely proportional to the anode area and proportional to the thickness of the undepleted n-well region. On the other hand, note that R_{HS} is newly proposed for CMOS planar SBD instead of R_2 in (2). From (4), a smaller t increases R_{HS}, because the

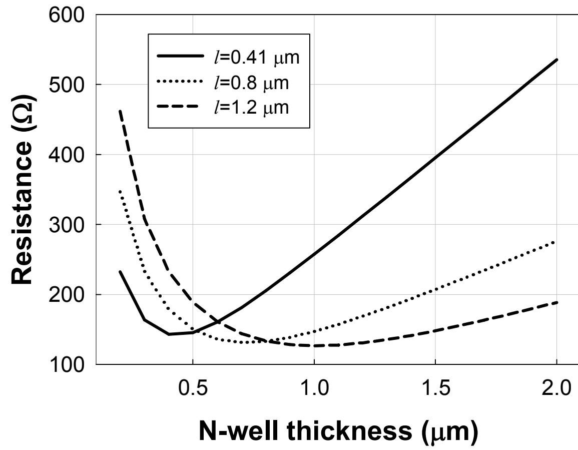


Fig. 3. Calculated resistance based on (4).

current path of the diode is limited by t. A larger $s+l/n$ increases the length of current path in n-well, thus it also increases R_{HS}. R_C is the contact resistance, which is regarded as very small value.

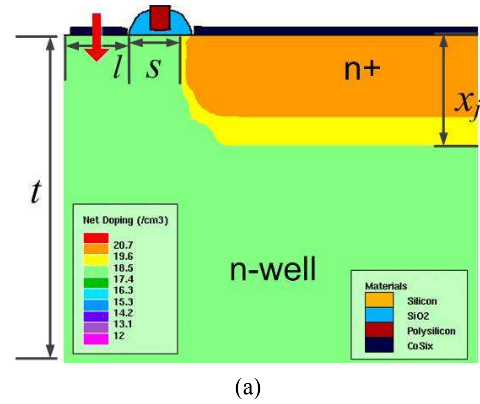
When the n-well is very thin, R_{HS} dominates the total resistance of the SBD, whereas when the n-well is thick enough, then the current path is unaffected by t and R_{VS} becomes the dominant component. Fig. 3 shows the calculated resistance of a planar SBD based on (4) for three different anode lengths as a function of the n-well thickness, while the width of the anode is fixed at 1.04 µm.

For the calculation, d=0.1 µm, n=2, s=0.2 µm, μ_n=800 cm^2/V-s, N_d=6.5·10^{17}/cm^3, and R_C=0 are adopted. In Fig. 3, when the n-well thickness is relatively thin (<0.5µm), R_{HS} is dominant and thus larger anode length leads to higher overall total resistance. On the other hand, when the n-well is relatively thick, narrower anode length shows lower total resistance since R_{VS} becomes the dominant factor and is inversely proportional to the anode area. Therefore, the anode length should be selected differently according to the thickness of the n-well.

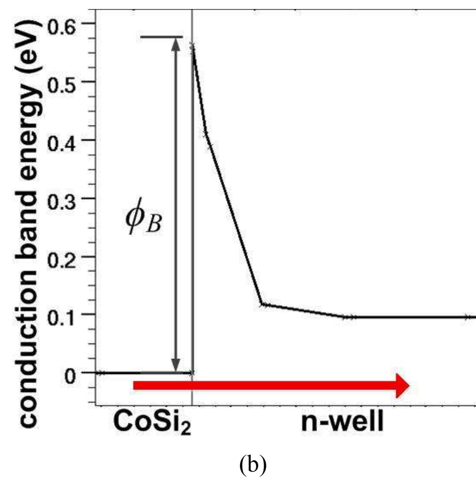
The main factor of the capacitance in the CMOS planar SBD is the junction capacitance between the metal and n-well and it is proportional to the anode area as in (3).

III. Model Verification using ATLAS

Fig. 4(a) shows the cross section of a planar SBD realized by ATLAS. In Fig. 4(a), the bulk semiconductor material is silicon because this SBD is based on a CMOS process.



(a)



(b)

Fig. 4. (a) Cross section of a planar SBD from ATLAS simulation, (b) conduction energy band diagram of metal-n-well junction.

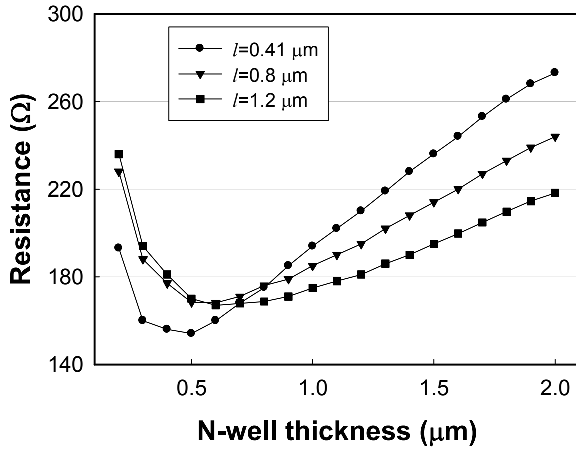
Table 1. Process variables for ATLAS simulation

Variable	Value
N_{D-} (for n-well)	6.5·10^{17}/cm^3
N_{D+} (for n+ region)	5·10^{20}/cm^3
x_j(n+ depth)	0.45 um
N_A (for p-substrate)	1.5·10^{17}/cm^3
φ_B (Barrier height)	0.56 eV

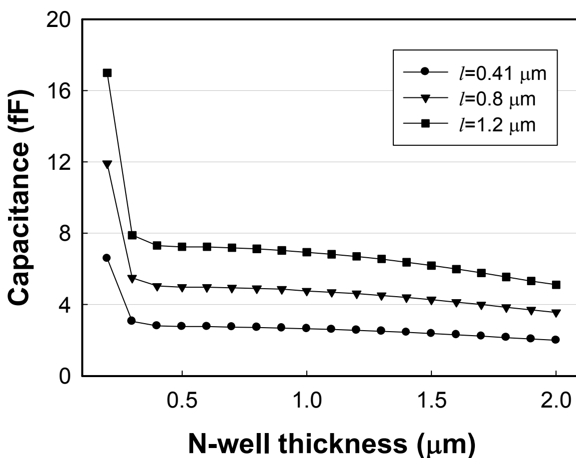
There are several process and dimension variables in the simulation. The doping concentrations of the p-substrate, n-well, and n+ region, and the barrier height of the Schottky junction belong to process variables, which are pre-determined in a given 0.13 µm CMOS technology.

In particular, the doping concentrations of the n-well and p-substrate are extracted from the conductivity information. For example, the conductivity of the n-well is $\sigma_{n-} = q\mu_n N_D$, and so, N_D can be extracted using the inversely proportional relationship between μ_n and

N_D [7]. $CoSi_2$, a well known silicide material, is used for the contact metal. Fig. 4(b) shows the form of the Schottky barrier between CoSi2 and the n-well region. The size of the anode and the cathode, the length of polysilicon, and the n-well thickness are dimension variables. In the simulation, for n-well thickness range of 0.2 μm to 2-μm and three different anode lengths, the resistance and capacitance of each SBD are extracted from a 2-port S-parameter analysis over the frequency range of 10 to 20-GHz. The width of each SBD is fixed at 1.04 μm. Fig. 5 shows the simulation results of the resistance and capacitance extracted from ATLAS simulator. As shown in Fig. 5(a), the simulation results agree well with the proposed model of the total resistance for CMOS SBD. Because the proposed model deals only with the resistance from the drift current, which is the dominant current of the SBD, there is a slight mismatch between the simulation and model. In Fig. 5(b), the capacitance of the SBD becomes higher as the anode length increases. When the n-well is thicker than a certain point (0.4 μm in this case), the capacitance is nearly constant for each anode length. Although the capacitance seems to be affected by the n-well thickness, the degree of this effect is much less significant than that of the anode area.



(a)



(b)

Fig. 5. Simulation result for (a) resistance, (b) capacitance as a function of the n-well thickness and the anode length.

IV. FABRICATION AND MEASUREMENT

Fig. 6 shows a micrograph of the fabricated chip. Several prototypes of the Schottky barrier diode were fabricated in a 0.13 μm CMOS process. Each prototype is designed to have different anode and cathode areas (length, width) while varying the number of cells. Fig. 7 shows measured I-V characteristics of three prototypes that have different anode lengths while the anode width is fixed at 1.04 μm. By adapting saturation current to equation [8], schottky barrier height is extracted as 0.56 eV on average. The S-parameters of the 0V biased SBDs are measured in a 1-port configuration with a vector network analyzer over the frequency range of 10 to 20-GHz. From measured S11, R and C are extracted and cut-off frequency is calculated using (5).

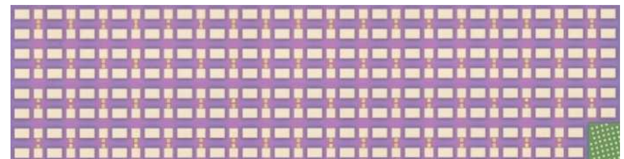


Fig. 6. Micrograph of several prototypes of Schottky barrier diode.

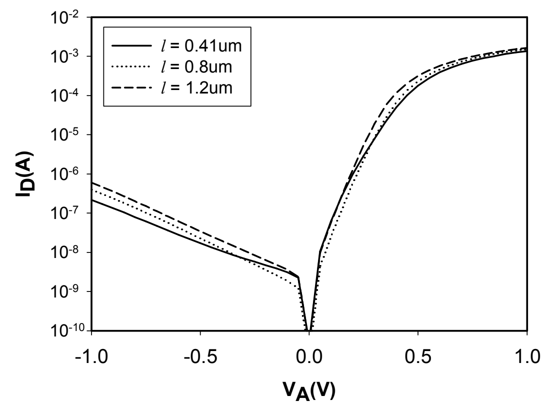
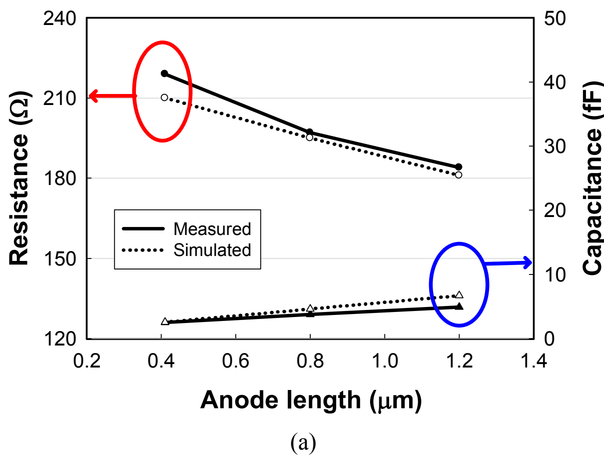


Fig. 7. Measured I-V characteristic of fabricated SBD.

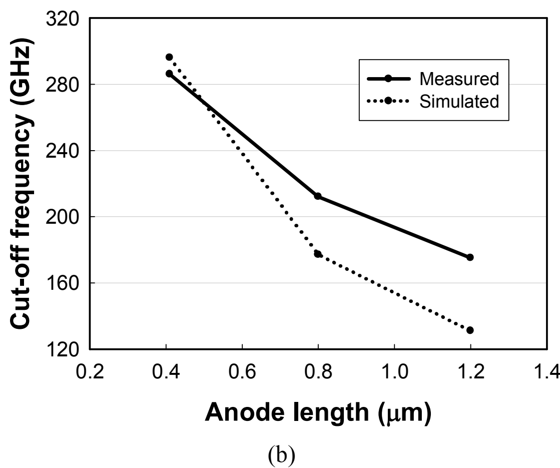
$$Z = \frac{1-S11}{1+S11} = R + \frac{1}{j\omega C} \quad (5)$$

Primary calibration is done by a calibration substrate, and the capacitances from pads are removed by an open dummy pattern.

Fig. 8(a) shows the simulated and measured resistance and capacitance of three prototypes that have different anode lengths while the anode width is fixed at 1.04μm. The n-well thickness for the prototypes is estimated as 1.2μm from the PDK, and this value is used for the simulation. In Fig. 8(a), the measurement results are in good agreement with the proposed model and simulation results; specifically, the total resistance becomes smaller with larger anode length in a thick n-well. The measured values of the resistance are slightly higher than that of the simulation results. This is attributed to the lack of calibration for the metal sheet resistance and the R_C effect in the simulation. Due to the lack of process



(a)



(b)

Fig. 8. (a) Simulated and measured resistance and capacitance, (b) corresponding cut-off frequency.

information, there are some error among calculation, simulation and measurement. As shown in Fig. 8(b), from the measured resistance and capacitance, the highest cut-off frequency of the prototype SBD is 286 GHz, when the anode length is 0.41 μm.

V. CONCLUSION

The dependency of the n-well thickness on the resistance of the CMOS Schottky barrier diode is described by a newly proposed resistance model in this paper. Depending on the dimension of the n-well thickness, the dominant resistance factor is changed. In the case of a thin n-well structure, short anode length is preferred for low dominant horizontal resistance, while long anode length improves the total resistance by decreasing the dominant vertical resistance in a thick n-well structure. The proposed model is verified with an ATLAS simulation and measurement of prototypes fabricated in a 0.13 μm CMOS process. As the n-well thickness is predicted to decrease with CMOS technology scaling, the proposed resistance model and the verification results can be very helpful for the design of CMOS SBDs in each technology considering the n-well thickness.

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